

MJE18002G

Switch-mode

NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE18002G have an applications specific state-of-the-art die designed for use in 220 V line operated Switch-mode Power supplies and electronic light ballasts.

Features

- Improved Efficiency Due to Low Base Drive Requirements:
 - ◆ High and Flat DC Current Gain h_{FE}
 - ◆ Fast Switching
 - ◆ No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot-to-Lot
- Standard TO-220
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector-Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter-Base Voltage	V_{EBO}	9.0	Vdc
Collector Current – Continuous	I_C	2.0	Adc
– Peak (Note 1)	I_{CM}	5.0	
Base Current – Continuous	I_B	1.0	Adc
– Peak (Note 1)	I_{BM}	2.0	
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	50 0.4	W W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{stg}	-65 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

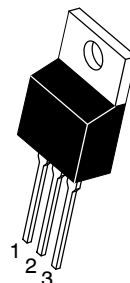
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



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**POWER TRANSISTOR
2.0 AMPERES
100 VOLTS – 50 WATTS**



TO-220AB
CASE 221A-09
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE18002G	TO-220 (Pb-Free)	50 Units / Rail

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I _C = 100 mA, L = 25 mH)	V _{CEO(sus)}	450	–	–	Vdc	
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , I _B = 0)	I _{CEO}	–	–	100	μAdc	
Collector Cutoff Current (V _{CE} = Rated V _{CEs} , V _{EB} = 0) (V _{CE} = 800 V, V _{EB} = 0)	I _{CES}	–	–	100 500 100	μAdc	
Emitter Cutoff Current (V _{EB} = 9.0 Vdc, I _C = 0)	I _{EBO}	–	–	100	μAdc	
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I _C = 0.4 Adc, I _B = 40 mAdc) (I _C = 1.0 Adc, I _B = 0.2 Adc)	V _{BE(sat)}	–	0.825 0.92	1.1 1.25	Vdc	
Collector–Emitter Saturation Voltage (I _C = 0.4 Adc, I _B = 40 mAdc) (I _C = 1.0 Adc, I _B = 0.2 Adc)	V _{CE(sat)}	–	0.2 0.2 0.25 0.3	0.5 0.5 0.5 0.6	Vdc	
DC Current Gain (I _C = 0.2 Adc, V _{CE} = 5.0 Vdc) (I _C = 0.4 Adc, V _{CE} = 1.0 Vdc) (I _C = 1.0 Adc, V _{CE} = 1.0 Vdc) (I _C = 10 mAdc, V _{CE} = 5.0 Vdc)	h _{FE}	14 – 11 11 6.0 5.0 10	– 27 17 20 8.0 8.0 20	34 – – – – – –	–	
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I _C = 0.2 Adc, V _{CE} = 10 Vdc, f = 1.0 MHz)	f _T	–	13	–	MHz	
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)	C _{ob}	–	35	60	pF	
Input Capacitance (V _{EB} = 8.0 V)	C _{ib}	–	400	600	pF	
Dynamic Saturation: determined 1.0 μs and 3.0 μs after rising I _{B1} reach 0.9 final I _{B1} (see Figure 18)	I _C = 0.4 A I _{B1} = 40 mA V _{CC} = 300 V	1.0 μs 3.0 μs	@ T _C = 125°C @ T _C = 125°C	V _{CE(dsat)} – – – – – –	3.5 8.0 1.5 3.8 8.0 14 2.0 7.0	– – – – – – – –

2. Proper strike and creepage distance must be provided.

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ELECTRICAL CHARACTERISTICS – continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS: Resistive Load ($D.C. \leq 10\%$, Pulse Width = 20 μs)

Turn-On Time	$I_C = 0.4 \text{ Adc}$ $I_{B1} = 40 \text{ mAdc}$ $I_{B2} = 0.2 \text{ Adc}$ $V_{CC} = 300 \text{ V}$	@ $T_C = 125^\circ\text{C}$	t_{on}	– –	200 130	300 –	ns
Turn-Off Time		@ $T_C = 125^\circ\text{C}$	t_{off}	– –	1.2 1.5	2.5 –	μs
Turn-On Time	$I_C = 1.0 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$ $V_{CC} = 300 \text{ V}$	@ $T_C = 125^\circ\text{C}$	t_{on}	– –	85 95	150 –	ns
Turn-Off Time		@ $T_C = 125^\circ\text{C}$	t_{off}	– –	1.7 2.1	2.5 –	μs

SWITCHING CHARACTERISTICS: Inductive Load ($V_{clamp} = 300 \text{ V}$, $V_{CC} = 15 \text{ V}$, $L = 200 \mu\text{H}$)

Fall Time	$I_C = 0.4 \text{ Adc}$, $I_{B1} = 40 \text{ mAdc}$, $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 125^\circ\text{C}$	t_{fi}	– –	125 120	200 –	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	t_{si}	– –	0.7 0.8	1.25 –	μs
Crossover Time		@ $T_C = 125^\circ\text{C}$	t_c	– –	110 110	200 –	ns
Fall Time	$I_C = 1.0 \text{ Adc}$, $I_{B1} = 0.2 \text{ Adc}$, $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 125^\circ\text{C}$	t_{fi}	– –	110 120	175 –	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	t_{si}	– –	1.7 2.25	2.75 –	μs
Crossover Time		@ $T_C = 125^\circ\text{C}$	t_c	– –	200 250	300 –	ns
Fall Time	$I_C = 0.4 \text{ Adc}$, $I_{B1} = 50 \text{ mAdc}$, $I_{B2} = 50 \text{ mAdc}$	@ $T_C = 125^\circ\text{C}$	t_{fi}	– –	140 185	200 –	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	t_{si}	– –	2.2 2.5	3.0 –	μs
Crossover Time		@ $T_C = 125^\circ\text{C}$	t_c	– –	140 220	250 –	ns

TYPICAL STATIC CHARACTERISTICS

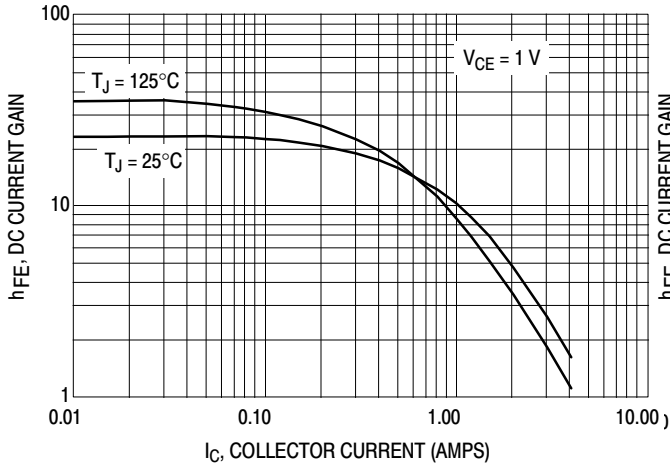


Figure 1. DC Current Gain @ 1 Volt

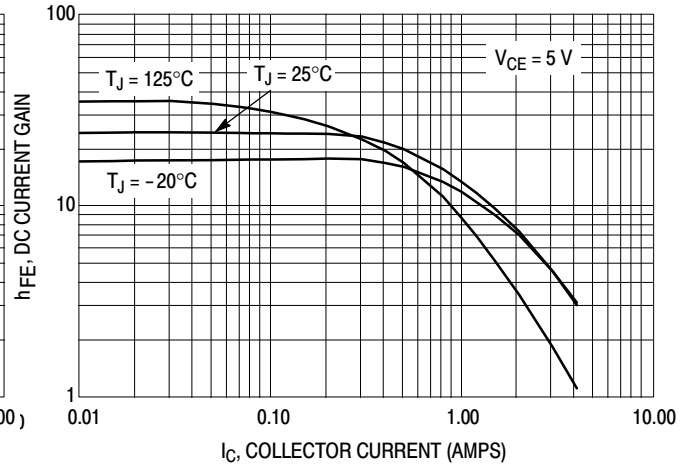


Figure 2. DC Current Gain @ 5 Volts

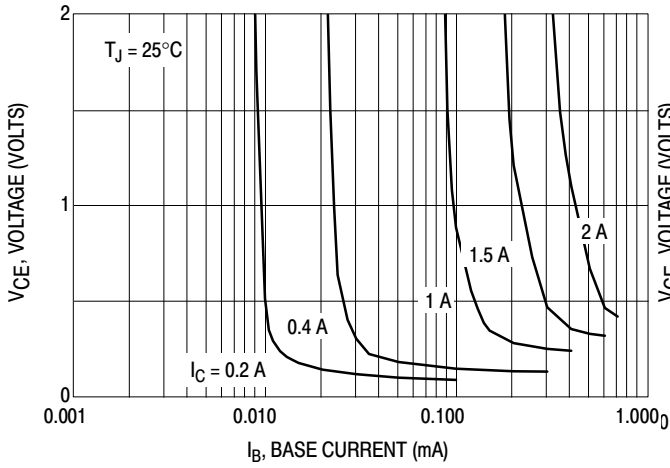


Figure 3. Collector Saturation Region

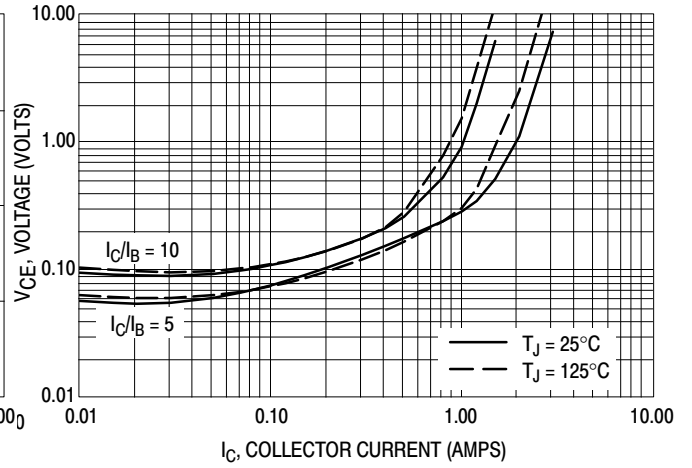


Figure 4. Collector-Emitter Saturation Voltage

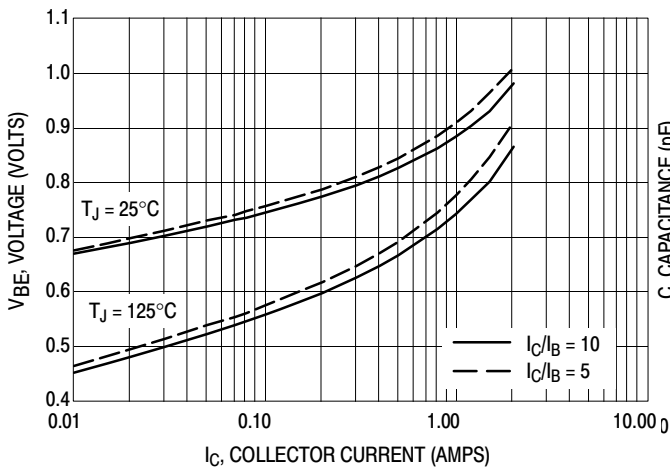


Figure 5. Base-Emitter Saturation Region

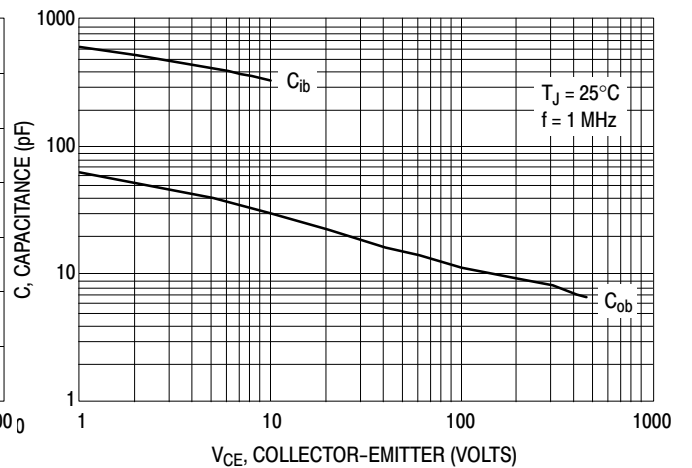


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

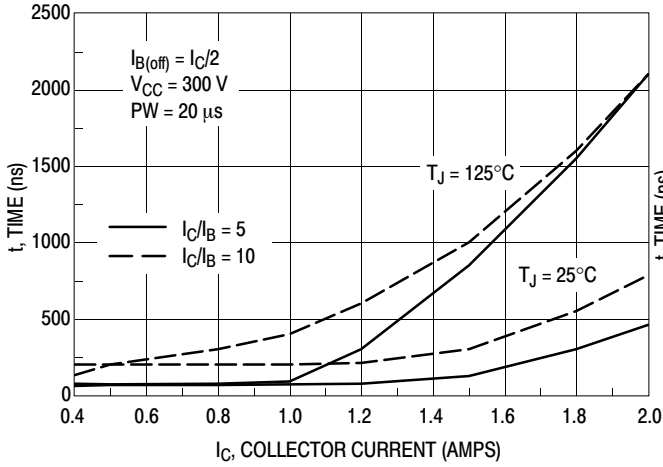


Figure 7. Resistive Switching, t_{on}

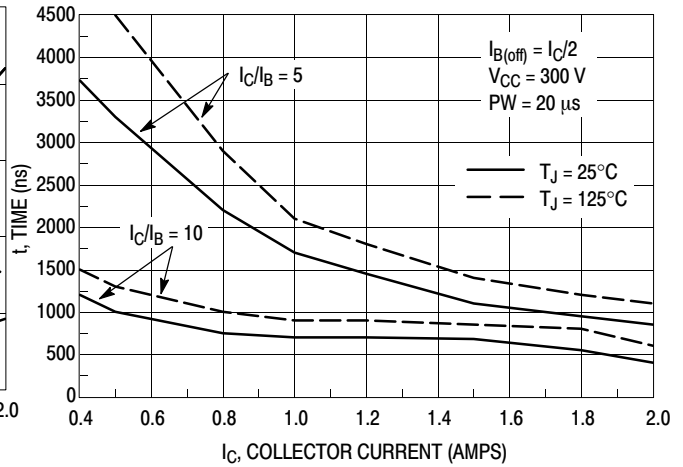


Figure 8. Resistive Switching, t_{off}

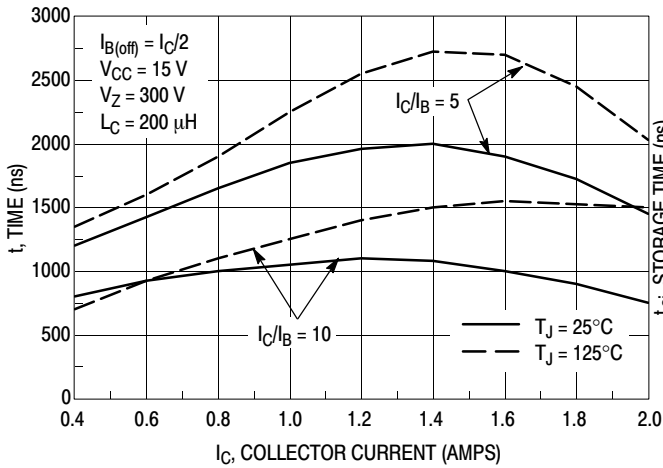


Figure 9. Inductive Storage Time, t_{si}

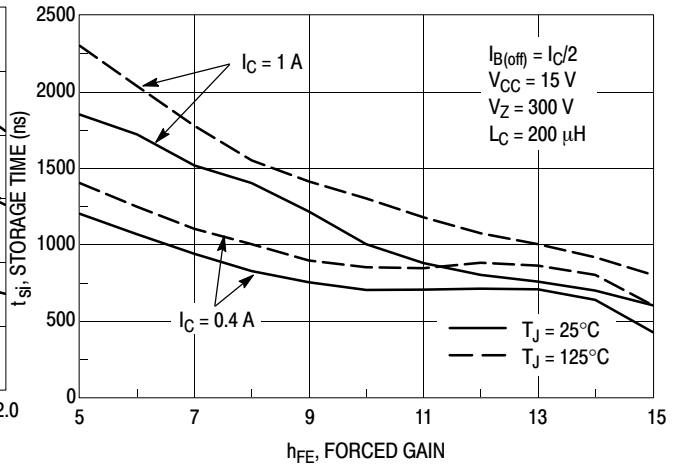


Figure 10. Inductive Storage Time

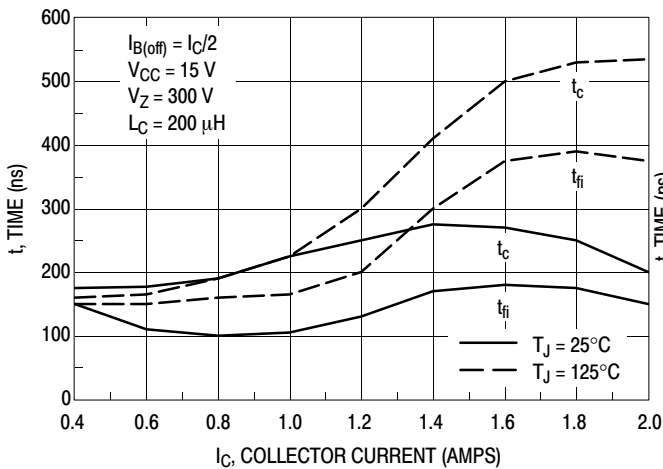


Figure 11. Inductive Switching, t_c and t_{fi} , $I_C/I_B = 5$

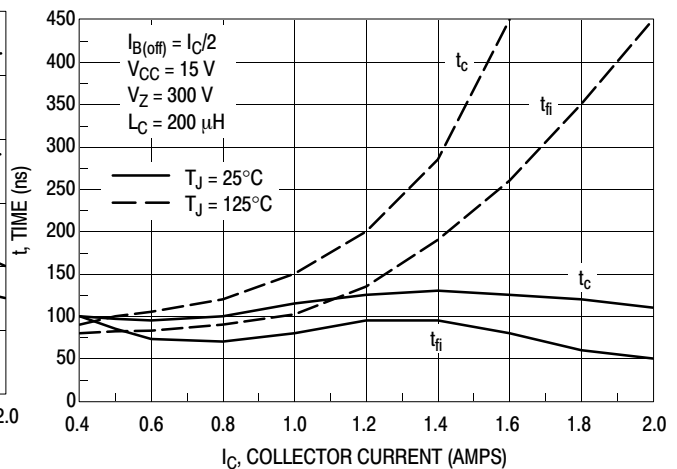


Figure 12. Inductive Switching, t_c and t_{fi} , $I_C/I_B = 10$

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TYPICAL SWITCHING CHARACTERISTICS ($I_{B2} = I_C/2$ for all switching)

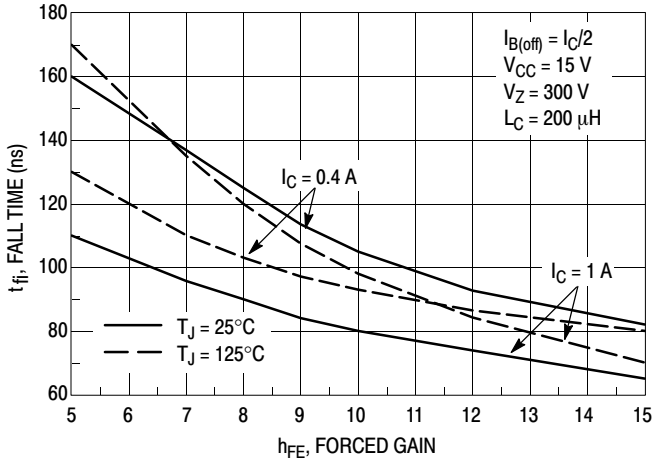


Figure 13. Inductive Fall Time

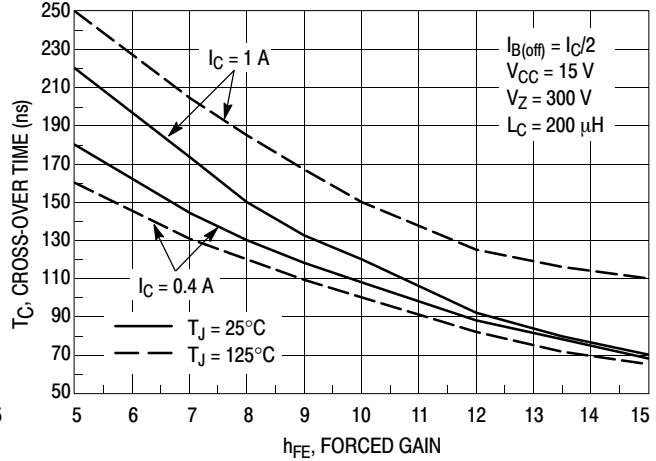


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

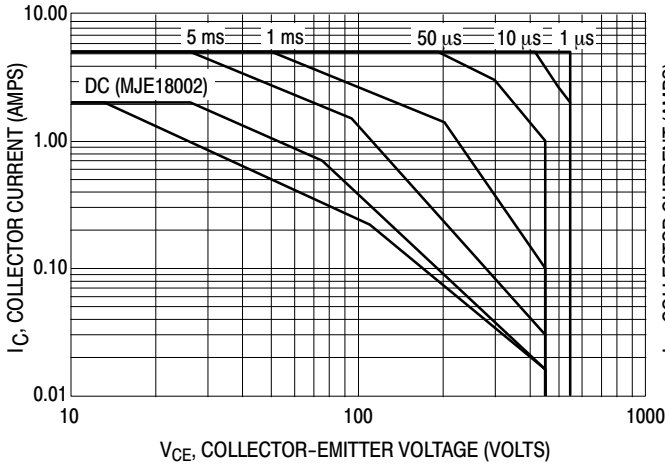


Figure 15. Forward Bias Safe Operating Area

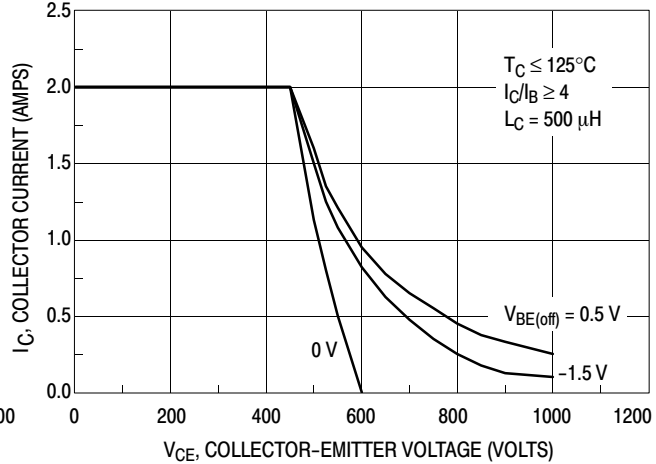


Figure 16. Reverse Bias Switching Safe Operating Area

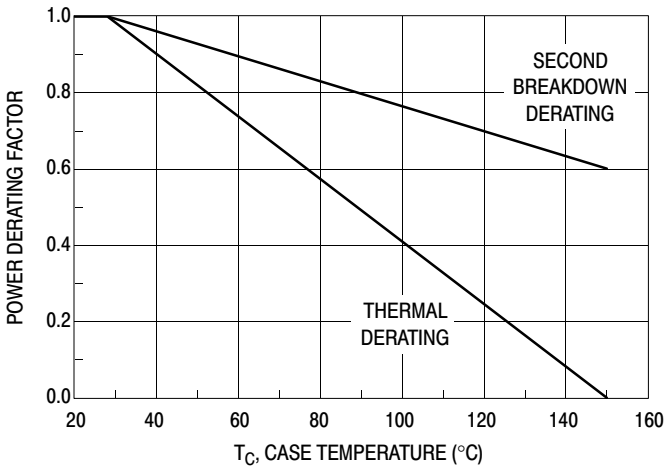


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_J(\text{pk})$ may be calculated from the data in Figures 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

MJE1802G

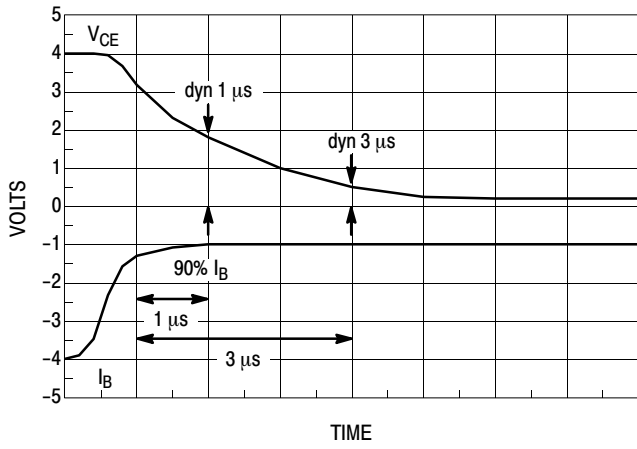


Figure 18. Dynamic Saturation Voltage Measurements

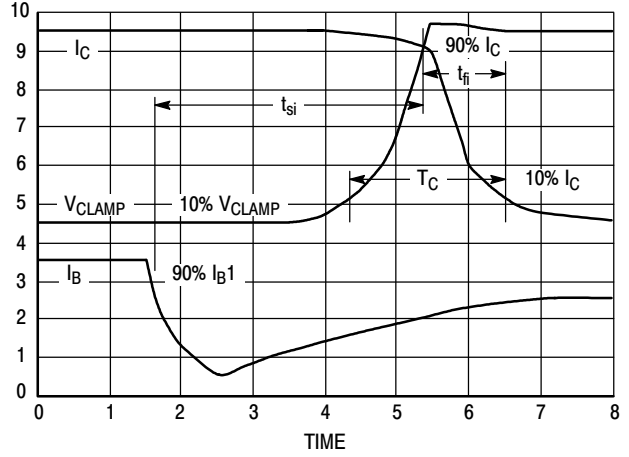
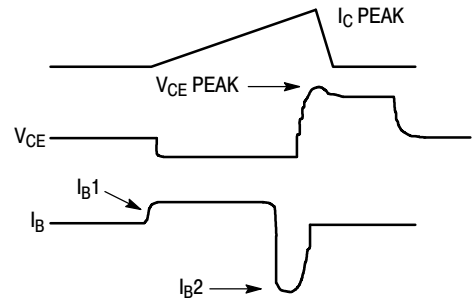
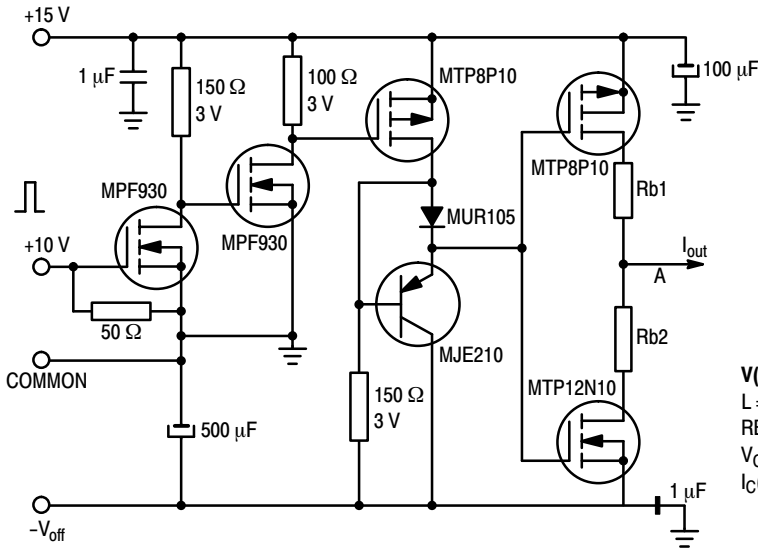


Figure 19. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 μH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
VCC = 20 VOLTS	VCC = 15 VOLTS	VCC = 15 VOLTS
IC(pk) = 100 mA	RB1 SELECTED FOR DESIRED IB1	RB1 SELECTED FOR DESIRED IB1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

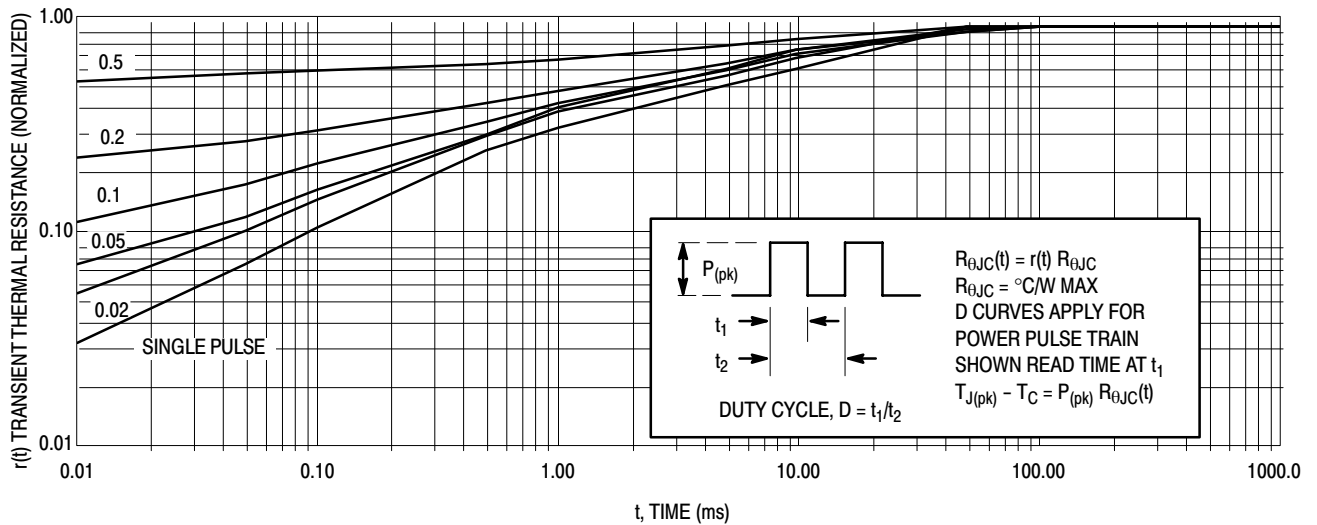
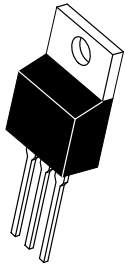
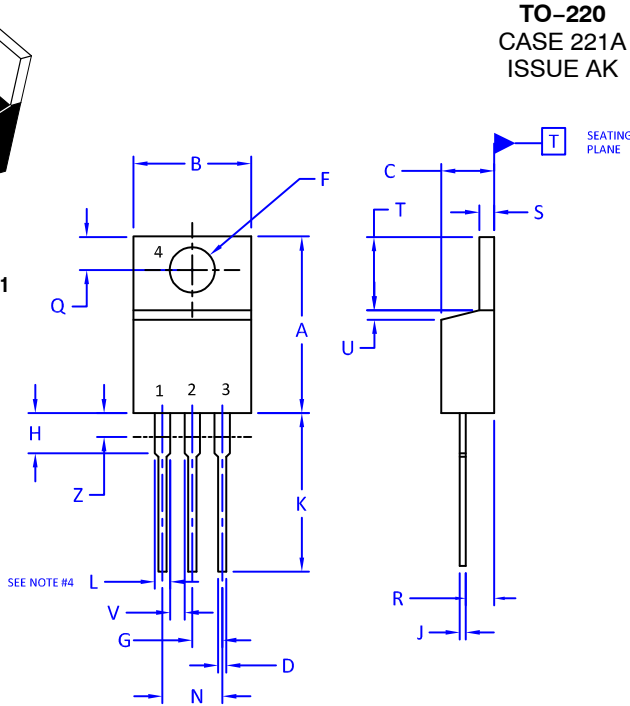


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE1802

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1



TO-220 CASE 221A ISSUE AK

DATE 13 JAN 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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