

N-Channel Logic Level Enhancement Mode Field Effect Transistor

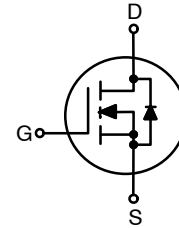
BSS123L

Description

This N-channel enhancement mode field effect transistor is produced using high cell density, trench MOSFET technology. This product minimizes on-state resistance while providing rugged, reliable and fast switching performance. This product is particularly suited for low-voltage, low-current applications such as small servo motor control, power MOSFET gate drivers, logic level transistor, high speed line drivers, power management/power supply and switching applications.

Features

- 0.17 A, 100 V
 - ◆ $R_{DS(on)} = 6 \Omega @ V_{GS} = 10 \text{ V}$
 - ◆ $R_{DS(on)} = 10 \Omega @ V_{GS} = 4.5 \text{ V}$
- High Density Cell Design for Low $R_{DS(ON)}$
- Rugged and Reliable
- Compact Industry Standard SOT-23 Surface Mount Package
- Very Low Capacitance
- Fast Switching Speed
- This Device is Pb-Free and Halogen Free

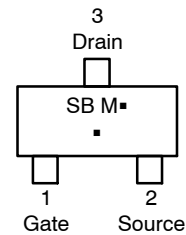


N-Channel



SOT-23-3
CASE 318-08

MARKING DIAGRAM



- SB = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
BSS123L	SOT-23-3 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain–Source Voltage	100	V
V _{GSS}	Gate–Source Voltage	±20	V
I _D	Maximum Drain Current – Continuous	0.17	A
	Maximum Drain Current – Pulsed	0.68	
T _J , T _{STG}	Operating and Storage Temperature Range	–55 to +150	°C
T _L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 s	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
PD	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above 25°C	2.8	mW/°C
R _{θJA}	Thermal Resistance, Junction–to–Ambient (Note 1)	380	°C/W

ESD RATING (Note 2)

Symbol	Parameter	Value	Unit
HBM	Human Body Model per ANSI/ESDA/JEDEC JS-001-2012	50	V
CDM	Charged Device Model per JEDEC C101C	>2000	V

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	100	103	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	100	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 100 V, V _{GS} = 0 V	–	0.027	1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 125°C	–	0.159	60	
		V _{DS} = 20 V, V _{GS} = 0 V	–	0.07	10	nA
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	0.036	50	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = –20 V, V _{DS} = 0 V	–	–0.019	–50	nA

ON CHARACTERISTICS (Note 3)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 1 mA	0.8	1.405	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	–	–2.82	–	mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 0.17 A	–	2.98	6	Ω
		V _{GS} = 4.5 V, I _D = 0.17 A	–	3.17	10	
		V _{GS} = 10 V, I _D = 0.17 A, T _J = 125°C	–	5.63	12	
I _{D(ON)}	On–State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	0.680	0.735	–	A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 0.17 A	0.08	2.13	–	S

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	–	21.5	–	pF
C_{oss}	Output Capacitance		–	3.52	–	
C_{rss}	Reverse Transfer Capacitance		–	1.67	–	
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$	–	7.18	–	Ω

SWITCHING CHARACTERISTICS (Note 3)

$t_{d(on)}$	Turn-On Delay	$V_{DD} = 30\text{ V}, I_D = 0.28\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	–	2.2	3.4	ns
t_r	Turn-On Rise Time		–	1.7	18	
$t_{d(off)}$	Turn-Off Delay		–	5.9	31	
t_f	Turn-Off Fall Time		–	5.6	5	
Q_g	Total Gate Charge	$V_{DS} = 30\text{ V}, I_D = 0.22\text{ A},$ $V_{GS} = 10\text{ V}$	–	0.793	2.5	nC
Q_{gs}	Gate-Source Charge		–	0.092	–	
Q_{gd}	Gate-Drain Charge		–	0.171	–	

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 440\text{ mA}$ (Note 1)	–	0.867	1.3	V
T_{rr}	Diode Reverse Recovery Time	$I_F = 0.2\text{ A}, d_{if}/d_t = 100\text{ A}/\mu\text{s}$	–	11.9	–	ns
Q_{rr}	Diode Reverse Recovery Charge		–	1.3	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
 - $380^\circ\text{C}/\text{W}$ when mounted on a minimum pad.



- ESD values are in typical, no over-voltage rating is implied, ESD CDM zap voltage is 2000 V maximum.
- Pulse test: pulse width $\leq 300\text{ ms}$, duty cycle $\leq 2.0\%$.

TYPICAL CHARACTERISTICS

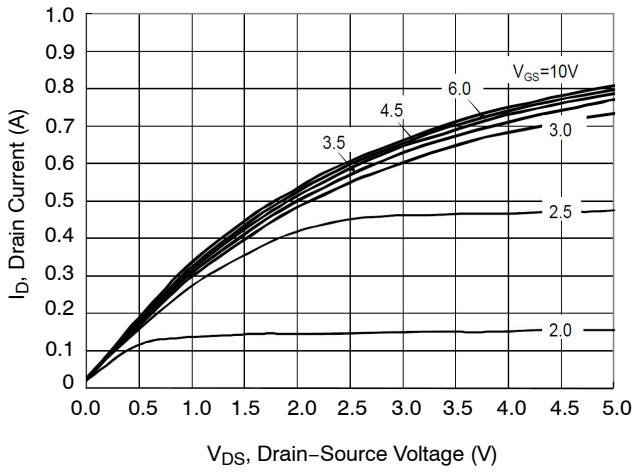


Figure 1. On-Region Characteristics

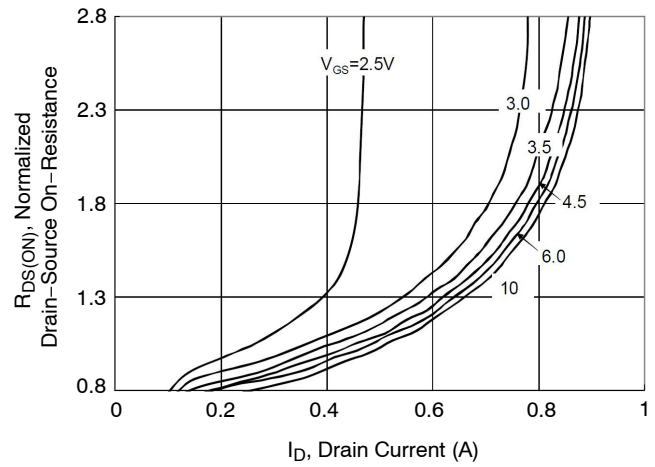


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

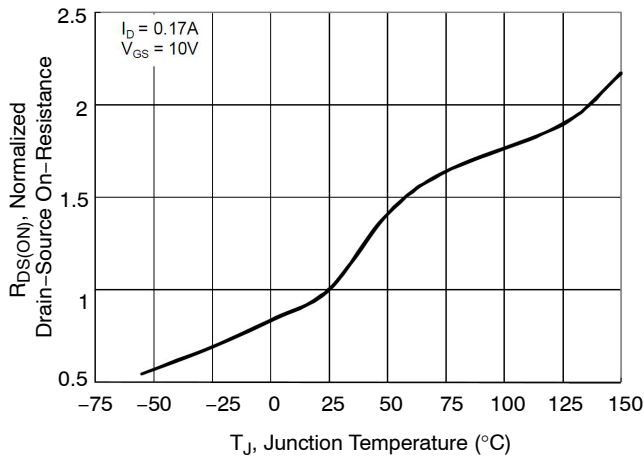


Figure 3. On-Resistance Variation with Temperature

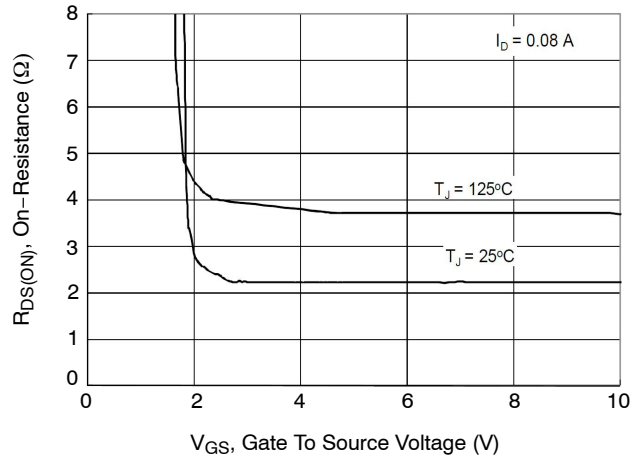


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

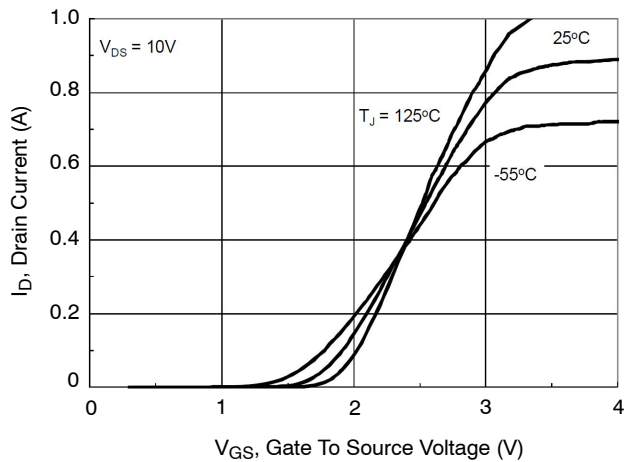


Figure 5. Transfer Characteristics

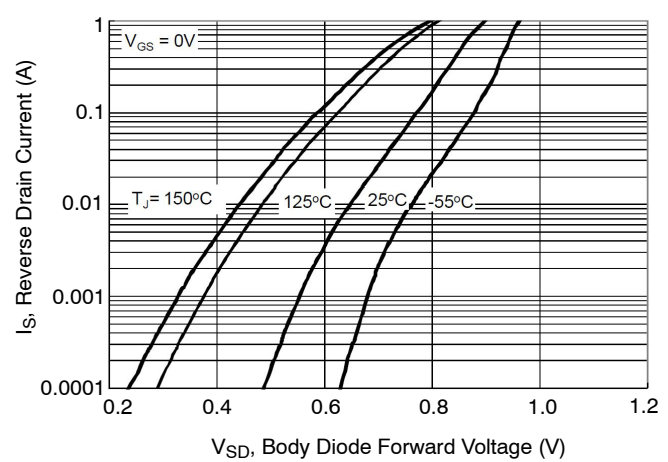


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

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TYPICAL CHARACTERISTICS (continued)

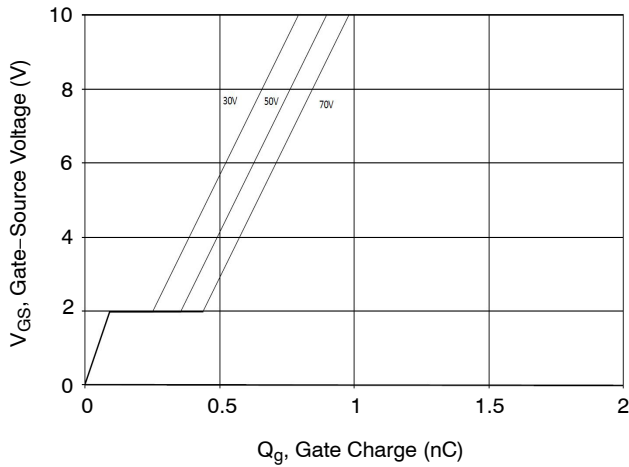


Figure 7. Gate Charge Characteristics

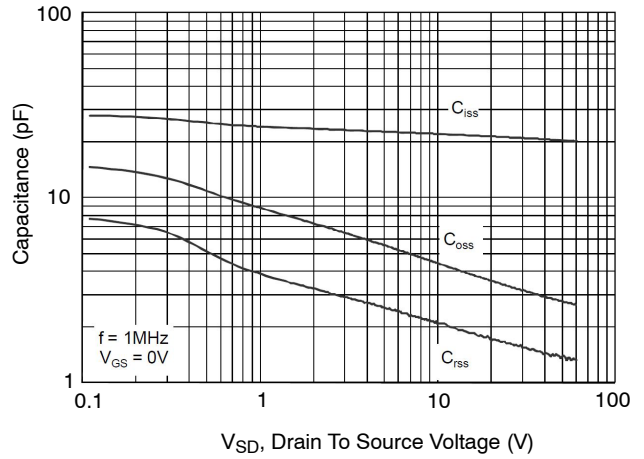


Figure 8. Capacitance Characteristics

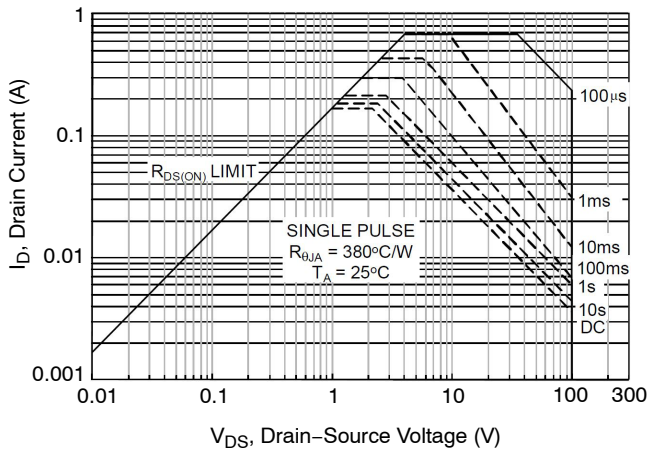


Figure 9. Maximum Safe Operating Area

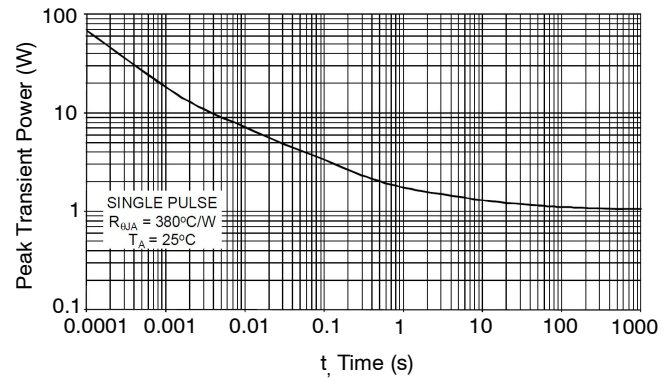


Figure 10. Single Pulse Maximum Power Dissipation

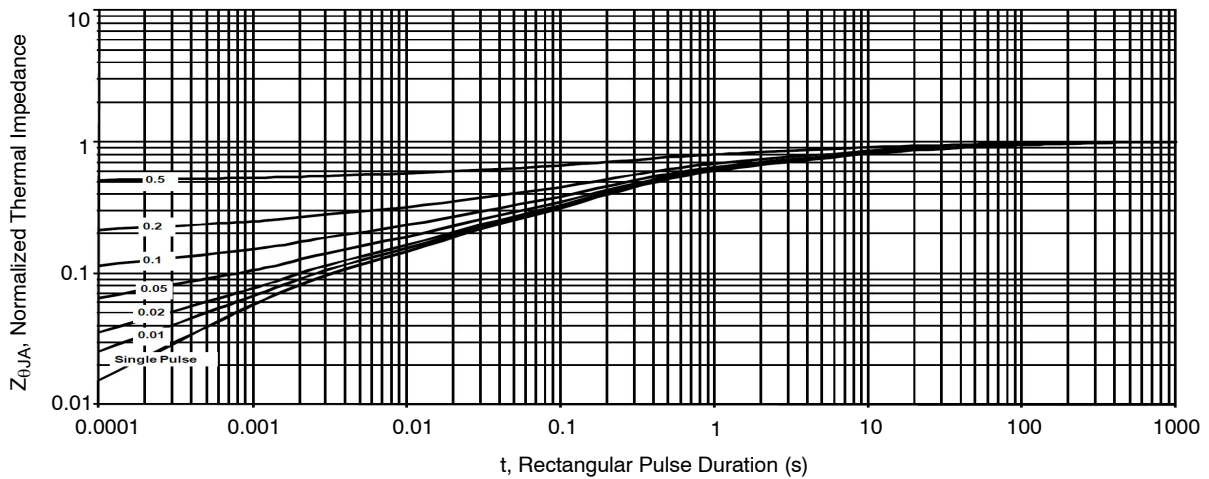


Figure 11. Transient Thermal Response Curve

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SOT-23 (TO-236)
CASE 318-08
ISSUE AS

DATE 30 JAN 2018

SCALE 4:1

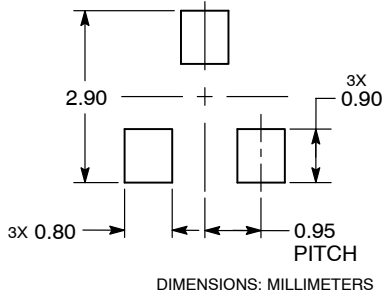


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

RECOMMENDED SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

- | | | | |
|---|---|---|--|
| STYLE 1 THRU 5:
CANCELLED | STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR | STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE |
| STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE | STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE | STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE |
| STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE | STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE | STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE | STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE |
| STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE | STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE | STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE-ANODE | STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE |
| STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN | STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT | STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE |
| STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE | STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION | STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE | STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE |

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