

TIP35A, TIP35B, TIP35C (NPN); TIP36A, TIP36B, TIP36C (PNP)

Complementary Silicon High-Power Transistors

Designed for general-purpose power amplifier and switching applications.

Features

- 25 A Collector Current
- Low Leakage Current –
 $I_{CEO} = 1.0 \text{ mA @ } 30 \text{ and } 60 \text{ V}$
- Excellent DC Gain –
 $h_{FE} = 40 \text{ Typ @ } 15 \text{ A}$
- High Current Gain Bandwidth Product –
 $|h_{fe}| = 3.0 \text{ min @ } I_C$
 $= 1.0 \text{ A, } f = 1.0 \text{ MHz}$
- These are Pb-Free Devices*

MAXIMUM RATINGS

Rating	Symbol	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
Collector – Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector – Base Voltage	V_{CB}	60	80	100	Vdc
Emitter – Base Voltage	V_{EB}	5.0			Vdc
Collector Current	I_C				Adc
– Continuous		25			
– Peak (Note 1)		40			
Base Current – Continuous	I_B	5.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	125			W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			$^\circ\text{C}$
Unclamped Inductive Load	E_{SB}	90			mJ

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Junction-to-Free-Air Thermal Resistance	$R_{\theta JA}$	35.7	$^\circ\text{C/W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 10 ms, Duty Cycle \leq 10%.

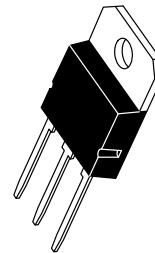
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



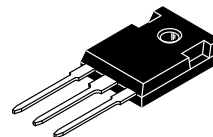
ON Semiconductor®

<http://onsemi.com>

25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–100 VOLTS, 125 WATTS



SOT-93 (TO-218)
CASE 340D
STYLE 1



TO-247
CASE 340L
STYLE 3

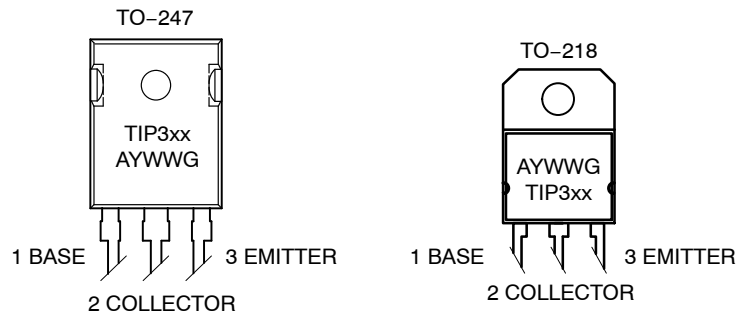
NOTE: Effective June 2012 this device will be available only in the TO-247 package. Reference FPCN# 16827.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

TIP35A, TIP35B, TIP35C (NPN); TIP36A, TIP36B, TIP36C (PNP)

MARKING DIAGRAMS



TIP3xx = Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
TIP35AG	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP35BG	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP35CG	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP36AG	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP36BG	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP36CG	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP35AG	TO-247 (Pb-Free)	30 Units / Rail
TIP35BG	TO-247 (Pb-Free)	30 Units / Rail
TIP35CG	TO-247 (Pb-Free)	30 Units / Rail
TIP36AG	TO-247 (Pb-Free)	30 Units / Rail
TIP36BG	TO-247 (Pb-Free)	30 Units / Rail
TIP36CG	TO-247 (Pb-Free)	30 Units / Rail

TIP35A, TIP35B, TIP35C (NPN); TIP36A, TIP36B, TIP36C (PNP)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (Note 2) ($I_C = 30\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	60 80 100	– – –	Vdc
Collector–Emitter Cutoff Current ($V_{CE} = 30\text{ V}$, $I_B = 0$) ($V_{CE} = 60\text{ V}$, $I_B = 0$)	I_{CEO}	– –	1.0 1.0	mA
Collector–Emitter Cutoff Current ($V_{CE} = \text{Rated } V_{CEO}$, $V_{EB} = 0$)	I_{CES}	–	0.7	mA
Emitter–Base Cutoff Current ($V_{EB} = 5.0\text{ V}$, $I_C = 0$)	I_{EBO}	–	1.0	mA
ON CHARACTERISTICS (Note 2)				
DC Current Gain ($I_C = 1.5\text{ A}$, $V_{CE} = 4.0\text{ V}$) ($I_C = 15\text{ A}$, $V_{CE} = 4.0\text{ V}$)	h_{FE}	25 15	– 75	–
Collector–Emitter Saturation Voltage ($I_C = 15\text{ A}$, $I_B = 1.5\text{ A}$) ($I_C = 25\text{ A}$, $I_B = 5.0\text{ A}$)	$V_{CE(sat)}$	– –	1.8 4.0	Vdc
Base–Emitter On Voltage ($I_C = 15\text{ A}$, $V_{CE} = 4.0\text{ V}$) ($I_C = 25\text{ A}$, $V_{CE} = 4.0\text{ V}$)	$V_{BE(on)}$	– –	2.0 4.0	Vdc
DYNAMIC CHARACTERISTICS				
Small–Signal Current Gain ($I_C = 1.0\text{ A}$, $V_{CE} = 10\text{ V}$, $f = 1.0\text{ kHz}$)	h_{fe}	25	–	–
Current–Gain — Bandwidth Product ($I_C = 1.0\text{ A}$, $V_{CE} = 10\text{ V}$, $f = 1.0\text{ MHz}$)	f_T	3.0	–	MHz

2. Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

TIP35A, TIP35B, TIP35C (NPN); TIP36A, TIP36B, TIP36C (PNP)

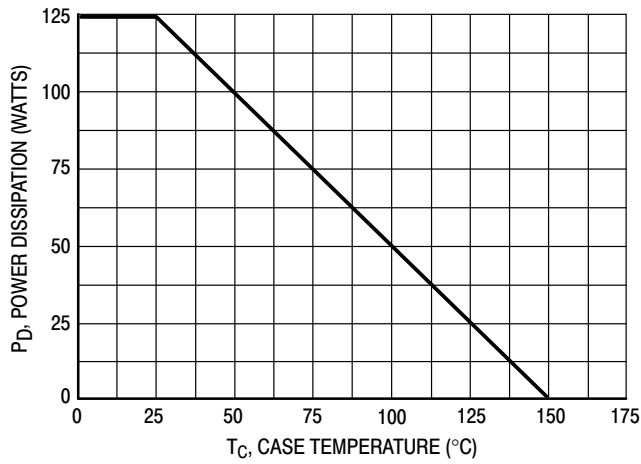


Figure 1. Power Derating



FOR CURVES OF FIGURES 3 & 4, R_B & R_L ARE VARIED.
 INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
 FOR NPN, REVERSE ALL POLARITIES.

Figure 2. Switching Time Equivalent Test Circuits



Figure 3. Turn-On Time

TIP35A, TIP35B, TIP35C (NPN); TIP36A, TIP36B, TIP36C (PNP)

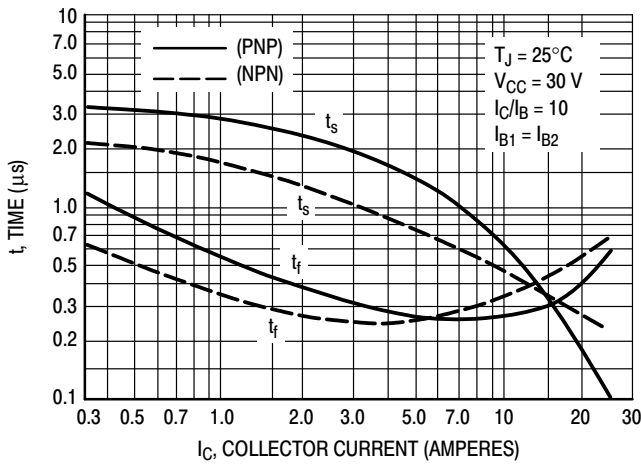


Figure 4. Turn-Off Time

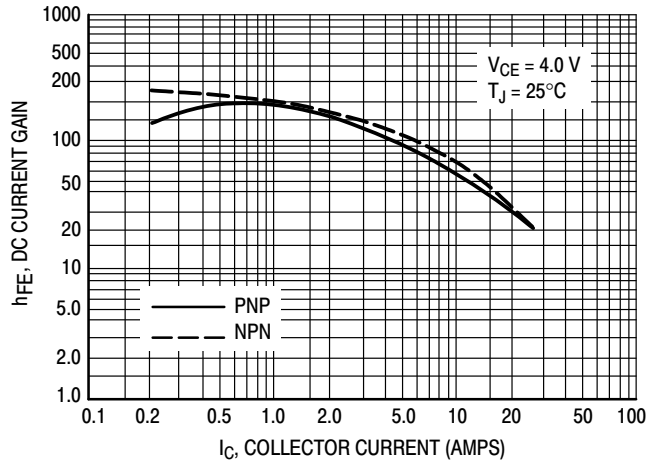


Figure 5. DC Current Gain

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

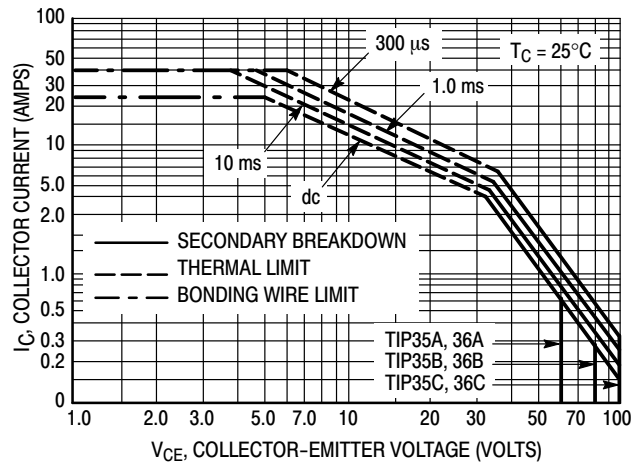


Figure 6. Maximum Rated Forward Bias Safe Operating Area

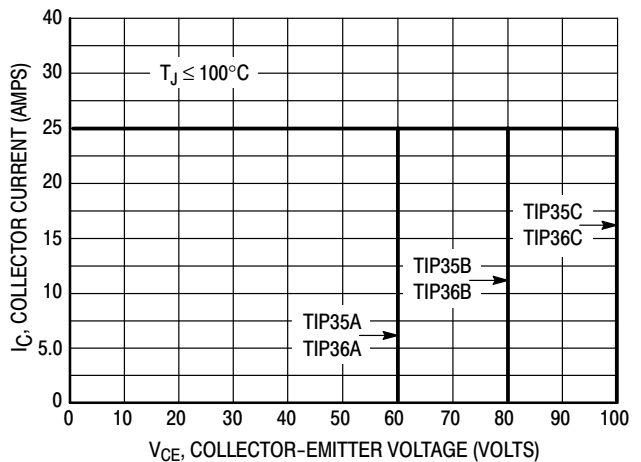


Figure 7. Maximum Rated Forward Bias Safe Operating Area

TIP35A, TIP35B, TIP35C (NPN); TIP36A, TIP36B, TIP36C (PNP)

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



NOTES:

- A. L1 and L2 are 10 mH, 0.11 Ω , Chicago Standard Transformer Corporation C-2688, or equivalent.
- B. Input pulse width is increased until $I_{CM} = -3.0$ A.
- C. For NPN, reverse all polarities.

Figure 8. Inductive Load Switching

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SOT-93 (TO-218) CASE 340D-02 ISSUE E

DATE 01/03/2002



SCALE 1:1



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
xxxxx = Device Code

DOCUMENT NUMBER:	98ASB42643B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-93	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TO-247
CASE 340L
ISSUE G

DATE 06 OCT 2021

SCALE 1:1

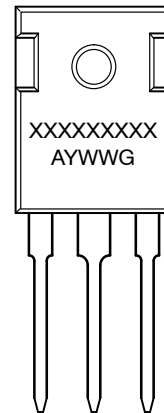


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER

DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	20.32	21.08	0.800	0.830
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	----	4.50	----	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

GENERIC
MARKING DIAGRAM*



- | | | | |
|--|--|--|--|
| <p>STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)</p> | <p>STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> |
| <p>STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> | <p>STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2</p> | | |

- XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB15080C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-247	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative