

FDMC8878

N-Channel POWERTRENCH[®] MOSFET 30 V, 16.5 A, 14 mΩ

This N-Channel MOSFET is a rugged gate version of ON Semiconductor's advanced PowerTrench process. It has been optimized for power management applications.

Features

- $R_{DS(on)} = 14 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 9.6 \text{ A}$
- $R_{DS(on)} = 17 \text{ m}\Omega$ (Max.) @ $V_{GS} = 4.5 \text{ V}$, $I_D = 8.7 \text{ A}$
- Low Profile – 0.8 mm Max in MLP 3.3 x 3.3
- These Devices are Pb-Free and are RoHS Compliant

Application

- DC – DC Conversion

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DS}	30	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$ (Package limited)	16.5	A
		$T_C = 25^\circ\text{C}$ (Silicon limited)	38	
		$T_A = 25^\circ\text{C}$ (Figure 1)	9.6	
Drain Current	Pulsed	I_D	60	A
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	31	W
			$T_A = 25^\circ\text{C}$ (Figure 1)	
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Figure 1)	$R_{\theta JA}$	60	

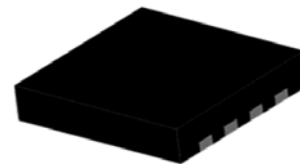
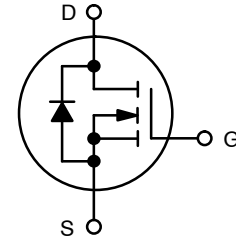
PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Quantity
FDMC8878	FDMC8878	MLP 3.3 x 3.3	13"	12 mm	3000 units

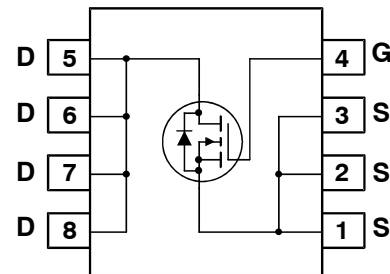


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WDFN8
CASE 511DH



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 1 of this data sheet.

FDMC8878

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	30	-	-	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	20	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 125°C	-	-	100	
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = V _{DS}	1	1.7	3	V
ΔBV _{DSS} /ΔT _J	Gate-to-Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	-5.7	-	mV/°C
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 9.6 A	-	9.6	14.0	mΩ
		V _{GS} = 4.5 V, I _D = 8.7 A	-	12.1	17.0	
		V _{GS} = 10 V, I _D = 9.6 A, T _J = 125°C	-	13.5	20.0	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 9.6 A	-	35	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	1000	1230	pF
C _{oss}	Output Capacitance		-	183	255	pF
C _{rss}	Reverse Transfer Capacitance		-	118	180	pF
R _g	Reverse Transfer Capacitance	f = 1 MHz	-	1.1	-	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 9.6 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	-	8	16	ns
t _r	Rise Time		-	4	10	
t _{d(off)}	Turn-Off Delay Time		-	20	36	
t _f	Fall Time		-	3	10	
Q _{g(tot)}	Total Gate Charge	V _{GS} = 10 V, V _{DD} = 15 V, I _D = 9.6 A	-	18	26	nC
Q _{gs}	Gate-to-Source Gate Charge		-	2.8	-	
Q _{gd}	Gate-to-Drain "Miller" Charge		-	3.9	-	

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source-to-Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 9.6 A (Note 2)	-	0.8	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 9.6 A, di/dt = 100 A/μs	-	23	35	ns
Q _{rr}	Reverse Recovery Charge		-	14	21	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

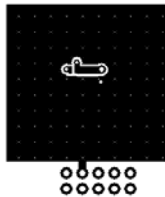


Figure 1.

a. 60°C/W when mounted on a 1 in² pad of 2 oz copper



Figure 2.

b. 135°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

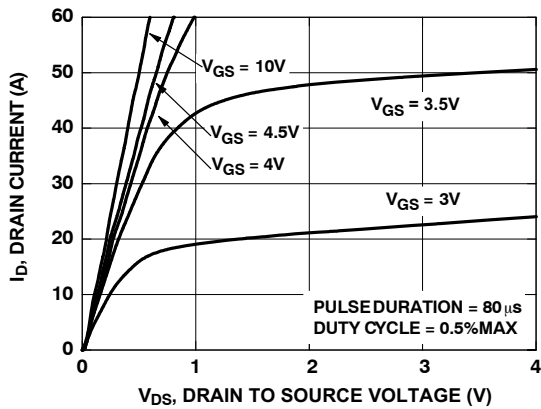


Figure 3. Gate Charge Characteristics

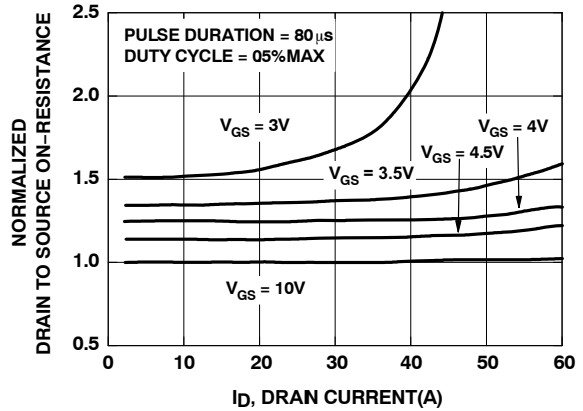


Figure 4. Capacitance vs. Drain to Source Voltage

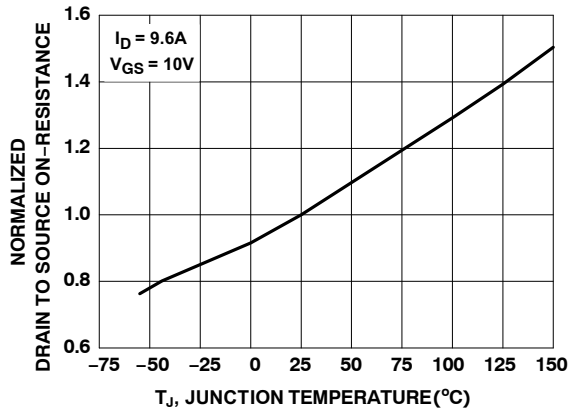


Figure 5. Unclamped Inductive Switching Capability

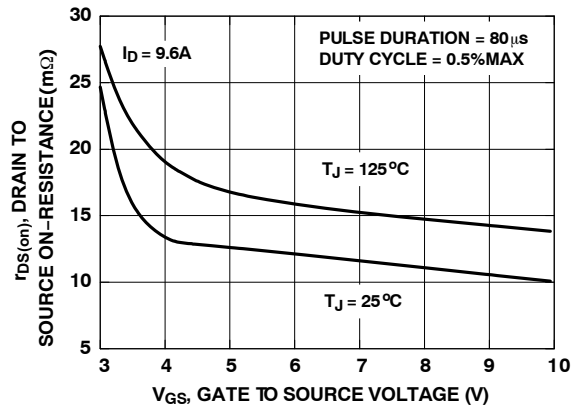


Figure 6. Maximum Continuous Drain Current vs. Ambient Temperature

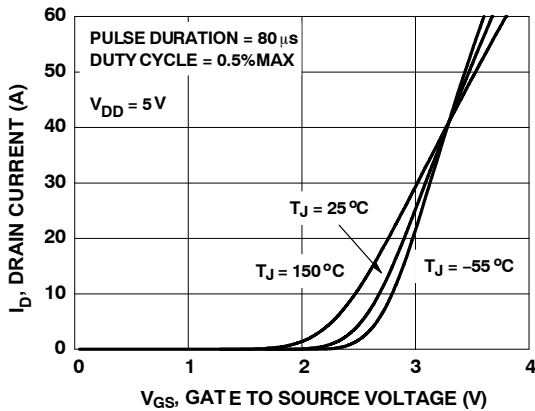


Figure 7. Forward Bias Safe Operating Area

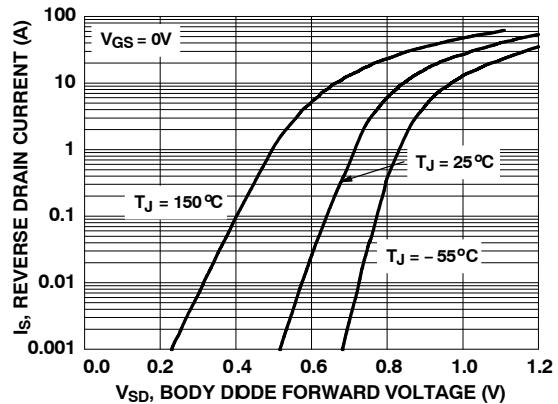


Figure 8. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

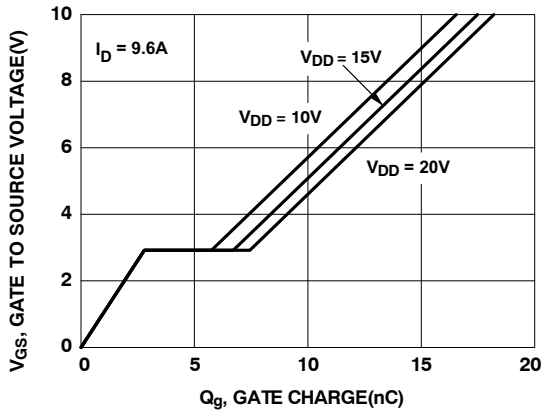


Figure 9. On-Region Characteristics

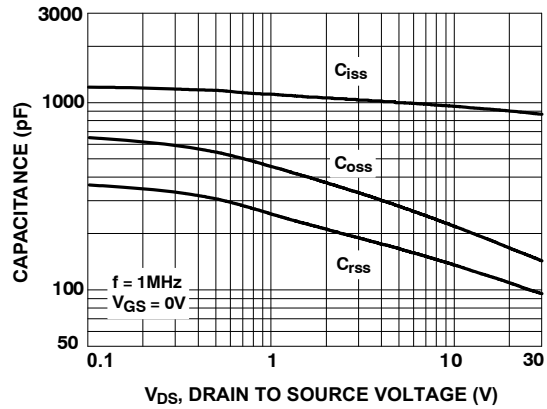


Figure 10. Transfer Characteristics

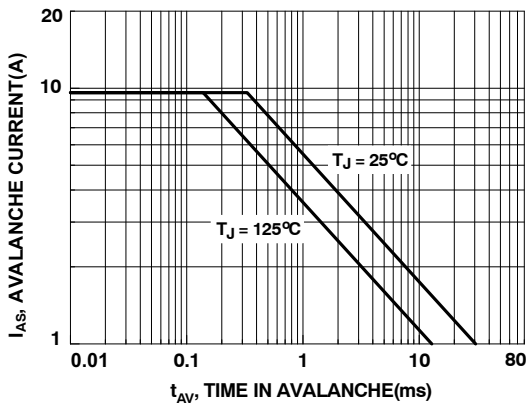


Figure 11. On-Resistance Variation vs. Drain Current and Gate Voltage

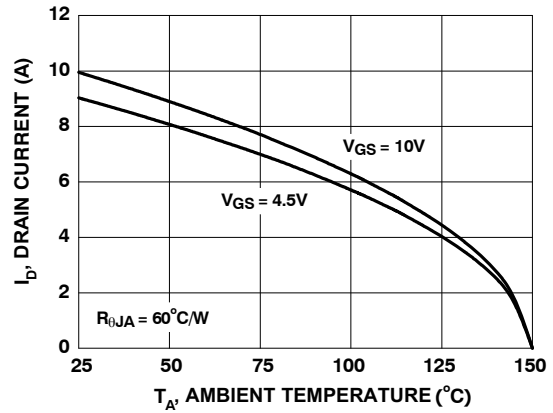


Figure 12. Body Diode Forward Voltage Variation vs. Source Current and Temperature

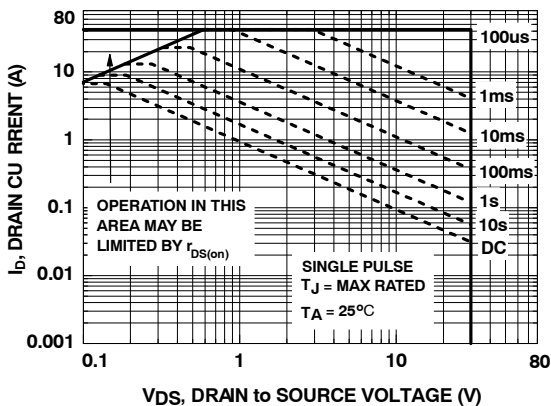


Figure 13. Capacitance Characteristics

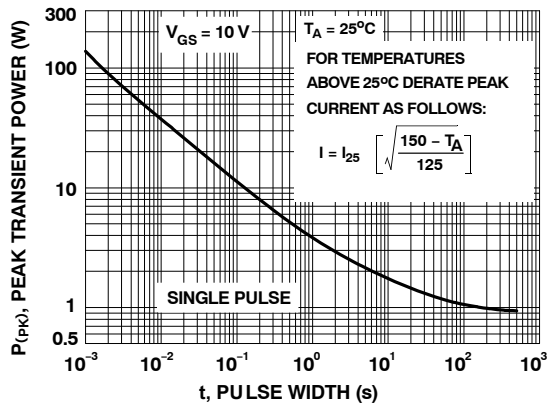


Figure 14. Gate Charge Characteristics

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

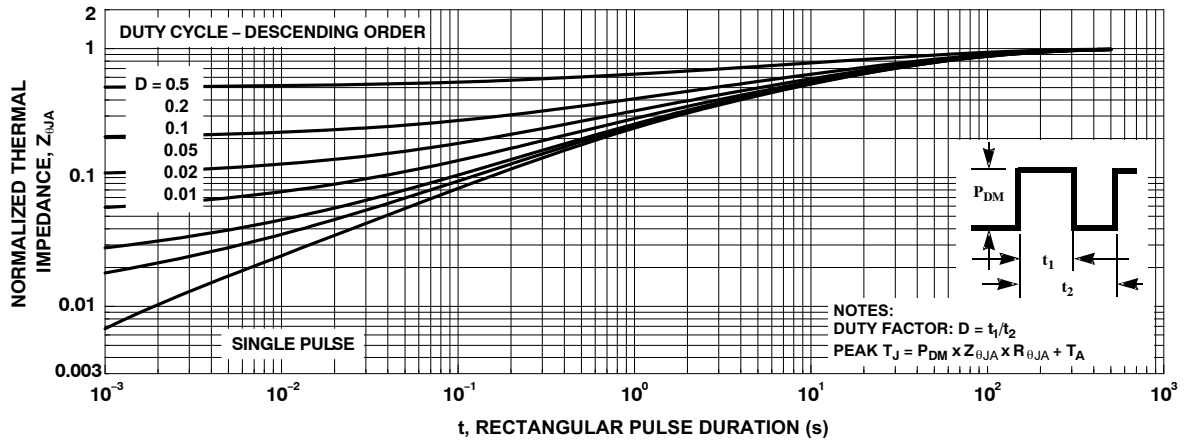


Figure 15. Transient Thermal Response Curve

MECHANICAL CASE OUTLINE

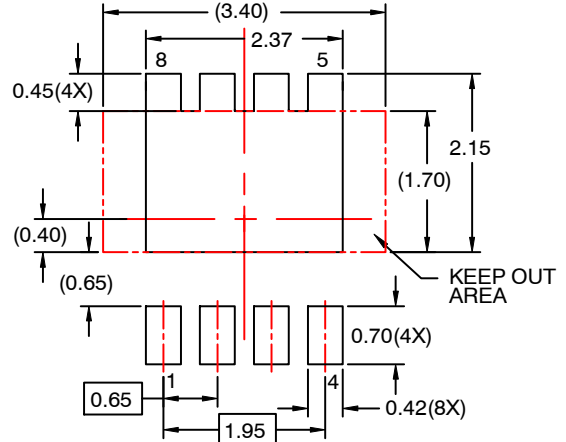
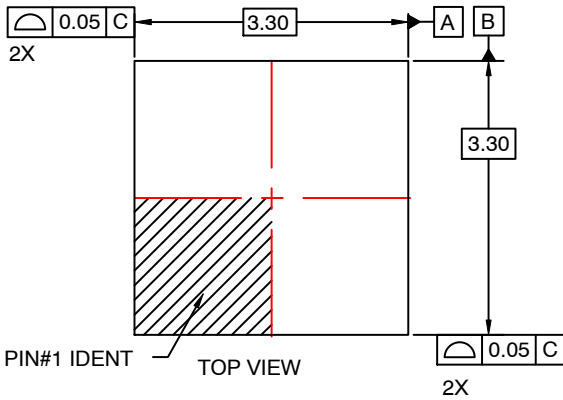
PACKAGE DIMENSIONS

ON Semiconductor®

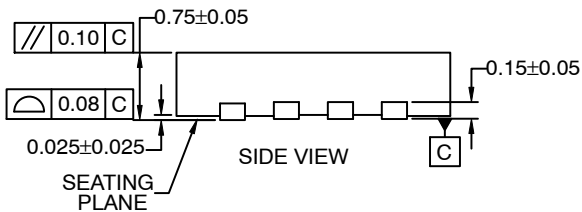


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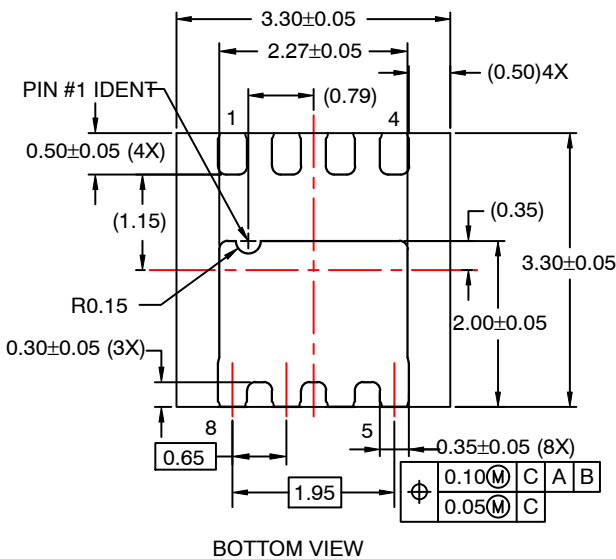


RECOMMENDED LAND PATTERN



NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW

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