MOSFET – Power, Single, P-Channel, SC-70 -30 V, -1.3 A

Features

- -30 V BV_{ds}, Low R_{DS(on)} in SC-70 Package
- Low Threshold Voltage
- Fast Switching Speed
- This is a Halide-Free Device
- This is a Pb-Free Device

Applications

- Load Switch
- Low Current Inverter and DC-DC Converters
- Power Switch for Printers, Communication Equipment

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Paramo	Symbol	Value	Unit			
Drain-to-Source Voltage	V_{DSS}	-30	V			
Gate-to-Source Voltage			V _{GS}	±12	V	
Continuous Drain Steady		T _A = 25°C		-1.2		
Current (Note 1)	State	T _A = 85°C	I _D	-0.80	Α	
	t ≤ 5 s			-1.3		
Power Dissipation				0.29		
(Note 1)	State T	$T_A = 25^{\circ}C$	P_{D}		W	
	t ≤ 5 s			0.35		
Pulsed Drain Current	Pulsed Drain Current $t_p = 10 \mu s$			-5.0	Α	
Operating Junction and S	T _J ,	-55 to	°C			
	T _{stg}	150				
Source Current (Body Diode)			Is	-1.0	Α	
Lead Temperature for Sol (1/8" from case for 10 s)	TL	260	°C			

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	425	°C/W
Junction-to-Ambient - t ≤ 5 s (Note 1)	$R_{\theta JA}$	360	

Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)

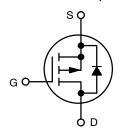


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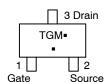
V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
-30 V	150 mΩ @ –10 V	-1.2 A
	200 mΩ @ -4.5 V	-1.0 A
	280 mΩ @ -2.5 V	-0.9 A

SC-70/SOT-323 (3 LEADS)





2 SC-70/SOT-323 CASE 419 STYLE 8



MARKING DIAGRAM/ PIN ASSIGNMENT

TG = Specific Device Code

M = Date Code*

■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTS4173PT1G	SC-70 (Pb-Free)	3000/Tape & Reel

- †For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
- * Date code orientation may vary depending upon manufacturing location

$\textbf{MOSFET ELECTRICAL CHARACTERISTICS} \ (T_J = 25^{\circ}\text{C unless otherwise noted})$

Parameter Sym		Test Condition	Min	Тур	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 \text{ V}, V_{DS} = -24 \text{ V}, T_J = 25^{\circ}\text{C}$ $V_{GS} = 0 \text{ V}, V_{DS} = -24 \text{ V}, T_J = 85^{\circ}\text{C}$			-1.0 -5.0	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			±0.1	μΑ
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-0.7	-1.15	-1.5	V
Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = −10 V, I _D = −1.2 A		90	150	mΩ
		$V_{GS} = -4.5 \text{ V}, I_D = -1.0 \text{ A}$		110	200	
		$V_{GS} = -2.5 \text{ V}, I_D = -0.9 \text{ A}$		165	280	
Forward Transconductance	9FS	$V_{DS} = -5 \text{ V}, I_D = -1.2 \text{ A}$		3.6		S
CHARGES, CAPACITANCES AND GA	ATE RESISTA	NCE				
Input Capacitance	C _{iss}			430		pF
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = -15 \text{ V}$		55		1
Reverse Transfer Capacitance	C _{rss}			40		
Total Gate Charge	Q _{G(TOT)}			4.8		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = -4.5 V, V _{DS} = -15 V,		0.6		
Gate-to-Source Charge	Q _{GS}	I _D = -1.2 A		1.1		
Gate-to-Drain Charge	Q_{GD}			1.5		
Total Gate Charge	Q _{G(TOT)}			10.1		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = -10 V, V _{DS} = -15 V,		0.6		
Gate-to-Source Charge	Q_{GS}	$I_D = -1.2 A$		1.1		
Gate-to-Drain Charge	Q_{GD}			1.5		
SWITCHING CHARACTERISTICS (No	ote 4)		•			•
Turn-On Delay Time	t _{d(on)}			7.7		ns
Rise Time	t _r	V _{GS} = -4.5 V, V _{DS} = -15 V,		5.2		1
Turn-Off Delay Time	t _{d(off)}	$I_D = -1.2 \text{ A}, R_G = 3 \Omega$		16.2		
Fall Time	t _f			6.7		1
Turn-On Delay Time	t _{d(on)}			5.3		ns
Rise Time	t _r	V _{GS} = -10 V, V _{DS} = -15 V,		6.7		
Turn-Off Delay Time	t _{d(off)}	$I_D = -1.2 \text{ A}, R_G = 3 \Omega$		19.9		1
Fall Time	t _f			7.1		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS		-	-	-	-
Forward Diode Voltage	V _{SD}	$V_{GS} = 0 \text{ V}, I_S = -1.0 \text{ A}$		-0.8	-1.0	V
Reverse Recovery Time	t _{RR}			12		ns
Charge Time	t _a	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, I_{S} = -1.0 \text{ A},$		10		1
Discharge Time	t _b	$dl_{SD}/d_t = 100 \text{ A/}\mu\text{s}$		2.0		1
Reverse Recovery Charge	Q _{RR}	1		7.0		nC

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
 Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%
 Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

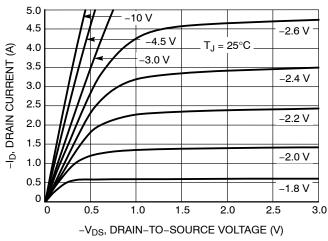


Figure 1. On-Region Characteristics

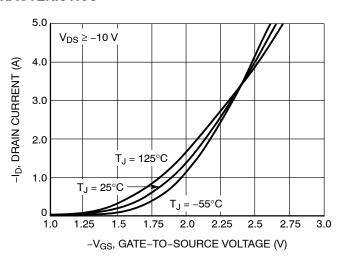


Figure 2. Transfer Characteristics

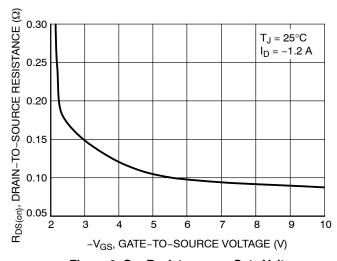


Figure 3. On-Resistance vs. Gate Voltage

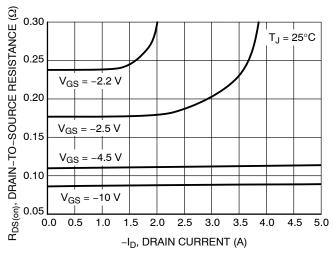


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

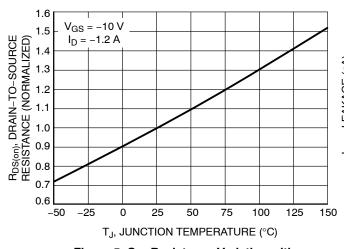


Figure 5. On–Resistance Variation with Temperature

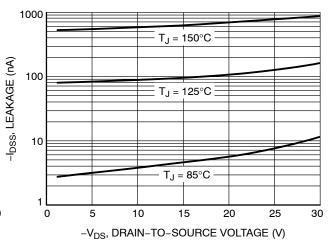


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

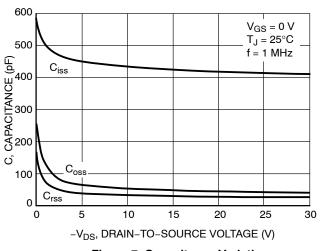


Figure 7. Capacitance Variation

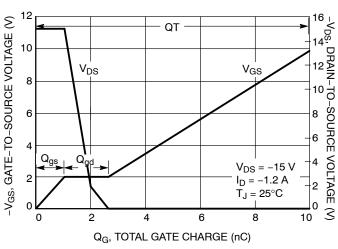


Figure 8. Gate-to-Source Voltage vs. Total Charge

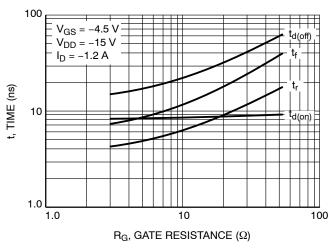


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

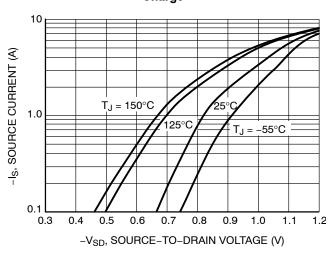


Figure 10. Diode Forward Voltage vs. Current

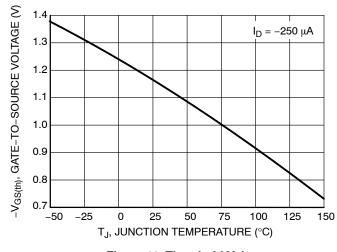


Figure 11. Threshold Voltage

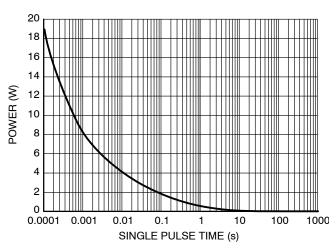


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CURVES

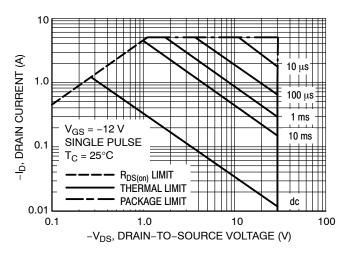


Figure 13. Maximum Rated Forward Biased Safe Operating Area

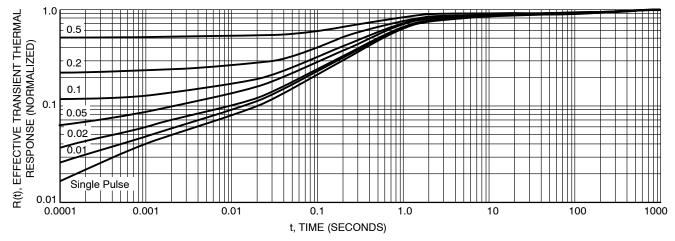


Figure 14. FET Thermal Response





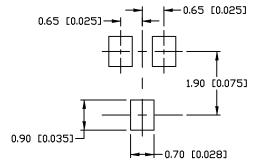
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DATE 07 OCT 2021

NOTES:

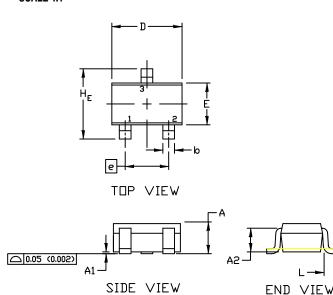
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH

	MILLIMETERS			INCHES		
DIM	MIN.	N□M.	MAX.	MIN.	N□M.	MAX.
Α	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF				0.028 BS	C
b	0.30	0.35	0.40	0.012	0.014	0.016
С	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
Ε	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC				0.026 BS	C
L	0.20	0.38	0.56	0.008	0.015	0.022
HE	2.00	2.10	2.40	0.079	0.083	0.095



For additional information on our Pb-Free strategy and soldering details, please download the IIN Semiconductor Soldering and Mounting Techniques Reference Manual, SILDERRM/D.

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM



XX = Specific Device Code

M = Date Code

■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: CANCELLED	STYLE 2: PIN 1. ANODE 2. N.C. 3. CATHODE	STYLE 3: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. CATHODE	
STYLE 6:	STYLE 7:	STYLE 8:	STYLE 9:	STYLE 10:	STYLE 11:
PIN 1. EMITTER	PIN 1. BASE	PIN 1. GATE	PIN 1. ANODE	PIN 1. CATHODE	PIN 1. CATHODE
2. BASE	2. EMITTER	2. SOURCE	2. CATHODE	2. ANODE	2. CATHODE
3. COLLECTOR	3. COLLECTOR	3. DRAIN	3. CATHODE-ANODE	3. ANODE-CATHODE	3. CATHODE

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