NCP5392Q

2/3/4-Phase Controller for CPU Applications

The NCP5392Q provides up to a four-phase buck solution which combines differential voltage sensing, differential phase current sensing, and adaptive voltage positioning to provide accurately regulated power for Intel processors. Dual-edge pulse-width modulation (PWM) combined with inductor current sensing reduces system cost by providing the fastest initial response to dynamic load events. Dual-edge multiphase modulation reduces the total bulk and ceramic output capacitance required to meet transient regulation specifications.

A high performance operational error amplifier is provided to simplify compensation of the system. Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed-loop transient response and Dynamic VID performance.

In addition, NCP5392Q provides an automatic power saving feature (Auto-PSI). When Auto-PSI function is enabled, NCP5392Q will automatically detect the VID transitions and direct the Vcore regulator in or out of low power states. As a result, the best efficiency scheme is always chosen.

Features

- Meets Intel's VR11.1 Specifications
- Dual-edge PWM for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Internal Soft Start
- Dynamic Reference Injection
- DAC Range from 0.375 V to 1.6 V
- DAC Feed Forward Function
- ±0.5% DAC Voltage Accuracy from 1.0 V to 1.6 V
- True Differential Remote Voltage Sensing Amplifier
- Phase-to-Phase Current Balancing
- "Lossless" Differential Inductor Current Sensing
- Differential Current Sense Amplifiers for each Phase
- Adaptive Voltage Positioning (AVP)
- Oscillator Frequency Range of 100 kHz – 1 MHz
- Latched Over Voltage Protection (OVP)
- Guaranteed Startup into Pre-Charged Loads
- Threshold Sensitive Enable Pin for VTT Sensing
- Power Good Output with Internal Delays
- Thermally Compensated Current Monitoring
- Automatic Power Saving (AUTO PSI Mode)
- Compatible to PSI Power Saving Requirements
- This is a Pb-Free Device

Applications

- Desktop Processors

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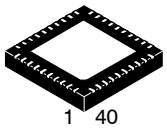
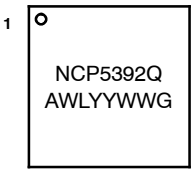
http://onsemi.com



40 PIN QFN, 6x6
MN SUFFIX
CASE 488AR

MARKING DIAGRAM



NCP5392Q = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*Pin 41 is the thermal pad on the bottom of the device.

ORDERING INFORMATION

Device	Package	Shipping†
NCP5392QMNR2G*	QFN-40 (Pb-Free)	2500/Tape & Reel

*Temperature Range: 0°C to 85°C

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN CONNECTIONS

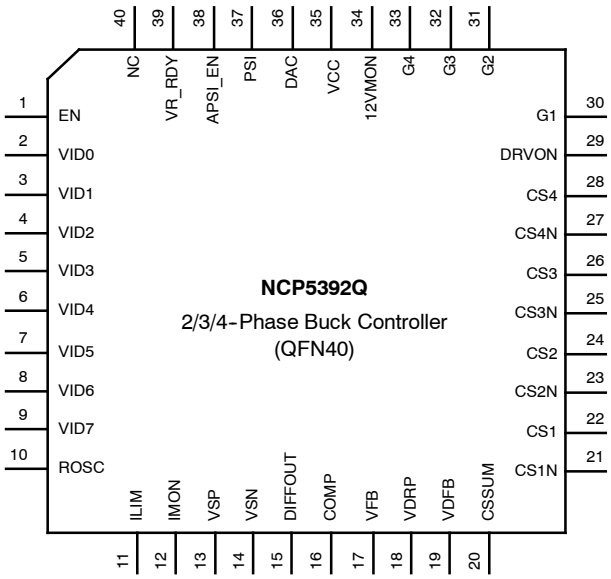


Figure 1. NCP5392Q QFN40 Pin Connections (Top View)

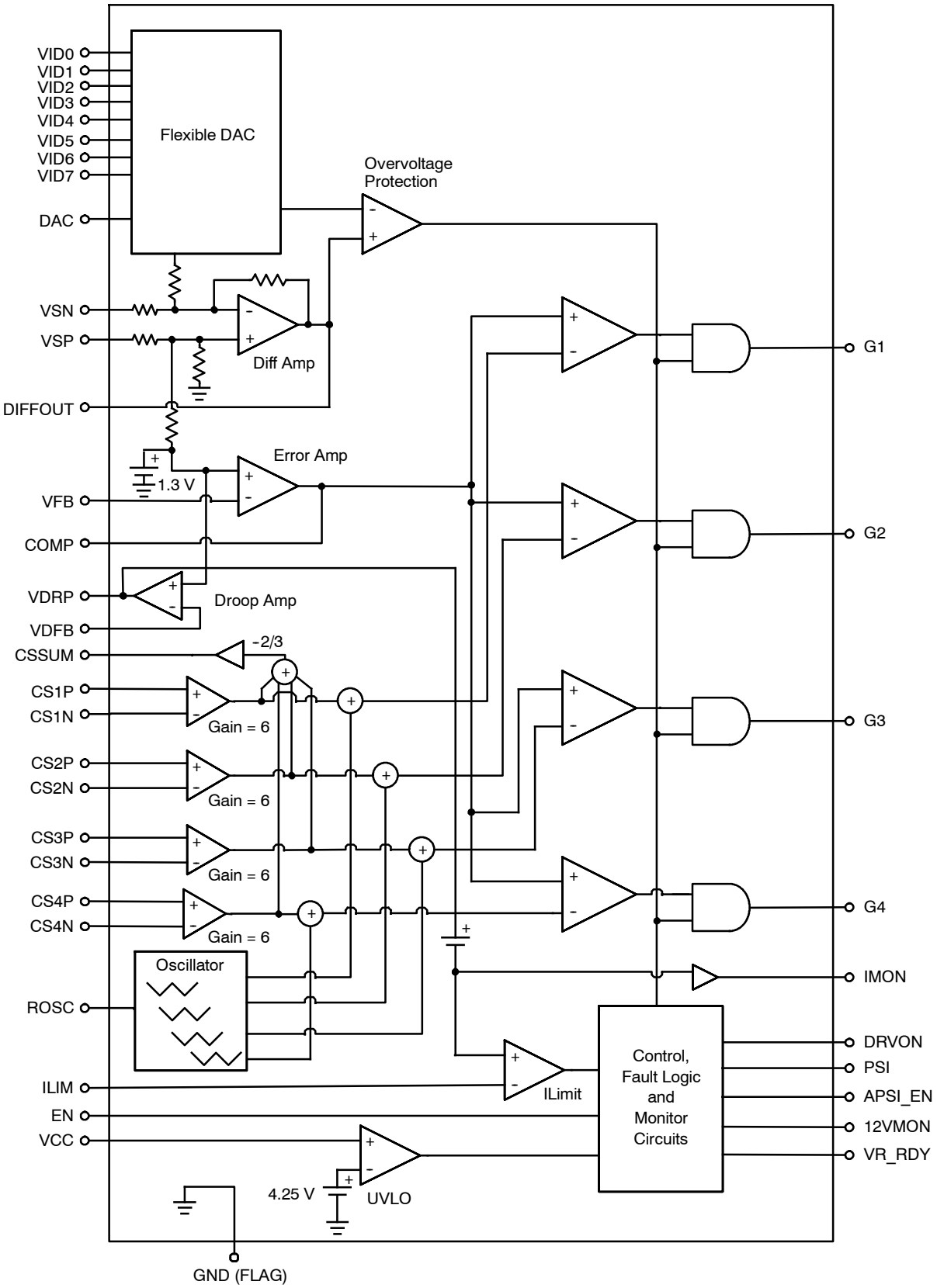


Figure 2. NCP5392Q Block Diagram

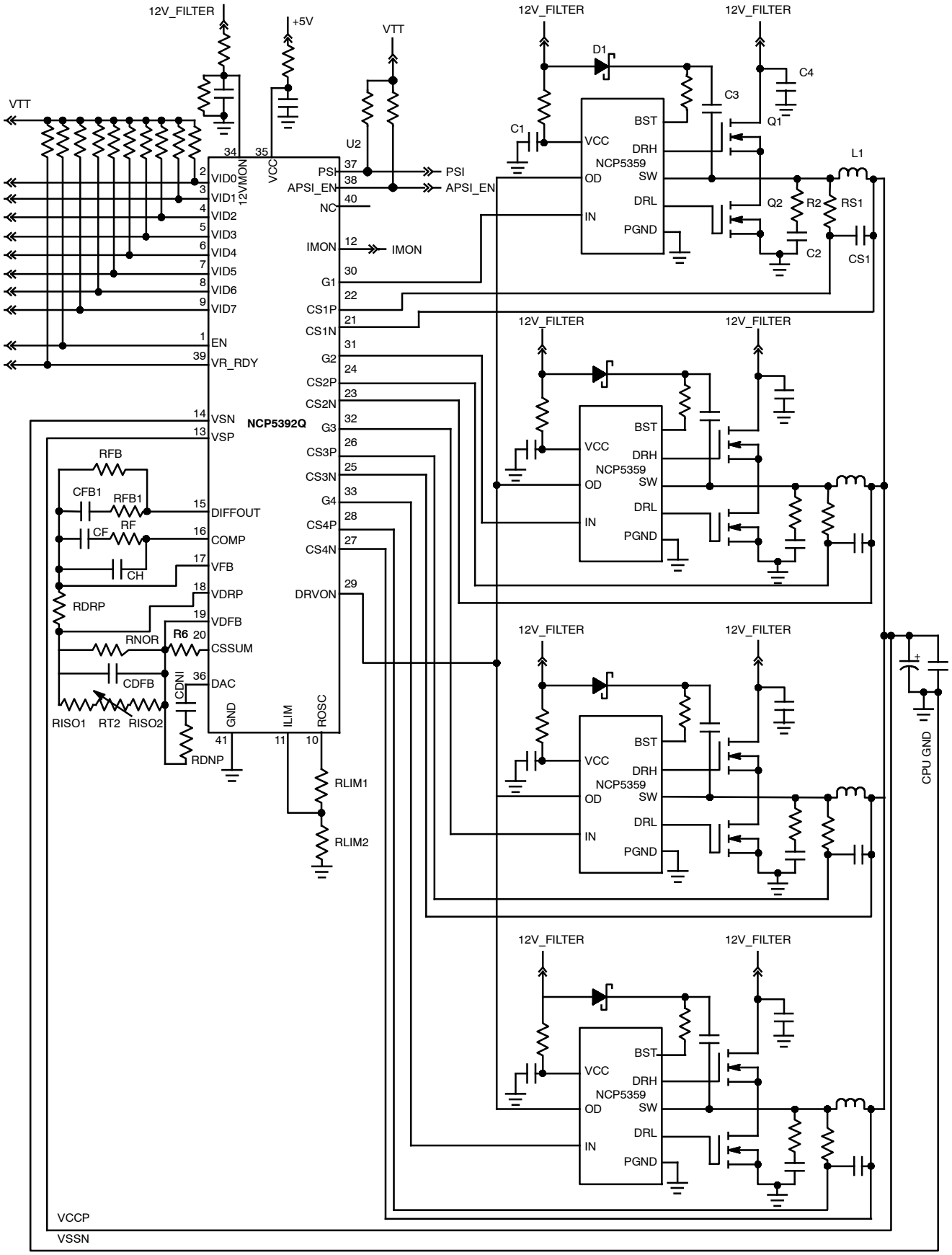


Figure 3. Application Schematic for Four Phases

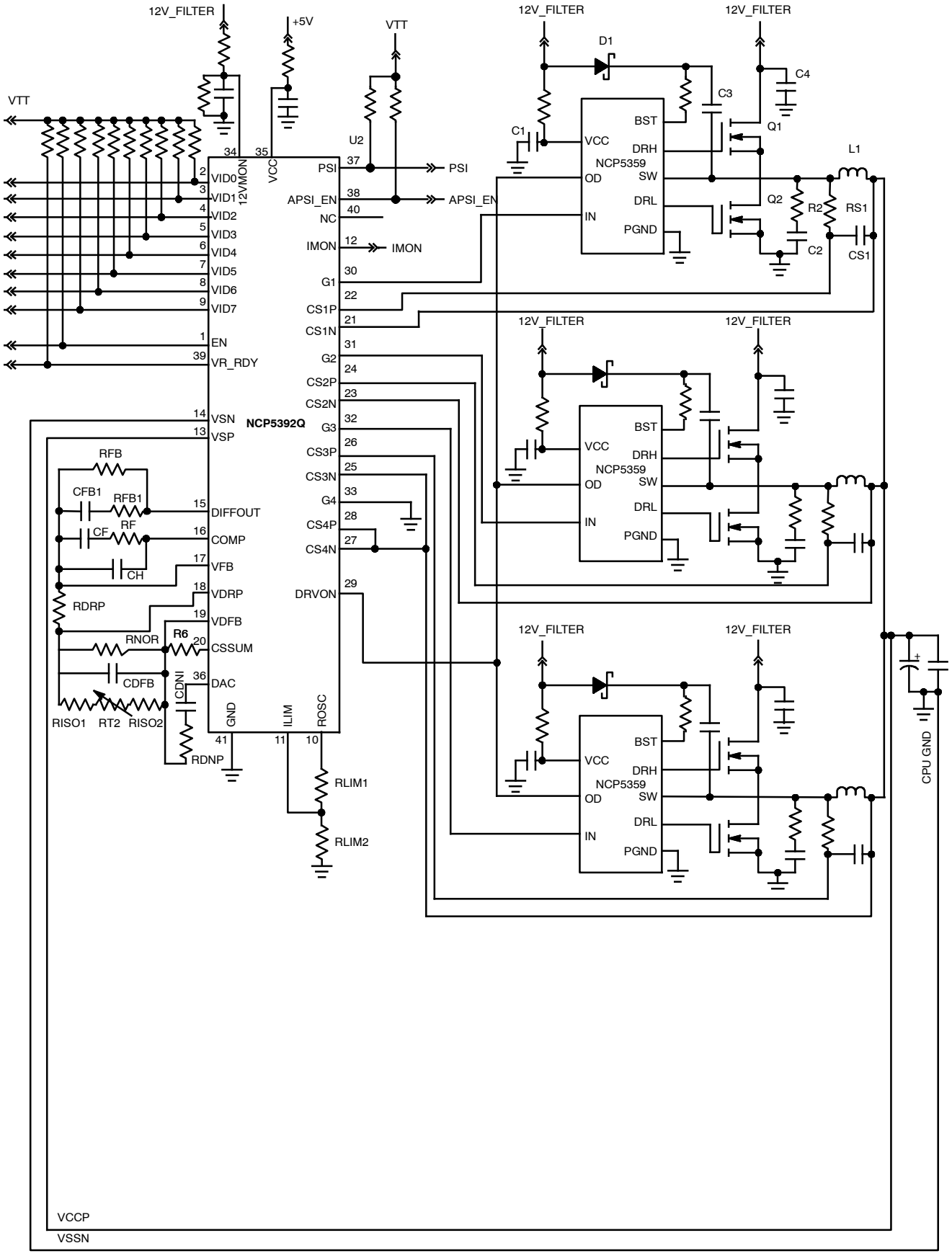


Figure 4. Application Schematic for Three Phases

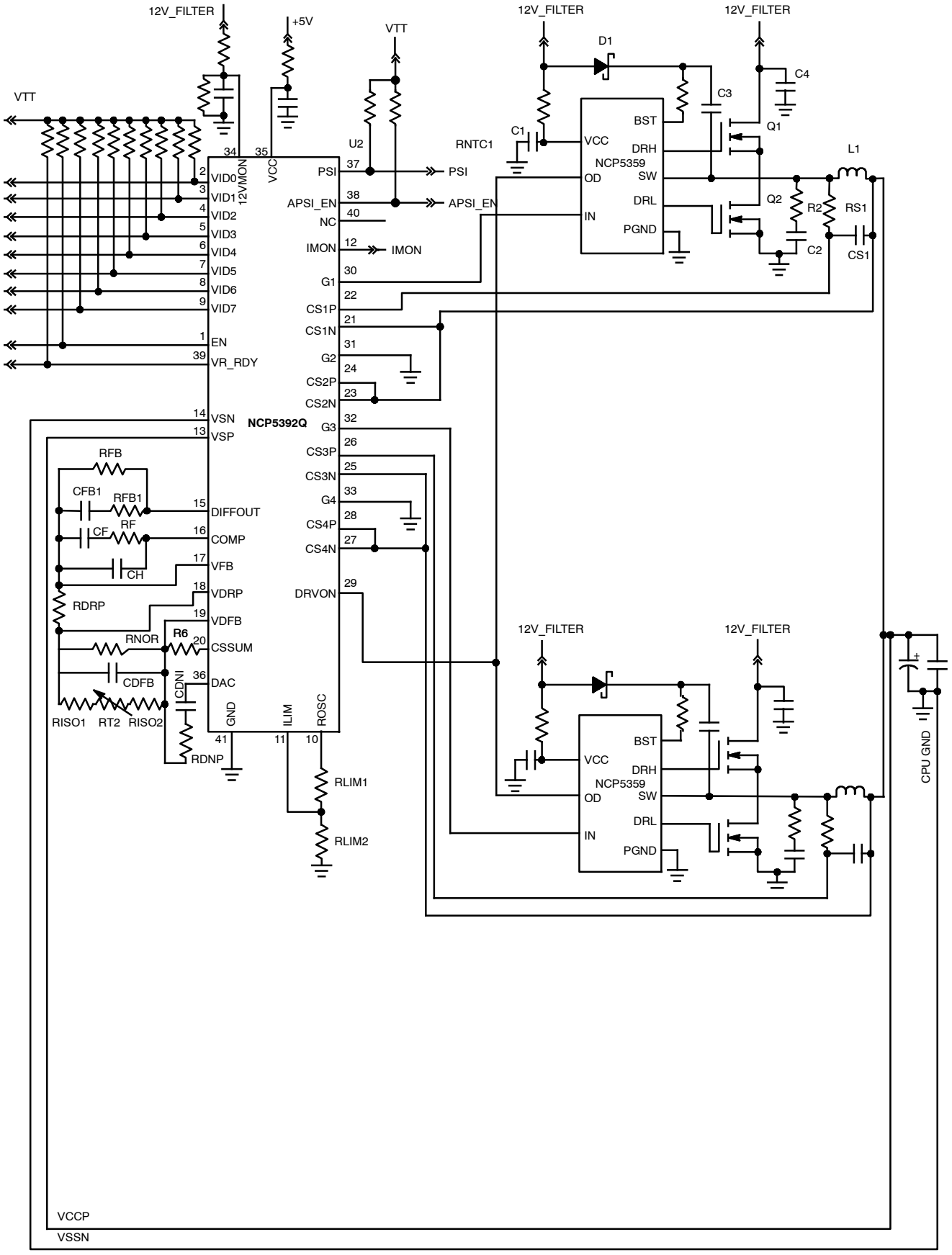


Figure 5. Application Schematic for Two Phases

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	EN	Threshold sensitive input. High = startup, Low = shutdown.
2	VID0	Voltage ID DAC input
3	VID1	Voltage ID DAC input
4	VID2	Voltage ID DAC input
5	VID3	Voltage ID DAC input
6	VID4	Voltage ID DAC input
7	VID5	Voltage ID DAC input
8	VID6	Voltage ID DAC input
9	VID7	Voltage ID DAC input
10	ROSC	A resistance from this pin to ground programs the oscillator frequency according to f_{SW}. This pin supplies a trimmed output voltage of 2 V.
11	ILIM	Overcurrent shutdown threshold setting. Connect this pin to the ROSC pin via a resistor divider as shown in the Application Schematics. To disable the overcurrent feature, connect this pin directly to the ROSC pin. To guarantee correct operation, this pin should only be connected to the voltage generated by the ROSC pin; do not connect this pin to any externally generated voltages.
12	IMON	0 mV to 900 mV analog signal proportional to the output load current. VSN referenced
13	VSP	Non−inverting input to the internal differential remote sense amplifier
14	VSN	Inverting input to the internal differential remote sense amplifier
15	DIFFOUT	Output of the differential remote sense amplifier
16	COMP	Output of the error amplifier
17	VFB	Compensation Amplifier Voltage feedback
18	VDRP	Voltage output signal proportional to current used for current limit and output voltage droop
19	VDFB	Droop Amplifier Voltage Feedback
20	CSSUM	Inverted Sum of the Differential Current Sense inputs. Av=CSSUM/CSx = −4
21	CS1N	Inverting input to current sense amplifier #1
22	CS1	Non−inverting input to current sense amplifier #1
23	CS2N	Inverting input to current sense amplifier #2
24	CS2	Non−inverting input to current sense amplifier #2
25	CS3N	Inverting input to current sense amplifier #3
26	CS3	Non−inverting input to current sense amplifier #3
27	CS4N	Inverting input to current sense amplifier #4
28	CS4	Non−inverting input to current sense amplifier #4
29	DRVON	Bidirectional Gate Drive Enable
30	G1	PWM output pulse to gate driver. 3−level output: Low = LSFET Enabled, Mid = Diode Emulation Enabled, High = HSFET Enabled
31	G2	PWM output pulse to gate driver. 3−level output (see G1)
32	G3	PWM output pulse to gate driver. 3−level output (see G1)
33	G4	PWM output pulse to gate driver. 3−level output (see G1)
34	12VMON	Monitor a 12 V input through a resistor divider.
35	VCC	Power for the internal control circuits.
36	DAC	DAC Feed Forward Output
37	PSI	Power Saving Control. Low = power saving operation, High = normal operation. PSI signal has higher priority over APSI_EN signal.
38	APSI_EN	APSI_EN High: Enable AUTO PSI function. When PSI = low, system will be forced into PSI mode, unconditionally. When PSI = high, APSI_EN will determine if the system needs to be in AUTO PSI mode. Once in AUTO PSI mode, system switches on/off PSI functions automatically based on VID change status.
39	VR_RDY	Open collector output. High indicates that the output is regulating
40	NC	Not Connected
FLAG	GND	Power supply return (QFN Flag)

PIN CONNECTIONS VS. PHASE COUNT

Number of Phases	G4	G3	G2	G1	CS4−CS4N	CS3−CS3N	CS2−CS2N	CS1−CS1N
4	Phase 4 Out	Phase 3 Out	Phase 2 Out	Phase 1 Out	Phase 4 CS input	Phase 3 CS input	Phase 2 CS input	Phase 1 CS input
3	Tie to GND	Phase 3 Out	Phase 2 Out	Phase 1 Out	Tie to CSN pin used	Phase 3 CS input	Phase 2 CS input	Phase 1 CS input
2	Tie to GND	Phase 2 Out	Tie to GND	Phase 1 Out	Tie to CSN pin used	Phase 2 CS input	Tie to CSN pin used	Phase 1 CS input

MAXIMUM RATINGS

ELECTRICAL INFORMATION

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP	5.5 V	−0.3 V	10 mA	10 mA
V_{DRP}	5.5 V	−0.3 V	5 mA	5 mA
V−	GND + 300 mV	GND − 300 mV	1 mA	1 mA
DIFFOUT	5.5 V	−0.3 V	20 mA	20 mA
VR_RDY	5.5 V	−0.3 V	N/A	20 mA
VCC	7.0 V	−0.3 V	N/A	10 mA
ROSC	5.5 V	−0.3 V	1 mA	N/A
IMON Output	1.1 V			
All Other Pins	5.5 V	−0.3 V		

*All signals referenced to AGND unless otherwise noted.

THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Characteristic, QFN Package (Note 1)	$R_{\theta JA}$	34	°C/W
Operating Junction Temperature Range (Note 2)	T_J	0 to 125	°C
Operating Ambient Temperature Range	T_A	0 to +85	°C
Maximum Storage Temperature Range	T_{STG}	−55 to +150	°C
Moisture Sensitivity Level, QFN Package	MSL	1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*The maximum package power dissipation must be observed.

1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM.
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current (Note 3)		−200		200	nA
Noninverting Voltage Range (Note 3)		0	1.3	3	V
Input Offset Voltage (Note 3)	V+ = V− = 1.1 V	−1.0	−	1.0	mV
Open Loop DC Gain	C_L = 60 pF to GND, R_L = 10 KΩ to GND	−	100		dB
Open Loop Unity Gain Bandwidth	C_L = 60 pF to GND, R_L = 10 KΩ to GND	−	10	−	MHz
Open Loop Phase Margin	C_L = 60 pF to GND, R_L = 10 KΩ to GND	−	80	−	°
Slew Rate	ΔV_{in} = 100 mV, G = − 10 V/V, ΔV_{out} = 1.5 V − 2.5 V, C_L = 60 pF to GND, DC Load = ±125 μA to GND	−	5	−	V/μs
Maximum Output Voltage	I_{SOURCE} = 2.0 mA	3.5	−	−	V
Minimum Output Voltage	I_{SINK} = 0.2 mA	−	−	50	mV
Output source current (Note 3)	V_{out} = 3.5 V	2	−	−	mA
Output sink current (Note 3)	V_{out} = 1.0 V	2	−	−	mA
DIFFERENTIAL SUMMING AMPLIFIER					
VSN Input Bias Current	VSN Voltage = 0 V		30		μA
VSP Input Resistance	DRVON = Low DRVON = High		1.5 17		kΩ
VSP Input Bias Voltage	DRVON = Low DRVON = High		0.09 0.66		V
Input Voltage Range (Note 3)		−0.3	−	3.0	V
−3 dB Bandwidth	C_L = 80 pF to GND, R_L = 10 KΩ to GND	−	10	−	MHz
Closed Loop DC Gain VS to Diffout	VS+ to VS− = 0.5 to 1.6 V	0.98	1.0	1.025	V/V
Maximum Output Voltage	I_{SOURCE} = 2 mA	3.0	−	−	V
Minimum Output Voltage	I_{SINK} = 2 mA	−	−	0.5	V
Output source current (Note 3)	V_{out} = 3 V	2.0	−	−	mA
Output sink current (Note 3)	V_{out} = 0.5 V	2.0	−	−	mA
INTERNAL OFFSET VOLTAGE					
Offset Voltage to the (+) Pin of the Error Amp and the VDRP pin		−	1.30	−	V
VDROOP AMPLIFIER					
Input Bias Current (Note 3)		−200		200	nA
Non−inverting Voltage Range (Note 3)		0	1.3	3	V
Input Offset Voltage (Note 3)	V+ = V− = 1.1 V	−4.0	−	4.0	mV
Open Loop DC Gain	C_L = 20 pF to GND including ESD, R_L = 1 kΩ to GND	−	100		dB
Open Loop Unity Gain Bandwidth	C_L = 20 pF to GND including ESD, R_L = 1 kΩ to GND	−	10	−	MHz
Slew Rate	C_L = 20 pF to GND including ESD, R_L = 1 kΩ to GND	−	5	−	V/μs
Maximum Output Voltage	I_{SOURCE} = 4.0 mA	3	−	−	V
Minimum Output Voltage	I_{SINK} = 1.0 mA	−	−	1	V
Output source current (Note 3)	V_{out} = 3.0 V	4	−	−	mA
Output sink current (Note 3)	V_{out} = 1.0 V	1	−	−	mA

3. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
CSSUM AMPLIFIER					
Current Sense Input to CSSUM Gain	−60 mV < CS < 60 mV	−4.00	−3.88	−3.76	V/V
Current Sense Input to CSSUM −3 dB Bandwidth	C_L = 10 pF to GND, R_L = 10 kΩ to GND	-	4	-	MHz
Current Sense Input to CSSUM Output Slew Rate	ΔV_{in} = 25 mV, CL = 10 pF to GND, Load = 1 k to 1.3 V	-	4	-	V/s
Current Summing Amp Output Offset Voltage	CSx − CSNx = 0, CSx = 1.1 V	−15	-	+15	mV
Maximum CSSUM Output Voltage	CSx − CSxN = −0.15 V (All Phases) I_{SOURCE} = 1 mA	3.0	-	-	V
Minimum CSSUM Output Voltage	CSx − CSxN = 0.066 V (All Phases) I_{SINK} = 1 mA	-	-	0.3	V
Output source current (Note 3)	V_{out} = 3.0 V	1	-	-	mA
Output sink current (Note 3)	V_{out} = 0.3 V	1	-	-	mA
PSI (Power Saving Control, Active Low)					
Enable High Input Leakage Current	External 1 K Pullup to 3.3 V	-	-	1.0	μA
Upper Threshold	V_{UPPER}	-	650	770	mV
Lower Threshold	V_{LOWER}	450	550	-	mV
Hysteresis	V_{UPPER} - V_{LOWER}	-	100	-	mV
APSI_EN (AUTO PSI Function Enable, Active High)					
Enable High Input Leakage Current	External 1k Pullup to 3.3 V	-	-	1.0	μA
Upper Threshold	V_{UPPER}	-	650	770	mV
Lower Threshold	V_{LOWER}	450	550	-	mV
Hysteresis	V_{UPPER} - V_{LOWER}	-	100	-	mV
DRVON					
Output High Voltage	Sourcing 500 μA	3.0	-	-	V
Sourcing Current for Output High	V_{CC} = 5 V	-	2.5	4.0	mA
Output Low Voltage	Sinking 500 μA	-	-	0.7	V
Sinking Current for Output Low		2.5	-	-	mA
Delay Time	Propagation Delay from EN Low to DRVON	-	10	-	ns
Rise Time	C_L (PCB) = 20 pF, ΔV_o = 10% to 90%	-	130	-	ns
Fall Time	C_L (PCB) = 20 pF, ΔV_o = 10% to 90%	-	10	-	ns
Internal Pulldown Resistance		35	70	140	kΩ
V_{CC} Voltage when DRVON Output Valid		-	-	2.0	V
CURRENT SENSE AMPLIFIERS					
Input Bias Current (Note 3)	CSx = CSxN = 1.4 V	-	0	-	nA
Common Mode Input Voltage Range (Note 3)		−0.3	-	2.0	V
Differential Mode Input Voltage Range (Note 3)		−120	-	120	mV
Input Offset Voltage	CSx = CSxN = 1.1 V,	−1.0	-	1.0	mV
Current Sense Input to PWM Gain (Note 3)	0 V < CSx − CSxN < 0.1 V,	5.7	6.0	6.3	V/V
Current Sharing Offset CS1 to CSx	All VID codes	−2.5	-	2.5	mV

3. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
IMON					
V_{DRP} to IMON Gain	1.325 V< V_{DRP} < 1.8 V	1.98	2	2.02	V/V
V_{DRP} to IMON -3 dB Bandwidth	C_L = 30 pF to GND, R_L = 100 kΩ to GND	-	4		MHz
Output Referred Offset Voltage	V_{DRP} = 1.6 V, I_{SOURCE} = 0 mA	81	90	99	mV
Minimum Output Voltage	V_{DRP} = 1.2 V, I_{SINK} = 100 μA	-	-	0.11	V
Output source current (Note 3)	V_{out} = 1 V	300	-	-	μA
Output sink current (Note 3)	V_{out} = 0.3 V	300	-	-	μA
Maximum Clamp Voltage	V_{DRP} Voltage = 2 V, R_{LOAD} = 100 k	-	-	1.15	V
OSCILLATOR					
Switching Frequency Range (Note 3)		100	-	1000	kHz
Switching Frequency Accuracy 2- or 4-Phase	R_{OSC} = 49.9 kΩ	200	-	224	kHz
	R_{OSC} = 24.9 kΩ	374	-	414	
	R_{OSC} = 10 kΩ	800	-	978	
Switching Frequency Accuracy 3-Phase	R_{OSC} = 49.9 kΩ	191	-	234	kHz
	R_{OSC} = 24.9 kΩ	354	-	434	
	R_{OSC} = 10 kΩ	755	-	1000	
R_{OSC} Output Voltage		1.95	2.01	2.065	V
MODULATORS (PWM Comparators)					
Minimum Pulse Width	F_{SW} = 800 KHz	-	30	-	ns
Propagation Delay	±20 mV of Overdrive	-	10	-	ns
0% Duty Cycle	COMP Voltage when the PWM Outputs Remain LO	-	1.3	-	V
100% Duty Cycle	COMP Voltage when the PWM Outputs Remain HI	-	2.3	-	V
PWM Ramp Duty Cycle Matching	Between Any Two Phases	-	90	-	%
PWM Phase Angle Error (Note 3)	Between Adjacent Phases	15	-	15	°
VR_RDY (POWER GOOD) OUTPUT					
VR_RDY Output Saturation Voltage	I_{PGD} = 10 mA,	-	-	0.4	V
VR_RDY Rise Time (Note 3)	External Pullup of 1 kΩ to 1.25 V, C_{TOT} = 45 pF, ΔV_o = 10% to 90%	-	100	150	ns
VR_RDY Output Voltage at Powerup (Note 3)	VR_RDY Pulled up to 5 V via 2 kΩ, $t_{R(VCC)} \le 3 \times t_{R(5V)}$ 100 μs ≤ $t_{R(VCC)}$ ≤ 20 ms	-	-	1.0	V
VR_RDY High − Output Leakage Current (Note 3)	VR_RDY = 5.5 V via 1 K	-	-	0.2	μA
VR_RDY Upper Threshold Voltage	VCore Increasing, DAC = 1.3 V	-	310	270	mV Below DAC
VR_RDY Lower Threshold Voltage	VCore Decreasing DAC = 1.3 V	410	370		mV Below DAC
VR_RDY Rising Delay	VCore Increasing	-	500	-	μs
VR_RDY Falling Delay	VCore Decreasing	-	5	-	μs
PWM OUTPUTS					
Output High Voltage	Sourcing 500 μA	3.0	-	-	V
Mid Output Voltage		1.4	1.5	1.6	V

3. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
PWM OUTPUTS					
Output Low Voltage	Sinking 500 μA	-	-	0.7	V
Delay + Fall Time (Note 3)	C_L (PCB) = **50 pF**, ΔVo = V_{CC} to GND	-	10	15	ns
Delay + Rise Time (Note 3)	C_L (PCB) = **50 pF**, ΔVo = GND to V_{CC}	-	10	15	ns
Output Impedance – HI or LO State	Resistance to V_{CC} (HI) or GND (LO)	-	75	-	Ω
2/3/4-PhASE DETECTION					
Gate Pin Source Current		60	80	150	μA
Gate Pin Threshold Voltage		210	240	265	mV
Phase Detect Timer		15	20	27	μs
DIGITAL SOFT-START					
Soft-Start Ramp Time	DAC = 0 to DAC = 1.1 V	1.0	-	1.5	ms
VR11 Vboot time		400	500	600	μs
VID INPUT					
VID Upper Threshold	V_{UPPER}	-	650	770	mV
VID Lower Threshold	V_{LOWER}	450	550	-	mV
VID Hysteresis	V_{UPPER} - V_{LOWER}	-	100	-	mV
VR11 Input Bias Current (Note 3)				200	nA
Delay before Latching VID Change (VID De-Skewing) (Note 3)	Measured from the edge of the 1st VID change	200	-	300	ns
VID7 Valid Range				3.33	V
ENABLE INPUT					
Enable High Input Leakage Current (Note 3)	Pullup to 1.3 V	-	-	200	nA
VR11 Rising Threshold		-	650	770	mV
VR11 Falling Threshold		450	550	-	mV
VR11 Total Hysteresis	Rising- Falling Threshold	-	100	-	mV
Enable Delay Time	Measure Time from Enable Transitioning HI to when Output Begins	2.5		5.0	ms
CURRENT LIMIT					
I_{LIM} to V_{DRP} Gain	Between V_{DRP} - V_{DFB} = 450 mV and V_{DRP} - V_{DFB} = 650 mV	0.95	1	1.05	V/V
I_{LIM} to V_{DRP} Gain in PSI 4 phase	Between V_{DRP} - V_{DFB} = 450 mV and V_{DRP} - V_{DFB} = 650 mV	-	0.25	-	V/V
I_{LIM} to V_{DRP} Gain in PSI 3 phase	Between V_{DRP} - V_{DFB} = 450 mV and V_{DRP} - V_{DFB} = 650 mV	-	0.33	-	V/V
I_{LIM} to V_{DRP} Gain in PSI 2 phase	Between V_{DRP} - V_{DFB} = 450 mV and V_{DRP} - V_{DFB} = 650 mV	-	0.5	-	V/V
I_{LIM} Offset	V_{DRP} - V_{DFB} = 520 mV	-50	0	50	mV
Delay		-	100	-	ns
OVERVOLTAGE PROTECTION					
VR11 Overvoltage Threshold		DAC +150	DAC +185	DAC +200	mV
VR11 PSI Overvoltage Threshold (Note 3)		(1.6 V DAC) +150		(1.6 V DAC) +200	mV
Delay			100		ns

3. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
UNDERVOLTAGE PROTECTION					
VCC UVLO Start Threshold		4	4.25	4.5	V
VCC UVLO Stop Threshold		3.8	4.05	4.3	V
VCC UVLO Hysteresis			200		mV
12VMON UVLO					
12VMON (High Threshold)	V_{CC} Valid	0.73	0.77	0.82	V
12VMON (Low Threshold)	V_{CC} Valid	0.64	0.68	0.73	V
DAC (FEED FORWARD FUNCTION)					
Output Source Current	V_{OUT} = 3 V	0.25			mA
Output Sink Current	V_{OUT} = 0.3 V	1.5			mA
Max Output Voltage (Note 3)	I_{source} = 2 mA	3			V
Min Output Voltage (Note 3)	I_{sink} = 2 mA			0.5	V
VRM 11 DAC					
Positive DAC Slew Rate		11	-	16.5	mV/μs
System Voltage Accuracy (DAC Value has a 19 mV Offset Over the Output Value)	1.0 V < DAC < 1.6 V 0.8 V < DAC < 1.0 V 0.5 V < DAC < 0.8 V	- - -	- - -	±0.5 ±5 ±8	% mV mV
V_{CC}					
V_{CC} Operating Current	EN Low, No PWM	-	15	30	mA

3. Guaranteed by design, not tested in production.

Table 1. VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	0	0	0	0	0	0	0		00
0	0	0	0	0	0	0	1		01
0	0	0	0	0	0	1	0	1.60000	02
0	0	0	0	0	0	1	1	1.59375	03
0	0	0	0	0	1	0	0	1.58750	04
0	0	0	0	0	1	0	1	1.58125	05
0	0	0	0	0	1	1	0	1.57500	06
0	0	0	0	0	1	1	1	1.56875	07
0	0	0	0	1	0	0	0	1.56250	08
0	0	0	0	1	0	0	1	1.55625	09
0	0	0	0	1	0	1	0	1.55000	0A
0	0	0	0	1	0	1	1	1.54375	0B
0	0	0	0	1	1	0	0	1.53750	0C
0	0	0	0	1	1	0	1	1.53125	0D
0	0	0	0	1	1	1	0	1.52500	0E
0	0	0	0	1	1	1	1	1.51875	0F
0	0	0	1	0	0	0	0	1.51250	10
0	0	0	1	0	0	0	1	1.50625	11
0	0	0	1	0	0	1	0	1.50000	12
0	0	0	1	0	0	1	1	1.49375	13
0	0	0	1	0	1	0	0	1.48750	14
0	0	0	1	0	1	0	1	1.48125	15
0	0	0	1	0	1	1	0	1.47500	16
0	0	0	1	0	1	1	1	1.46875	17
0	0	0	1	1	0	0	0	1.46250	18
0	0	0	1	1	0	0	1	1.45625	19
0	0	0	1	1	0	1	0	1.45000	1A
0	0	0	1	1	0	1	1	1.44375	1B
0	0	0	1	1	1	0	0	1.43750	1C
0	0	0	1	1	1	0	1	1.43125	1D
0	0	0	1	1	1	1	0	1.42500	1E
0	0	0	1	1	1	1	1	1.41875	1F
0	0	1	0	0	0	0	0	1.41250	20
0	0	1	0	0	0	0	1	1.40625	21
0	0	1	0	0	0	1	0	1.40000	22
0	0	1	0	0	0	1	1	1.39375	23
0	0	1	0	0	1	0	0	1.38750	24
0	0	1	0	0	1	0	1	1.38125	25
0	0	1	0	0	1	1	0	1.37500	26
0	0	1	0	0	1	1	1	1.36875	27
0	0	1	0	1	0	0	0	1.36250	28
0	0	1	0	1	0	0	1	1.35625	29
0	0	1	0	1	0	1	0	1.35000	2A
0	0	1	0	1	0	1	1	1.34375	2B
0	0	1	0	1	1	0	0	1.33750	2C
0	0	1	0	1	1	0	1	1.33125	2D
0	0	1	0	1	1	1	0	1.32500	2E
0	0	1	0	1	1	1	1	1.31875	2F

Table 1. VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	0	1	1	0	0	0	0	1.31250	30
0	0	1	1	0	0	0	1	1.30625	31
0	0	1	1	0	0	1	0	1.30000	32
0	0	1	1	0	0	1	1	1.29375	33
0	0	1	1	0	1	0	0	1.28750	34
0	0	1	1	0	1	0	1	1.28125	35
0	0	1	1	0	1	1	0	1.27500	36
0	0	1	1	0	1	1	1	1.26875	37
0	0	1	1	1	0	0	0	1.26250	38
0	0	1	1	1	0	0	1	1.25625	39
0	0	1	1	1	0	1	0	1.25000	3A
0	0	1	1	1	0	1	1	1.24375	3B
0	0	1	1	1	1	0	0	1.23750	3C
0	0	1	1	1	1	0	1	1.23125	3D
0	0	1	1	1	1	1	0	1.22500	3E
0	0	1	1	1	1	1	1	1.21875	3F
0	1	0	0	0	0	0	0	1.21250	40
0	1	0	0	0	0	0	1	1.20625	41
0	1	0	0	0	0	1	0	1.20000	42
0	1	0	0	0	0	1	1	1.19375	43
0	1	0	0	0	1	0	0	1.18750	44
0	1	0	0	0	1	0	1	1.18125	45
0	1	0	0	0	1	1	0	1.17500	46
0	1	0	0	0	1	1	1	1.16875	47
0	1	0	0	1	0	0	0	1.16250	48
0	1	0	0	1	0	0	1	1.15625	49
0	1	0	0	1	0	1	0	1.15000	4A
0	1	0	0	1	0	1	1	1.14375	4B
0	1	0	0	1	1	0	0	1.13750	4C
0	1	0	0	1	1	0	1	1.13125	4D
0	1	0	0	1	1	1	0	1.12500	4E
0	1	0	0	1	1	1	1	1.11875	4F
0	1	0	1	0	0	0	0	1.11250	50
0	1	0	1	0	0	0	1	1.10625	51
0	1	0	1	0	0	1	0	1.10000	52
0	1	0	1	0	0	1	1	1.09375	53
0	1	0	1	0	1	0	0	1.08750	54
0	1	0	1	0	1	0	1	1.08125	55
0	1	0	1	0	1	1	0	1.07500	56
0	1	0	1	0	1	1	1	1.06875	57
0	1	0	1	1	0	0	0	1.06250	58
0	1	0	1	1	0	0	1	1.05625	59
0	1	0	1	1	0	1	0	1.05000	5A
0	1	0	1	1	0	1	1	1.04375	5B
0	1	0	1	1	1	0	0	1.03750	5C
0	1	0	1	1	1	0	1	1.03125	5D
0	1	0	1	1	1	1	0	1.02500	5E
0	1	0	1	1	1	1	1	1.01875	5F

Table 1. VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	1	1	0	0	0	0	0	1.01250	60
0	1	1	0	0	0	0	1	1.00625	61
0	1	1	0	0	0	1	0	1.00000	62
0	1	1	0	0	0	1	1	0.99375	63
0	1	1	0	0	1	0	0	0.98750	64
0	1	1	0	0	1	0	1	0.98125	65
0	1	1	0	0	1	1	0	0.97500	66
0	1	1	0	0	1	1	1	0.96875	67
0	1	1	0	1	0	0	0	0.96250	68
0	1	1	0	1	0	0	1	0.95625	69
0	1	1	0	1	0	1	0	0.95000	6A
0	1	1	0	1	0	1	1	0.94375	6B
0	1	1	0	1	1	0	0	0.93750	6C
0	1	1	0	1	1	0	1	0.93125	6D
0	1	1	0	1	1	1	0	0.92500	6E
0	1	1	0	1	1	1	1	0.91875	6F
0	1	1	1	0	0	0	0	0.91250	70
0	1	1	1	0	0	0	1	0.90625	71
0	1	1	1	0	0	1	0	0.90000	72
0	1	1	1	0	0	1	1	0.89375	73
0	1	1	1	0	1	0	0	0.88750	74
0	1	1	1	0	1	0	1	0.88125	75
0	1	1	1	0	1	1	0	0.87500	76
0	1	1	1	0	1	1	1	0.86875	77
0	1	1	1	1	0	0	0	0.86250	78
0	1	1	1	1	0	0	1	0.85625	79
0	1	1	1	1	0	1	0	0.85000	7A
0	1	1	1	1	0	1	1	0.84375	7B
0	1	1	1	1	1	0	0	0.83750	7C
0	1	1	1	1	1	0	1	0.83125	7D
0	1	1	1	1	1	1	0	0.82500	7E
0	1	1	1	1	1	1	1	0.81875	7F
1	0	0	0	0	0	0	0	0.81250	80
1	0	0	0	0	0	0	1	0.80625	81
1	0	0	0	0	0	1	0	0.80000	82
1	0	0	0	0	0	1	1	0.79375	83
1	0	0	0	0	1	0	0	0.78750	84
1	0	0	0	0	1	0	1	0.78125	85
1	0	0	0	0	1	1	0	0.77500	86
1	0	0	0	0	1	1	1	0.76875	87
1	0	0	0	1	0	0	0	0.76250	88
1	0	0	0	1	0	0	1	0.75625	89
1	0	0	0	1	0	1	0	0.75000	8A
1	0	0	0	1	0	1	1	0.74375	8B
1	0	0	0	1	1	0	0	0.73750	8C
1	0	0	0	1	1	0	1	0.73125	8D
1	0	0	0	1	1	1	0	0.72500	8E
1	0	0	0	1	1	1	1	0.71875	8F

Table 1. VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
1	0	0	1	0	0	0	0	0.71250	90
1	0	0	1	0	0	0	1	0.70625	91
1	0	0	1	0	0	1	0	0.70000	92
1	0	0	1	0	0	1	1	0.69375	93
1	0	0	1	0	1	0	0	0.68750	94
1	0	0	1	0	1	0	1	0.68125	95
1	0	0	1	0	1	1	0	0.67500	96
1	0	0	1	0	1	1	1	0.66875	97
1	0	0	1	1	0	0	0	0.66250	98
1	0	0	1	1	0	0	1	0.65625	99
1	0	0	1	1	0	1	0	0.65000	9A
1	0	0	1	1	0	1	1	0.64375	9B
1	0	0	1	1	1	0	0	0.63750	9C
1	0	0	1	1	1	0	1	0.63125	9D
1	0	0	1	1	1	1	0	0.62500	9E
1	0	0	1	1	1	1	1	0.61875	9F
1	0	1	0	0	0	0	0	0.61250	A0
1	0	1	0	0	0	0	1	0.60625	A1
1	0	1	0	0	0	1	0	0.60000	A2
1	0	1	0	0	0	1	1	0.59375	A3
1	0	1	0	0	1	0	0	0.58750	A4
1	0	1	0	0	1	0	1	0.58125	A5
1	0	1	0	0	1	1	0	0.57500	A6
1	0	1	0	0	1	1	1	0.56875	A7
1	0	1	0	1	0	0	0	0.56250	A8
1	0	1	0	1	0	0	1	0.55625	A9
1	0	1	0	1	0	1	0	0.55000	AA
1	0	1	0	1	0	1	1	0.54375	AB
1	0	1	0	1	1	0	0	0.53750	AC
1	0	1	0	1	1	0	1	0.53125	AD
1	0	1	0	1	1	1	0	0.52500	AE
1	0	1	0	1	1	1	1	0.51875	AF
1	0	1	1	0	0	0	0	0.51250	B0
1	0	1	1	0	0	0	1	0.50625	B1
1	0	1	1	0	0	1	0	0.50000	B2
1	1	1	1	1	1	1	0	OFF	FE
1	1	1	1	1	1	1	1	OFF	FF

FUNCTIONAL DESCRIPTION

General

The NCP5392Q provides up to four−phase buck solution which combines differential voltage sensing, differential phase current sensing, and adaptive voltage positioning to provide accurately regulated power necessary for Intel VR11.1 CPU power system. NCP5392Q has been designed to work with the NCP5359 driver.

AUTO−PSI Function

NCP5392Q makes energy saving possible without receiving PSI signal from the CPU by wisely introducing Auto−PSI feature. The device will monitor VID lines for transition into/out−of Low Power States. When the VID drops (An indication of entering power saving state), the Auot−PSI logic will detect the transition and enable PSI mode. On the other hand, when the VID rises (exiting power saving mode), the Auto−PSI logic detects the transition and exit PSI mode automatically. Auto−PSI uses the dynamic VID(DVID) transitions of VR11.0 and VR11.1 to shed phases. The phase shedding improves the efficiency of the Vcore regulator eventually. In PSI mode, the total current limit is reduced by the ratio of the phase count left after phase shedding.

Auto−PSI function can be activated and deactivated by toggling APSI_EN (PIN38), but with lower priority compared to PSI signal. When PSI (PIN37) is pulled to low, the system will be forced into PSI mode unconditionally, and APSI_EN signal will be shielded.

NCP5392Q can be operated up to four phases. It operates at one phase mode when the system enter PSI mode automatically (for example, VID down from 1.2 V to 1.1 V).

Remote Output Sensing Amplifier(RSA)

A true differential amplifier allows the NCP5392Q to measure V_{core} voltage feedback with respect to the V_{core} ground reference point by connecting the V_{core} reference point to VSP, and the V_{core} ground reference point to VSN. This configuration keeps ground potential differences between the local controller ground and the V_{core} ground reference point from affecting regulation of V_{core} between V_{core} and V_{core} ground reference points. The RSA also subtracts the DAC (minus VID offset) voltage, thereby producing an unamplified output error voltage at the DIFFOUT pin. This output also has a 1.3 V bias voltage as the floating ground to allow both positive and negative error voltages.

Precision Programmable DAC

A precision programmable DAC is provided and system trimmed. This DAC has 0.5% accuracy over the entire operating temperature range of the part. The DAC can be programmed to support either Intel VR11 VID code specifications.

High Performance Voltage Error Amplifier

The error amplifier is designed to provide high slew rate and bandwidth. Although not required when operating as the controller of a voltage regulator, a capacitor from COMP to VFB is required for stable unity gain test configurations.

Gate Driver Outputs and 2/3/4 Phase Operation

The part can be configured to run in 2−, 3−, or 4−phase mode. In 2−phase mode, phases 1 and 3 should be used to drive the external gate drivers as shown in the 2−phase Applications Schematic, G2 and G4 must be grounded. In 3−phase mode, gate output G4 must be grounded as shown in the 3−phase Applications Schematic. In 4−phase mode all 4 gate outputs are used as shown in the 4−phase Applications Schematic. The Current Sense inputs of unused channels should be connected to VCCP shown in the Application Schematics. Please refer to table “PIN CONNECTIONS vs. PHASE COUNTS” for details.

Differential Current Sense Amplifiers and Summing Amplifier

Four differential amplifiers are provided to sense the output current of each phase. The inputs of each current sense amplifier must be connected across the current sensing element of the phase controlled by the corresponding gate output (G1, G2, G3, or G4). If a phase is unused, the differential inputs to that phase’s current sense amplifier must be shorted together and connected to the output as shown in the 2− and 3−phase Application Schematics.

The current signals sensed from inductor DCR are fed into a summing amplifier to have a summed−up output (CSSUM). Signal of CSSUM combines information of total current of all phases in operation.

The outputs of current sense amplifiers control three functions. First, the summing current signal (CCSUM) of all phases will go through DROOP amplifier and join the voltage feedback loop for output voltage positioning. Second, the output signal from DROOP amplifier also goes to ILIM amplifier to monitor the output current limit. Finally, the individual phase current contributes to the current balance of all phases by offsetting their ramp signals of PWM comparators.

Thermal Compensation Amplifier with VDRP and VDFB Pins

Thermal compensation amplifier is an internal amplifier in the path of droop current feedback for additional adjustment of the gain of summing current and temperature compensation. The way thermal compensation is implemented separately ensures minimum interference to the voltage loop compensation network.

Oscillator and Triangle Wave Generator

A programmable precision oscillator is provided. The oscillator's frequency is programmed by the resistance connected from the ROSC pin to ground. The user will usually form this resistance from two resistors in order to create a voltage divider that uses the ROSC output voltage as the reference for creating the current limit setpoint voltage. The oscillator frequency range is 100 kHz per phase to 1.0 MHz per phase. The oscillator generates up to 4 symmetrical triangle waveforms with amplitude between 1.3 V and 2.3 V. The triangle waves have a phase delay between them such that for 2-, 3- and 4-phase operation the PWM outputs are separated by 180, 120, and 90 angular degrees, respectively.

PWM Comparators with Hysteresis

Four PWM comparators receive an error signal at their noninverting input. Each comparator receives one of the triangle waves at its inverting output. The output of each comparator generates the PWM outputs G1, G2, G3, and G4.

During steady state operation, the duty cycle will center on the valley of the triangle waveform, with steady state duty cycle calculated by V_{out}/V_{in}. During a transient event, both high and low comparator output transitions shift phase to the points where the error signal intersects the down and up ramp of the triangle wave.

PROTECTION FEATURES

Power Saving Mode

Upon receiving PSI low command, or VID down with Auto-PSI enabled, the NCP5392Q enters power saving mode with only single phase running. The device operates in power saving mode to maintain a high power efficiency and good transient performance.

Undervoltage Lockout

An undervoltage lockout (UVLO) senses the V_{CC} input. During power-up, the input voltage to the controller is monitored, and the PWM outputs and the soft-start circuit are disabled until the input voltage exceeds the threshold voltage of the UVLO comparator. The UVLO comparator incorporates hysteresis to avoid chattering.

12VMON UVLO and VIN Information

12V UVLO senses the 12V power supply by connecting it to the 12VMON pin through an appropriate resistor divider. During power-up, the 12VMON is monitored and the PWM outputs and soft-start circuit are disabled until the voltage exceeds the threshold of its UVLO comparator. The UVLO comparator incorporates hysteresis to avoid chattering.

Overcurrent Shutdown

A programmable overcurrent function is incorporated within the IC. A comparator and latch make up this function. The inverting input of the comparator is connected to the ILIM pin. The voltage at this pin sets the maximum output current the converter can produce. The ROSC pin provides a convenient and accurate reference voltage from which a resistor divider can create the overcurrent setpoint voltage. Although not actually disabled, tying the ILIM pin directly to the ROSC pin sets the limit above useful levels - effectively disabling overcurrent shutdown. The comparator noninverting input is the summed current information from the VDRP minus offset voltage. The overcurrent latch is set when the current information exceeds the voltage at the ILIM pin. The outputs are pulled low, and the soft-start is pulled low. The outputs will remain disabled until the V_{CC} voltage is removed and re-applied, or the ENABLE input is brought low and then high.

Output Overvoltage and Undervoltage Protection and Power Good Monitor

An output voltage monitor is incorporated. During normal operation, if the output voltage is 180 mV (typical) over the DAC voltage, the VR_RDY goes low, the DRVON signal remains high, the PWM outputs are set low. The outputs will remain disabled until the V_{CC} voltage is removed and reapplied. During normal operation, if the output voltage falls more than 350 mV below the DAC setting, the VR_RDY pin will be set low until the output voltage rises.

Soft-Start

The VR11 mode ramps V_{core} to 1.1 V boot voltage at a fixed rate of 0.8 mV/μS, pauses at 1.1 V for around 500 μS, reads the VID pins to determine the DAC setting. Then ramps V_{core} to the final DAC setting at the Dynamic VID slew rate of up to 12.5 mV/μS. Typical VR11 soft-start sequences are shown in the following graphs (Figure 9 and 10).

APPLICATION INFORMATION

The NCP5392Q demo board for the NCP5392Q is available by request. It is configured as a four phase solution with decoupling designed to provide a 1 mΩ load line under a 100 A step load.

Startup Procedure

Start by installing the test tool software. It is best to power the test tool from a separate ATX power supply. The test tool should be set to a valid VID code of 0.5 V or above in order for the controller to start. Consult the VTT help manual for more detailed instruction.

Step Load Testing

The VTT tool is used to generate the d_i/d_t step load. Select the dynamic loading option in the VTT test tool software. Set the desired step load size, frequency, duty, and slew rate. See Figure 6.

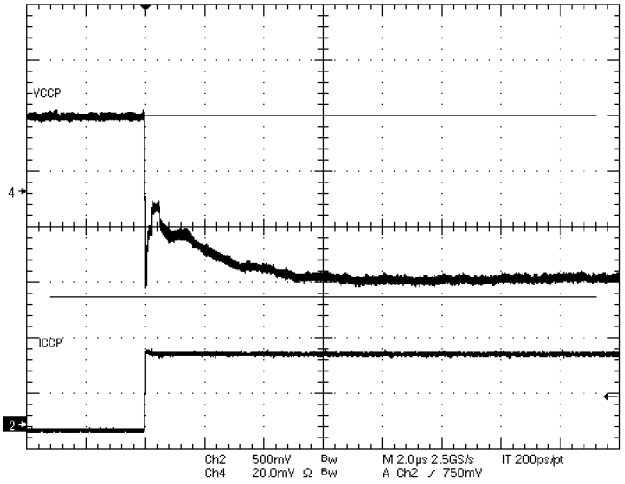


Figure 6. Typical Load Step Response (full load, 35 A − 100 A)

Dynamic VID Testing

The VTT tool provides for VID stepping based on the Intel Requirements. Select the Dynamic VID option. Before enabling the test set the lowest VID to 0.5 V or greater and set the highest VID to a value that is greater than the lowest VID selection, then enable the test. See Figures 7 and 8.

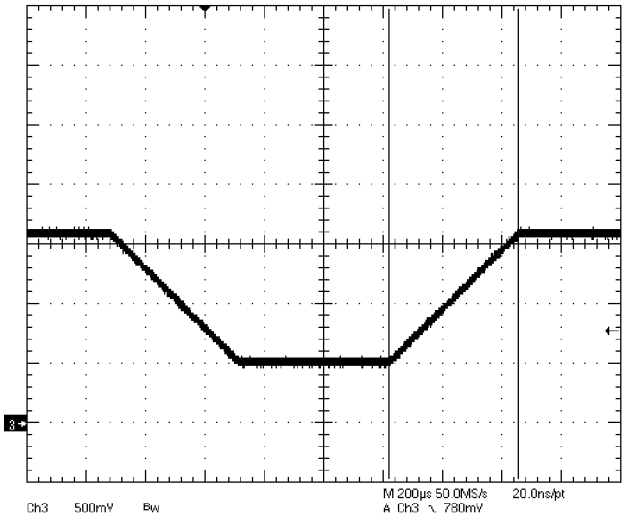


Figure 7. 1.6 V to 0.5 V Dynamic VID response

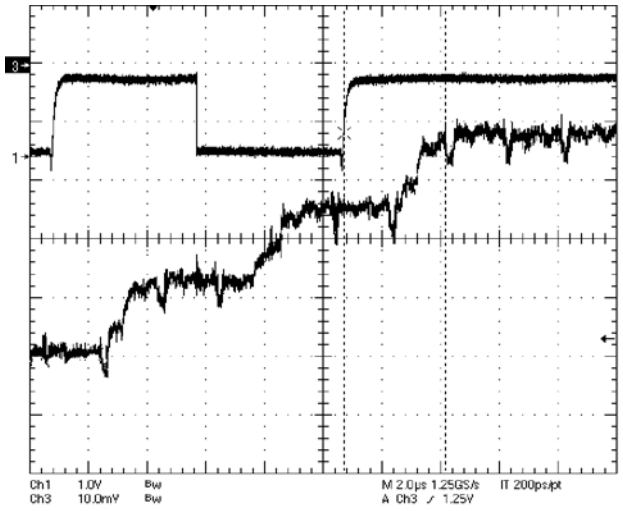


Figure 8. Dynamic VID Settling Time Rising (CH1: VID1, CH2: DAC, CH3:VCCP)

DESIGN METHODOLOGY

Decoupling the V_{CC} Pin on the IC

An RC input filter is required as shown in the V_{CC} pin to minimize supply noise on the IC. The resistor should be sized such that it does not generate a large voltage drop between 5 V supply and the IC.

Understanding Soft−Start

The controller supports typical VR11 startup routines. Vcore voltage ramps to the 1.1 V boot voltage, with a pause to capture the VID code then resume ramping to target value based on internal slew rate limit. The initial ramp rate was set to be 0.8 mV/μS.

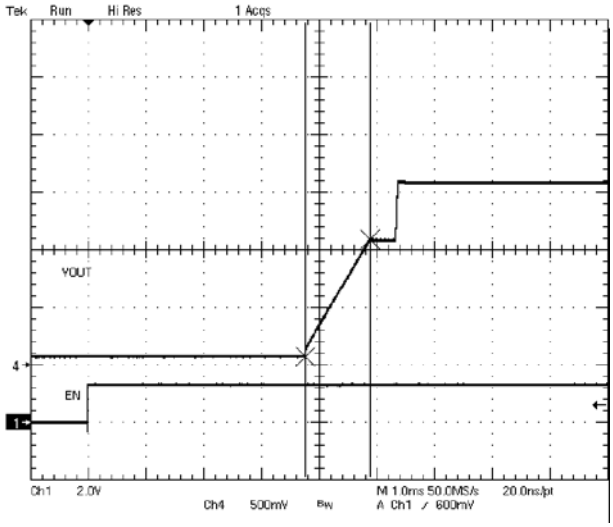


Figure 9. VR11.1 Startup

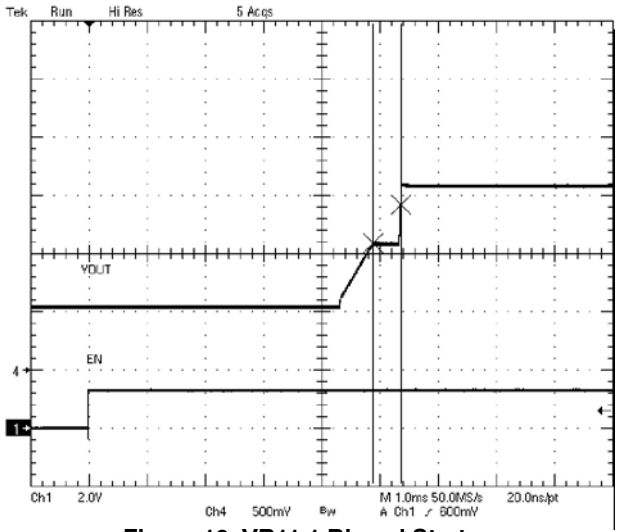


Figure 10. VR11.1 Biased Startup

Programming the Current Limit and the Oscillator Frequency

The demo board is set for an operating frequency of approximately 330 kHz. The R_{OSC} pin provides a 2.0 V reference voltage which is divided down with a resistor divider and fed into the current limit pin ILIM. Then calculate the individual RLIM1 and RLIM2 values for the divider. The series resistors RLIM1 and RLIM2 sink current from the ILIM pin to ground. This current is internally mirrored into a capacitor to create an oscillator. The period is proportional to the resistance and frequency is inversely proportional to the total resistance. The total resistance may be estimated by Equation 1. This equation is valid for the individual phase frequency in both three and four phase mode.

$$R_{osc} \cong 20947 \times F_{SW}^{-1.1262} \quad \text{(eq. 1)}$$

$$30.5\ k\Omega \cong 20947 \times 330^{-1.1262}$$

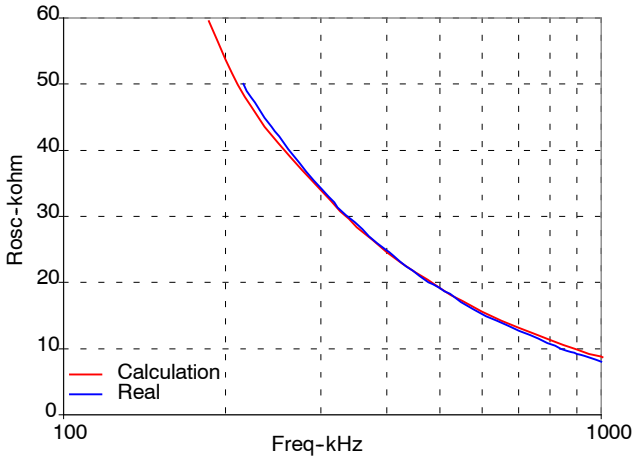


Figure 11. ROSC vs. Frequency

The current limit function is based on the total sensed current of all phases multiplied by a controlled gain (Acssum*Adrp). DCR sensed inductor current is a function of the winding temperature. The best approach is to set the maximum current limit based on expected average maximum temperature of the inductor windings,

$$DCR_{Tmax} = DCR_{25C}(1 + 0.00393 \cdot (T_{max} - 25)) \quad \text{(eq. 2)}$$

For multiphase controller, the ripple current can be calculated as,

$$Ipp = \frac{(V_{in} - N \cdot V_{out}) \cdot V_{out}}{L \cdot F_{SW} \cdot V_{in}} \quad \text{(eq. 3)}$$

Therefore calculate the current limit voltage as below,

$$V_{LIMIT} \cong A_{CSSUM} \cdot A_{DRP} \cdot DCR_{Tmax} \cdot (I_{MIN\_OCP} \cdot + 0.5 \cdot Ipp) \quad \text{(eq. 4)}$$

$$V_{LIMIT} \cong A_{CSSUM} \cdot A_{DRP} \cdot DCR_{Tmax} \cdot \left(I_{MIN\_OCP} \cdot + 0.5 \cdot \frac{(V_{in} - N \cdot V_{out}) \cdot V_{out}}{L \cdot F_{SW} \cdot V_{in}}\right)$$

In Equation 4, A_{CSSUM} and A_{DRP} are the gain of current summing amplifier and droop amplifier.

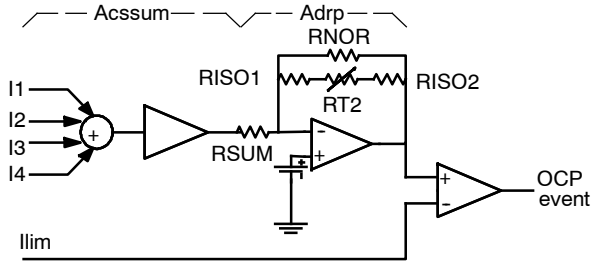


Figure 12. ACSSUM and ADRP

As introduced before, V_{LIMIT} comes from a resistor divider connected to Rosc pin, thus,

$$V_{LIMIT} = 2\,V \cdot \frac{R_{LIM2}}{R_{LIM1} + R_{LIM2}} \cdot COEpsi \quad \text{(eq. 5)}$$

$$A_{CSSUM} = -4$$

$$A_{DRP} = -\frac{R_{NOR} \cdot (R_{ISO1} + R_{ISO2} + R_{T2})}{(R_{NOR} + R_{ISO1} + R_{ISO2} + R_{T2}) \cdot R_{SUM}} \quad \text{(eq. 6)}$$

R_{ISO1} and R_{ISO2} are in series with R_{T2}, the NTC temperature sense resistor placed near inductor. R_{SUM} is the resistor connecting between pin VDFB and pin CSSUM. If PSI = 1, PSI function is off, the current limit follows the Equation 7; if PSI = 0, the power saving mode will be enabled, COEpsi is a coefficient for the current limiting related with power saving function (PSI), the current limit can be calculated from Equation 8. COEpsi value is one over the original phase count N. Refer to the PSI and phase shedding section for more details.

Final Equations for the Current Limit Threshold

Final equations are described based on two conditions: normal mode and PSI mode.

$$I_{LIMIT}(normal) \cong \frac{\frac{2V \cdot R_{LIM2}}{R_{LIM1}+R_{LIM2}}}{4 \cdot \frac{R_{NOR}\cdot(R_{ISO1}+R_{ISO2}+R_{T2})}{(R_{NOR}+R_{ISO1}+R_{ISO2}+R_{T2})\cdot R_{SUM}} \cdot DCR_{25C}(1 + 0.00393 \cdot (T_{inductor} - 25))} - 0.5 \cdot \frac{(V_{in} - N \cdot V_{out}) \cdot V_{out}}{L \cdot F_{SW} \cdot V_{in}} \quad \text{(eq. 7)}$$

$$I_{LIMIT}(PSI) \cong \frac{\frac{2V \cdot R_{LIM2}}{R_{LIM1}+R_{LIM2}} \cdot COEpsi}{4 \cdot \frac{R_{NOR}\cdot(R_{ISO1}+R_{ISO2}+R_{T2})}{(R_{NOR}+R_{ISO1}+R_{ISO2}+R_{T2})\cdot R_{SUM}} \cdot DCR_{25C}(1 + 0.00393 \cdot (T_{inductor} - 25))} - 0.5 \cdot \frac{(V_{in} - V_{out}) \cdot V_{out}}{L \cdot F_{SW} \cdot V_{in}} \quad \text{(eq. 8)}$$

N is the number of phases involved in the circuit.

The inductors on the demo board have a DCR at 25°C of 0.6 mΩ. Selecting the closest available values of 21.3 kΩ for R_{LIM1} and 9.28 kΩ for R_{LIM2} yields a nominal operating frequency of 330 kHz. Select $R_{ISO}1$ = 1 k, R_{ISO2} = 1 k, R_{T2} = 10 K (25°C), R_{NOR}/R_{SUM} = 2, (refer to application diagram). That results to an approximate current limit of 133 A at 100°C for a four phase operation and 131 A at 25°C. The total sensed current can be observed as a scaled voltage at the VDRP with a positive no-load offset of approximately 1.3 V.

Inductor Selection

When using inductor current sensing it is recommended that the inductor does not saturate by more than 10% at maximum load. The inductor also must not go into hard saturation before current limit trips. The demo board includes a four phase output filter using the T44-8 core from Micrometals with 3 turns and a DCR target of 0.6 mΩ @ 25°C. Smaller DCR values can be used, however, current sharing accuracy and droop accuracy decrease as DCR decreases. Use the NCP5392Q design aide for regulation accuracy calculations for specific value of DCR.

Inductor Current Sensing Compensation

The NCP5392Q uses the inductor current sensing method. An RC filter is selected to cancel out the impedance from inductor and recover the current information through the inductor's DCR. This is done by matching the RC time constant of the sensing filter to the L/DCR time constant. The first cut approach is to use a 0.1 μF capacitor for C and then solve for R.

$$R_{sense}(T) = \frac{L}{0.1 \cdot \mu F \cdot DCR_{25C} \cdot (1 + 0.00393(T - 25))} \quad \text{(eq. 9)}$$

Because the inductor value is a function of load and inductor temperature final selection of R is best done experimentally on the bench by monitoring the V_{droop} pin and performing a step load test on the actual solution.

Simple Average SPICE Model

A simple state average model shown in Figure 13 can be used to determine a stable solution and provide insight into the control system.

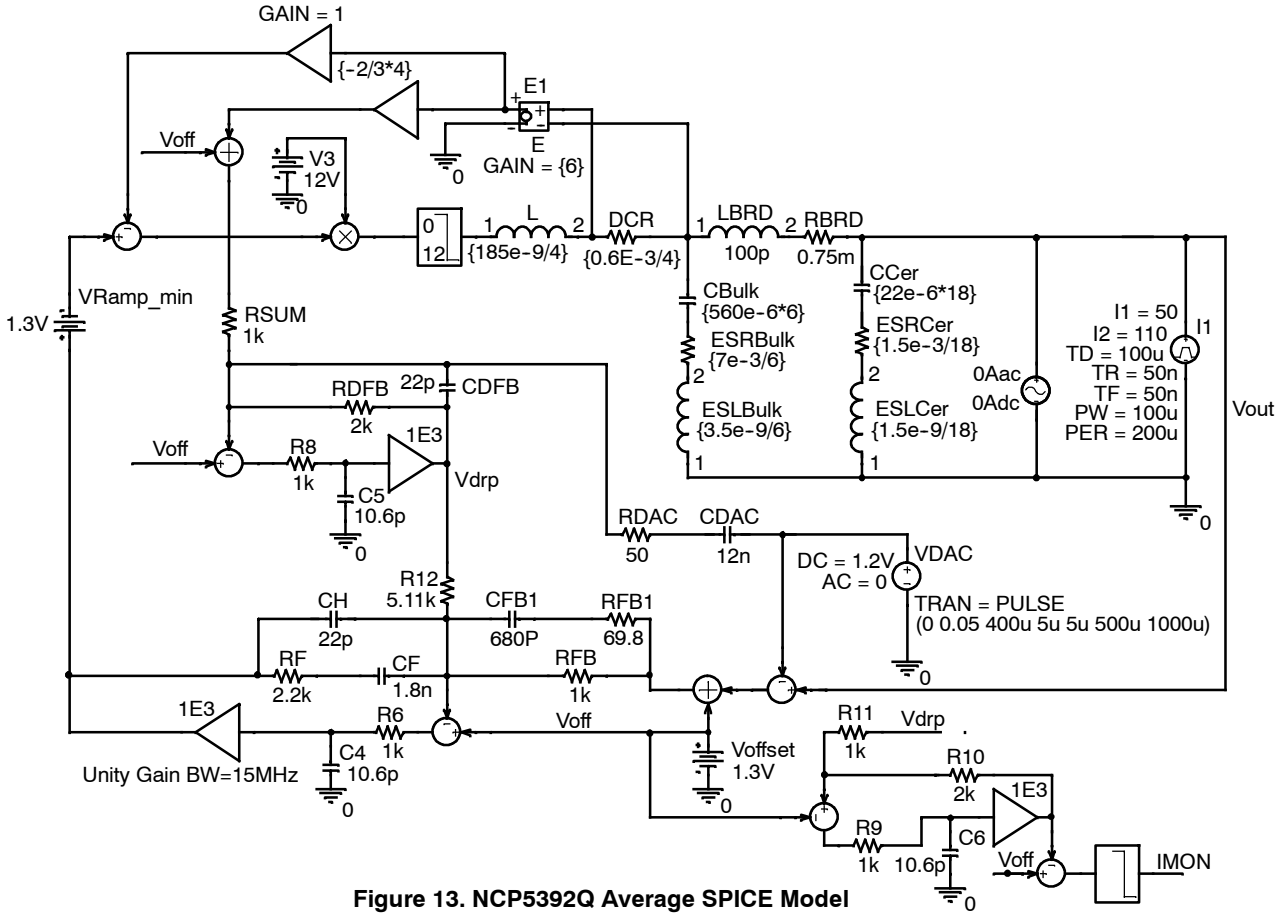


Figure 13. NCP5392Q Average SPICE Model

Compensation and Output Filter Design

If the required output filter and switching frequency are significantly different, it's best to use the available PSPICE models to design the compensation and output filter from scratch.

The design target for this demo board was 1.0 mΩ up to 2.0 MHz. The phase switching frequency is currently set to 330 kHz. It can easily be seen that the board impedance of 0.75 mΩ between the load and the bulk capacitance has a large effect on the output filter. In this case the six 560 μF bulk capacitors have an ESR of 7.0 mΩ. Thus the bulk ESR plus the board impedance is 1.15 mΩ + 0.75 mΩ or 1.9 mΩ. The actual output filter impedance does not drop to 1.0 mΩ until the ceramic breaks in at over 375 kHz. The controller must provide some loop gain slightly less than one out to a frequency in excess 300 kHz. At frequencies below where the bulk capacitance ESR breaks with the bulk capacitance, the DC-DC converter must have sufficiently high gain to control the output impedance completely. Standard Type-3 compensation works well with the NCP5392Q.

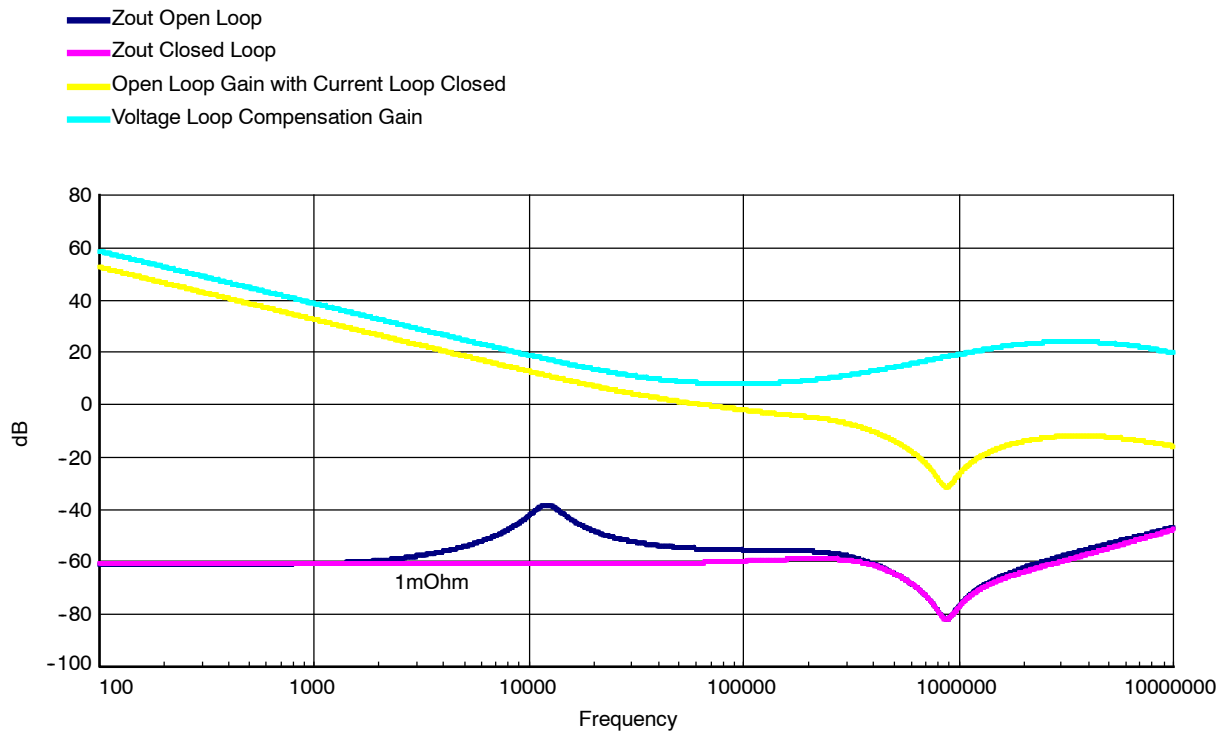


Figure 14. NCP5392Q Circuit Frequency Response

The goal is to compensate the system such that the resulting gain generates constant output impedance from DC up to the frequency where the ceramic takes over holding the impedance below 1.0 mΩ. See the example of the locations of the poles and zeros that were set to optimize the model above.

By matching the following equations a good set of starting compensation values can be found for a typical mixed bulk and ceramic capacitor type output filter.

$$\frac{1}{2\pi \cdot CF \cdot RF} = \frac{1}{2\pi \cdot (RBRD + ESR_{Bulk}) \cdot C_{Bulk}} \quad \text{(eq. 10)}$$

$$\frac{1}{2\pi \cdot CFB1 \cdot (RFB1 + RFB)} = \frac{1}{2\pi \cdot C_{Cer} \cdot (RBRD + ESR_{Bulk})} \quad \text{(eq. 11)}$$

R_{FB} should be set to provide optimal thermal compensation in conjunction with thermistor R_{T2}, R_{ISO1} and R_{ISO2}. With R_{FB} set to 1.0 kΩ, R_{FB1} is usually set to 100 Ω for maximum phase boost, and the value of RF is typically set to 3.0 kΩ.

Droop Injection and Thermal Compensation

The VDRP signal is generated by summing the sensed output currents for each phase. A droop amplifier is added to adjust the total gain to approximately eight. VDRP is externally summed into the feedback network by the resistor RDRP. This introduces an offset which is proportional to the output current thereby forcing a controlled, resistive output impedance.

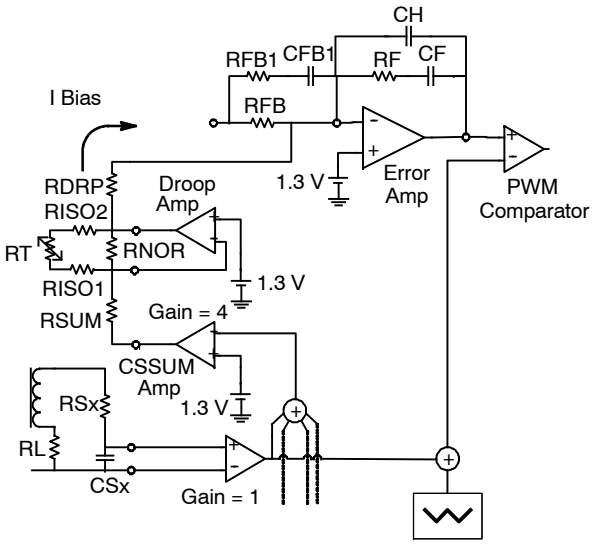


Figure 15. Droop Injection and Thermal Compensation

RDRP determines the target output impedance by the basic equation:

$$\frac{V_{out}}{I_{out}} = Z_{out} = \frac{R_{FB} \cdot DCR \cdot A_{CSSUM} \cdot A_{DRP}}{R_{DRP}} \quad \text{(eq. 12)}$$

$$R_{DRP} = \frac{R_{FB} \cdot DCR \cdot A_{CSSUM} \cdot A_{DRP}}{Z_{out}} \quad \text{(eq. 13)}$$

The value of the inductor's DCR is a function of temperature according to the Equation 14:

$$DCR\ (T) = DCR_{25C} \cdot (1 + 0.00393 \cdot (T - 25)) \quad \text{(eq. 14)}$$

Actual DCR increases by temperature, the system can be thermally compensated to cancel this effect to a great degree by adding an NTC in parallel with R_{NOR} to reduce the droop gain as the temperature increases. The NTC device is nonlinear. Putting a resistor in series with the NTC helps make the device appear more linear with temperature. The series resistor is split and inserted on both sides of the NTC to reduce noise injection into the feedback loop. The recommended total value for R_{ISO1} plus R_{ISO2} is approximately 1.0 kΩ.

The output impedance varies with inductor temperature by the equation:

$$Z_{out}(T) = \frac{R_{FB} \cdot DCR_{25C} \cdot (1 + 0.00393 \cdot (T - 25)) \cdot A_{CSSUM} \cdot A_{DRP}}{R_{DRP}} \quad \text{(eq. 15)}$$

By including the NTC R_{T2} and the series isolation resistors the new equation becomes:

$$Z_{out}(T) = \frac{R_{FB} \cdot DCR_{25C} \cdot (1 + 0.00393 \cdot (T - 25)) \cdot A_{CSSUM} \cdot \frac{R_{NOR} \cdot (R_{ISO1} + R_{ISO2} + R_{T2})}{(R_{NOR} + R_{ISO1} + R_{ISO2} + R_{T2}) \cdot R_{SUM}}}{R_{DRP}} \quad \text{(eq. 16)}$$

The typical equation of an NTC is based on a curve fit Equation 17

$$RT2(T) = RT2_{25C} \cdot e^{\beta\left[\left(\frac{1}{273+T}\right)-\left(\frac{1}{298}\right)\right]} \quad \text{(eq. 17)}$$

The demo board use a 10 kΩ NTC with a β value of 3740. Figure 16 shows the comparison of the compensated output impedance and uncompensated output impedance varying with temperature.

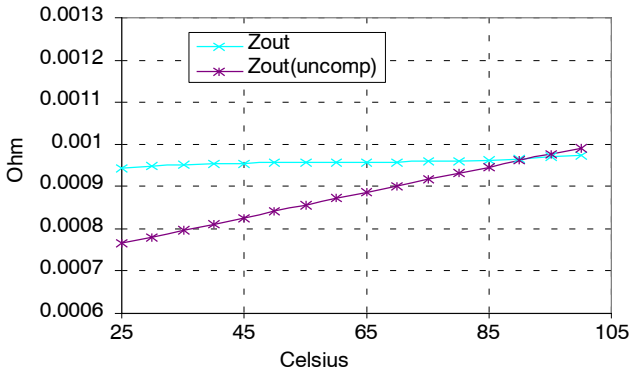


Figure 16. Z_{out} vs. Temperature

IMON for Current Monitor

Since VDRP signal reflects the current information of all phases. It can be fed into the IMON amplifier for current monitoring as shown in Figure 17. IMON amplifier has a fixed gain of 2 with an offset when VDRP is equal to 1.3 V, the internal floating reference voltage. The IMON amplifier will be saturated at an maximum output of 1.09 V therefore the total gain of current should be carefully considered to make the maximum load current indicated by the IMON output. Figure 18 shows a typical of the relation between IMON output and the load current.

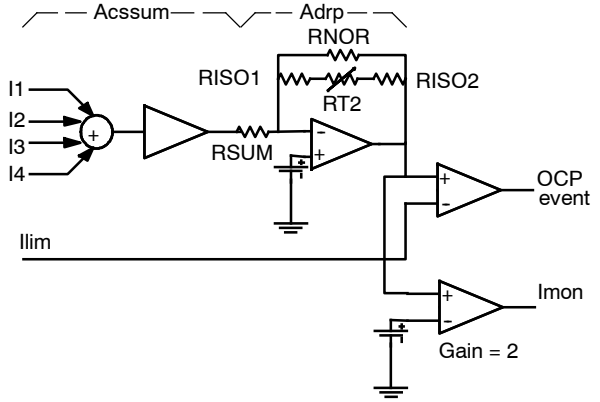


Figure 17. IMON Circuit

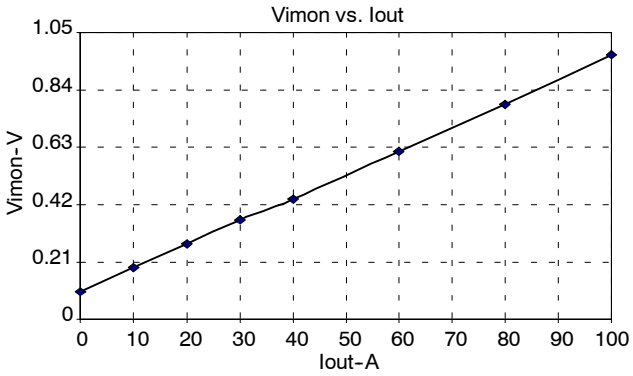


Figure 18. IMON Output vs. Output Current

Power Saving Indicator (PSI) and Phase Shedding

VR11.1 requires the processor to provide an output signal to the VR controller to indicate when the processor is in a low power state. NCP5392Q use the status of PSI pin to decide if there is a need to change its operating state to maximize efficiency at light loads. When PSI = 0, the PSI function will be enabled, and VR system will be running at a single phase power saving mode.

The PSI signal will de-assert 1 μs prior to moving to a normal power state.

When system switches on PSI function, a phase shedding will be presented. Only one is active in the emulation mode while other phases are shed. Figure 19 indicates a PSI-on transition from a 3-phase mode to a single phase mode. While staying stable in PSI mode, the PWM signal of phase 1 will vary from a low-state level to high level while other phases all go to mid-state level (1.5 V typical). Vice verse, when PSI signal goes high, the system will go back to the original phase mode such as shown in Figure 20.

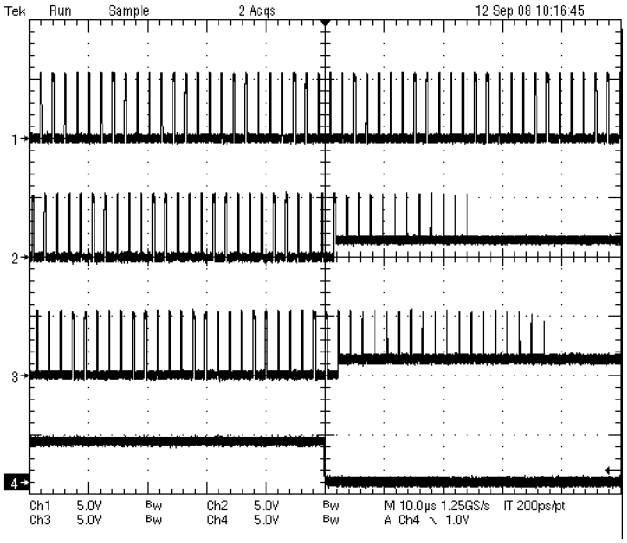


Figure 19. PSI turns on, CH1: PWM1, CH2: PWM2, CH3: PWM3, CH4: PSI

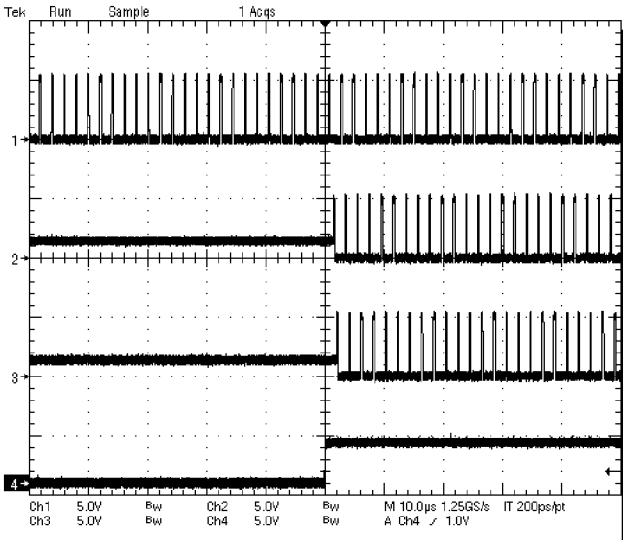


Figure 20. PSI turns off, CH1: PWM1, CH2: PWM2, CH3: PWM3, CH4: PSI

Auto-PSI Function:

In Auto-PSI mode (APSI_EN=1, PSI=1), the device will monitor VID lines for transition into/out-of Low Power States. Figures 21 and 22 describe the Auto-PSI function during VID transitions.

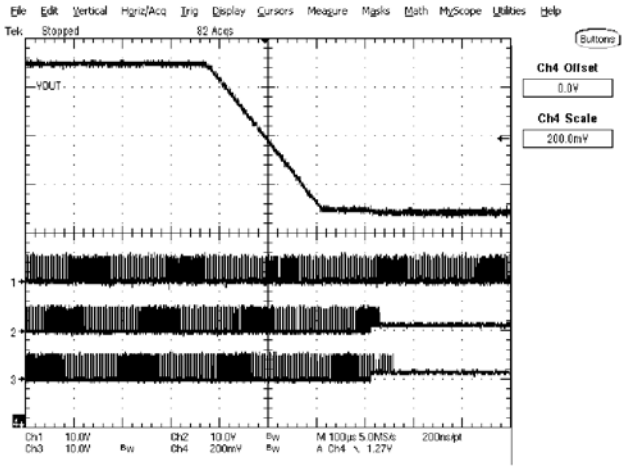


Figure 21. 10 A Load, VID Down, into PSI, CH1: PWM1, CH2: PWM2, CH3: PWM3, CH4: VOUT

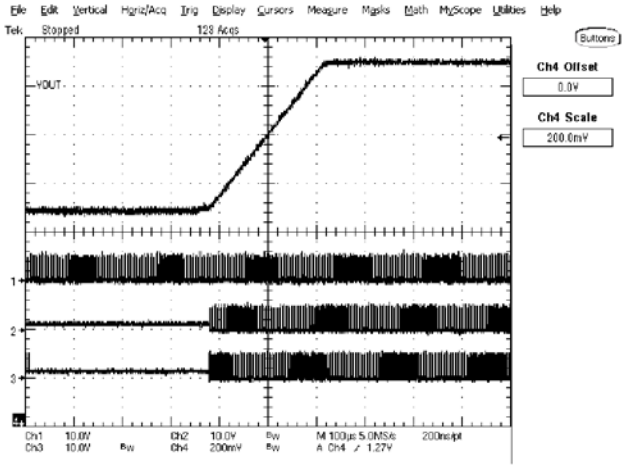


Figure 22. 10 A Load, VID Up, Out of PSI, CH1: PWM1, CH2: PWM2, CH3: PWM3, CH4: VOUT

OVP Improved Performance

The overvoltage protection threshold is not adjustable. OVP protection is enabled as soon as soft−start begins and is disabled when part is disabled. When OVP is tripped, the controller commands all four gate drivers to enable their low side MOSFETs and VR_RDY transitions low. In order to recover from an OVP condition, V_{CC} must fall below the UVLO threshold. See the state diagram for further details. The OVP circuit monitors the output of DIFFOUT. If the DIFFOUT signal reaches 180 mV (typical) above the nominal 1.3 V offset the OVP will trip and VRRDY will be pulled low, after eight consecutive OVP events are detected, all PWMs will be latched. The DIFFOUT signal is the difference between the output voltage and the DAC voltage (minus 19 mV if in VR11.1 modes) plus the 1.3 V internal offset. This results in the OVP tracking on the DAC voltage even during a dynamic change in the VID setting during operation.

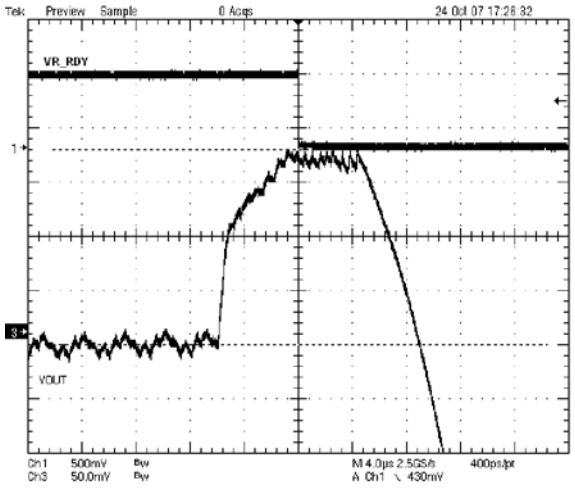


Figure 23. VR11.1, 1.6 V OVP Event

Gate Driver and MOSFET Selection

ON Semiconductor provides the NCP5359 as a companion gate driver IC. The NCP5359 driver is optimized to work with a range of MOSFETs commonly used in CPU applications. The NCP5359 provides special functionality including power saving mode operation and is required for high performance dynamic VID operation. Contact your local ON Semiconductor applications engineer for MOSFET recommendations.

Board Stackup and Board Layout

Close attention should be paid to the routing of the sense traces and control lines that propagate away from the controller IC. Routing should follow the demo board example. For further information or layout review contact ON Semiconductor.

SYSTEM TIMING DIAGRAM

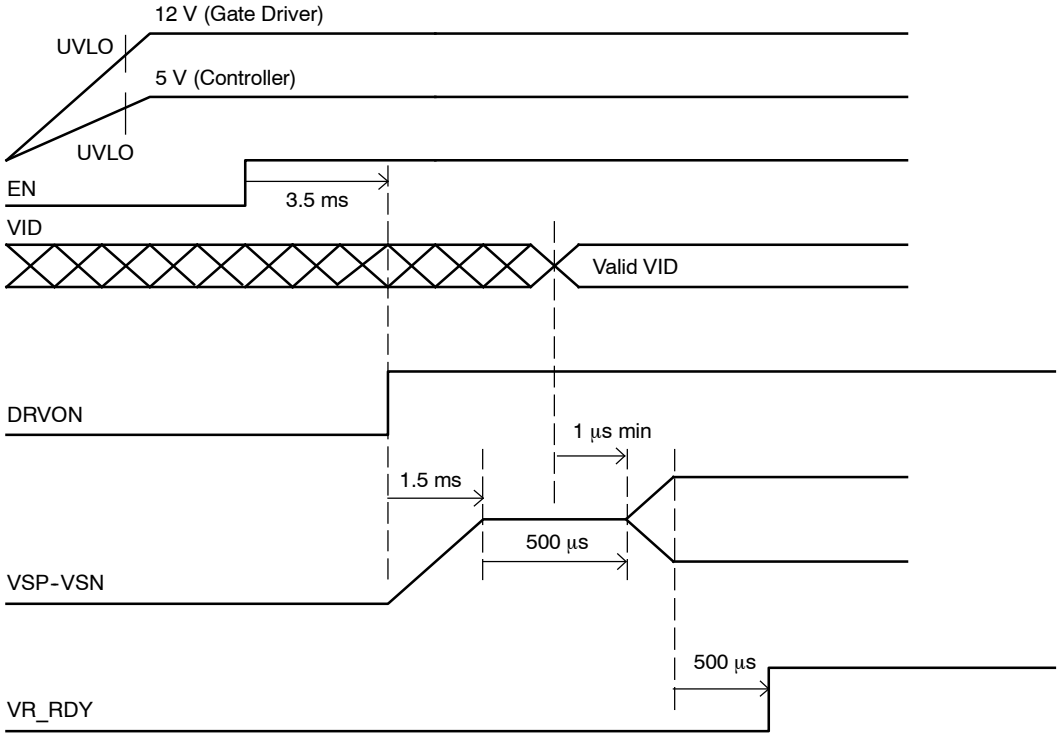


Figure 24. Normal Startup

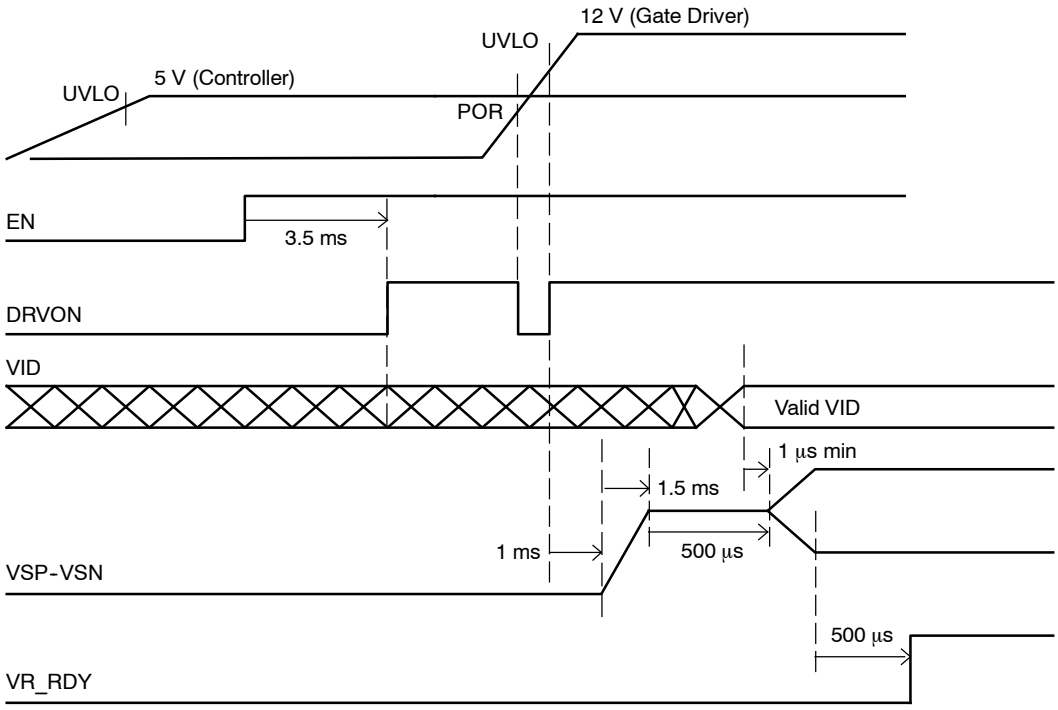


Figure 25. Driver UVLO Limited Startup

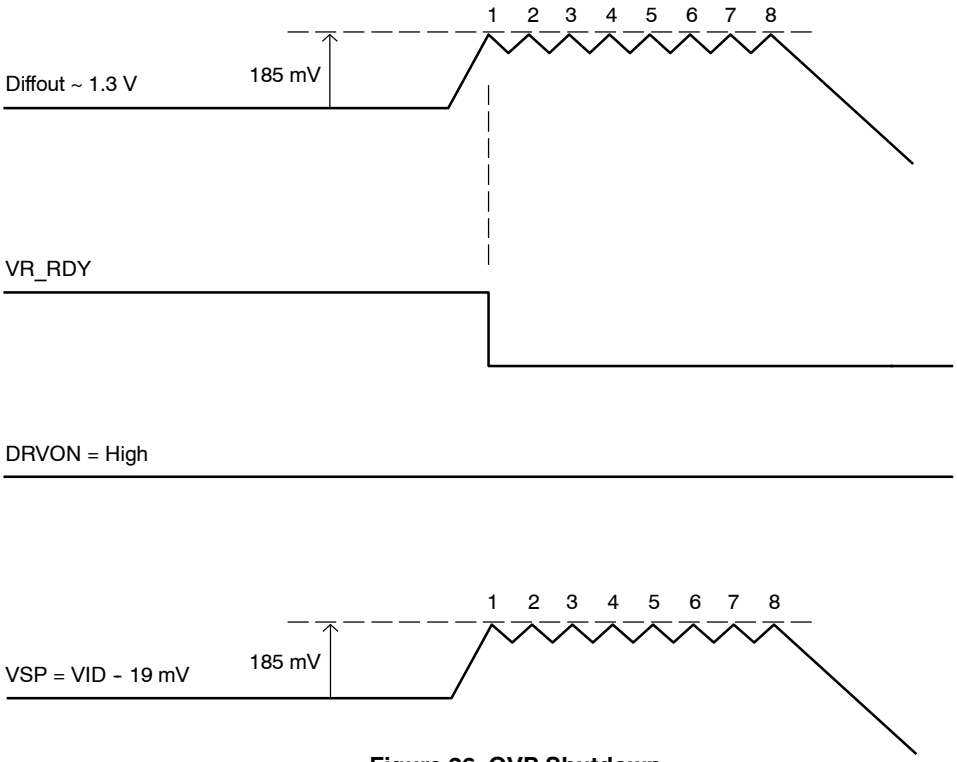


Figure 26. OVP Shutdown

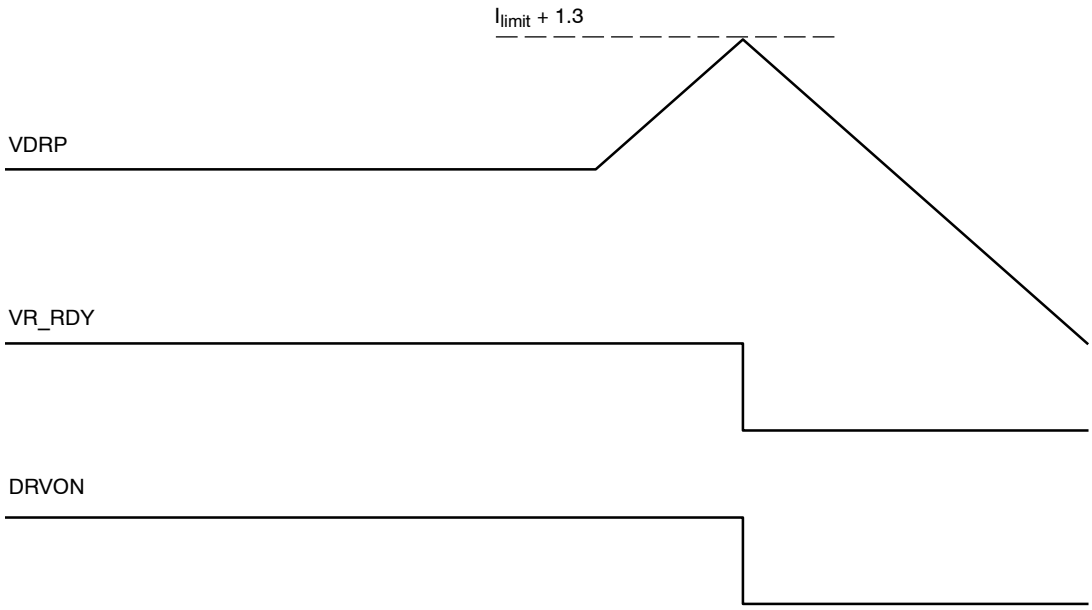


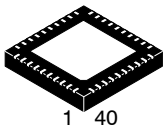
Figure 27. Non−PSI Current Limit

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

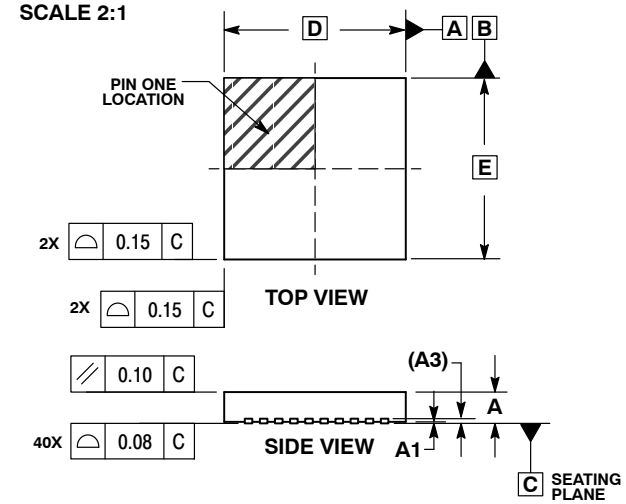
ON Semiconductor®

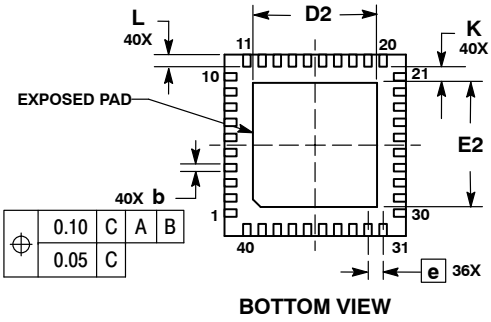
QFN40 6x6, 0.5P
CASE 488AR−01
ISSUE A

DATE 18 APR 2007



SCALE 2:1





BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

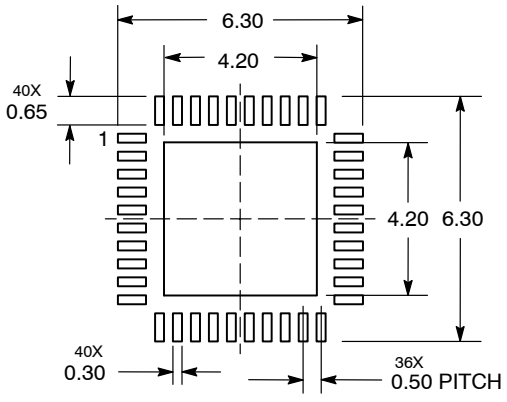
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	4.00	4.20
E	6.00 BSC	
E2	4.00	4.20
e	0.50 BSC	
L	0.30	0.50
K	0.20	−−−

GENERIC MARKING DIAGRAM*

XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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