

NTMFS4108N

Power MOSFET

30 V, 35 A, Single N-Channel,
SO-8 Flat Lead Package

Features

- Thermally and Electrically Enhanced Packaging Compatible with Standard SO-8 Package Footprint
- New Package Provides Capability of Inspection and Probe After Board Mounting
- Ultra Low $R_{DS(on)}$ (at 4.5 V_{GS}), Low Gate Resistance and Low Q_G
- Optimized for Low Side Synchronous Applications
- High Speed Switching Capability
- These are Pb-Free Devices

Applications

- Notebook Computer Vcore Applications
- Network Applications
- DC-DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	30	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	22	A
		T _A = 85°C		16	
	t ≤ 10 s	T _A = 25°C		35	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	2.7	W
	t ≤ 10 s			7.2	
Continuous Drain Current (Note 2)	Steady State	T _A = 25°C	I _D	13.5	A
		T _A = 85°C		10	
Power Dissipation (Note 2)	Steady State	T _A = 25°C	P _D	1.1	W
Power Dissipation R _{θJC} (Note 1)		T _C = 25°C		P _D	
Pulsed Drain Current	t _p = 10 μs		I _{DM}	288	A
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 150	°C
Continuous Source Current (Body Diode)			I _S	6.0	A
Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 30 V, V _{GS} = 10 V, I _{PK} = 30 A, L = 1 mH, R _G = 25 Ω)			E _{AS}	450	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

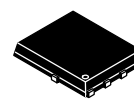
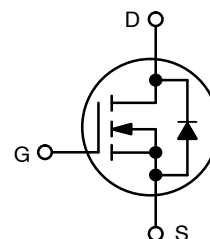
1. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 650 mm² [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 50 mm²).



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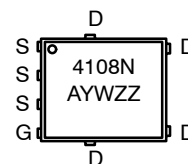
<http://onsemi.com>

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
30 V	1.8 mΩ @ 10 V	35 A
	2.7 mΩ @ 4.5 V	



SO-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



4108N = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4108NT1G	SO-8 FL (Pb-Free)	1500 Tape / Reel
NTMFS4108NT3G	SO-8 FL (Pb-Free)	5000 Tape / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMFS4108N

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Case (Drain Terminal)	$R_{\theta JC}$	1.3	°C/W
Junction-to-Ambient - Steady State (Note 3)	$R_{\theta JA}$	45.7	
Junction-to-Ambient - $t \leq 10$ s (Note 3)	$R_{\theta JA}$	17.3	
Junction-to-Ambient - Steady State (Note 4)	$R_{\theta JA}$	117	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		25	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			7.5		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 19\text{ A}$		2.7	3.4	m Ω
			$V_{GS} = 10\text{ V}, I_D = 21\text{ A}$		1.8	
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		25		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		6000		pF
Output Capacitance	C_{OSS}			1200		
Reverse Transfer Capacitance	C_{RSS}			700		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 24\text{ V}, I_D = 21\text{ A}$		54		nC
Threshold Gate Charge	$Q_{G(TH)}$			11		
Gate-to-Source Charge	Q_{GS}			16		
Gate-to-Drain Charge	Q_{GD}			23		
Gate Resistance	R_G			0.7		

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 1.0\text{ A}, R_G = 6.0\ \Omega$		45		ns
Rise Time	t_r			60		
Turn-Off Delay Time	$t_{d(OFF)}$			70		
Fall Time	t_f			140		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 6.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.72	1.1	V
			$T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 6.0\text{ A}$		41		ns	
Charge Time	t_a			20			
Discharge Time	t_b			21			
Reverse Recovery Charge	Q_{RR}			45			nC

- Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 650 mm² [1 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 50 mm²).
- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

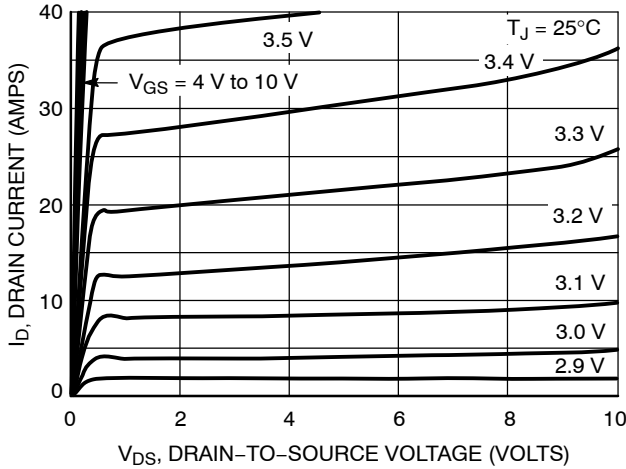


Figure 1. On-Region Characteristics

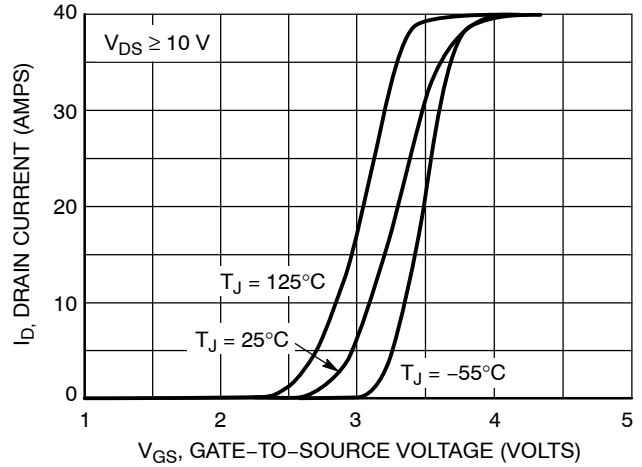


Figure 2. Transfer Characteristics

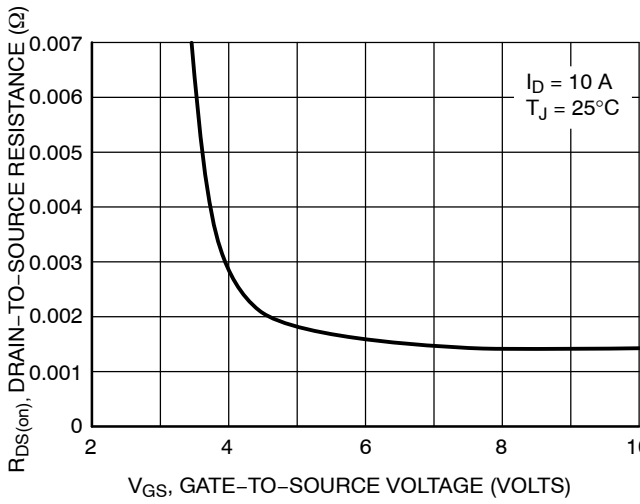


Figure 3. On-Resistance vs. Gate-to-Source Voltage

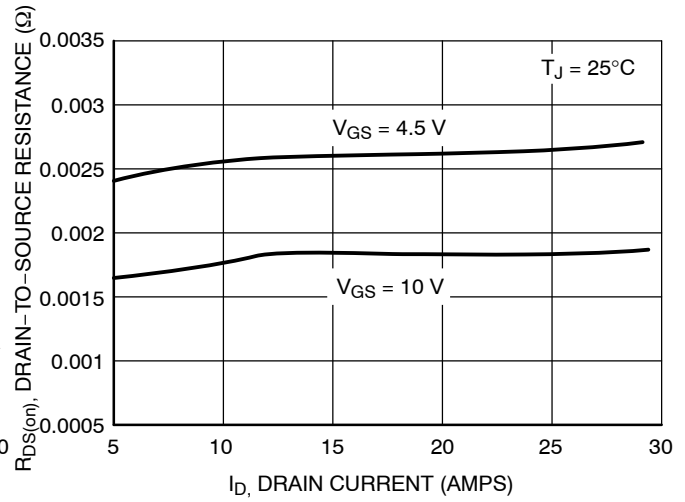


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

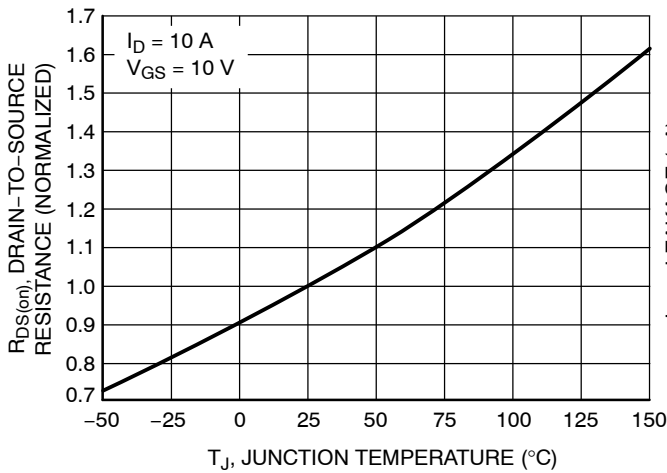


Figure 5. On-Resistance Variation with Temperature

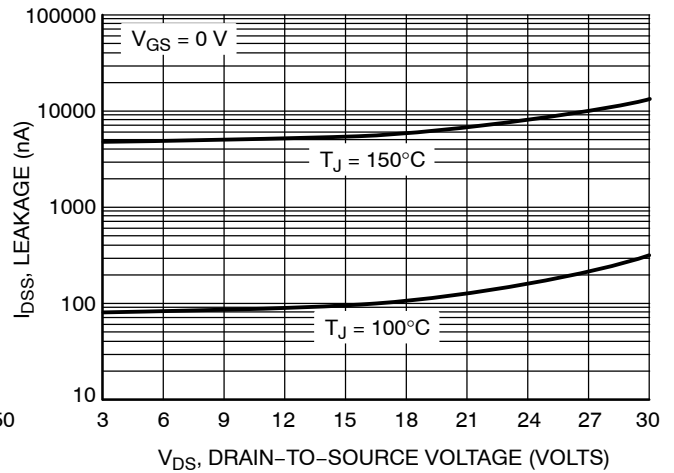


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

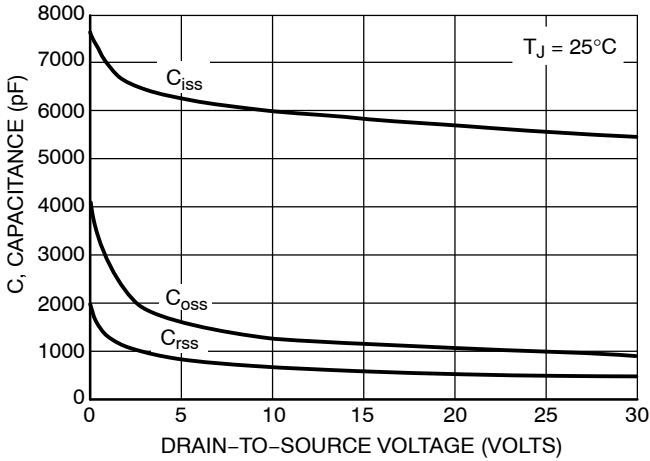


Figure 7. Capacitance Variation

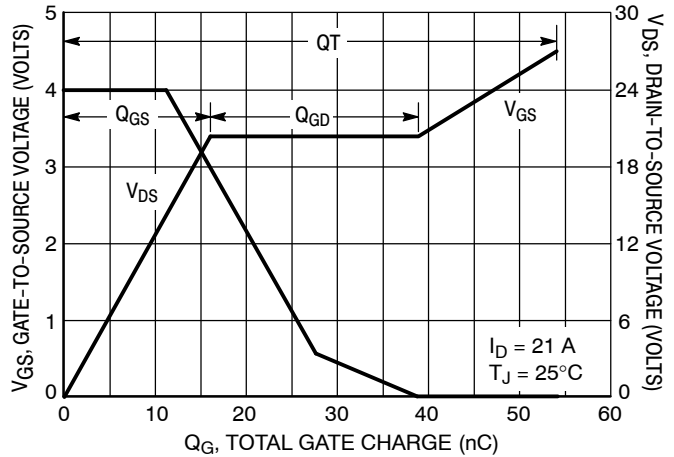


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

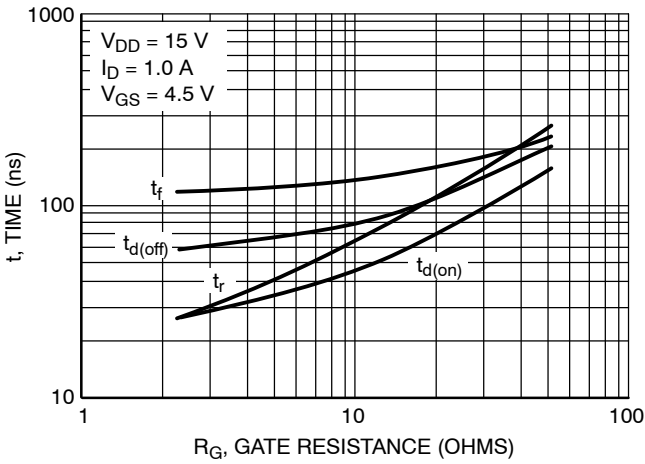


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

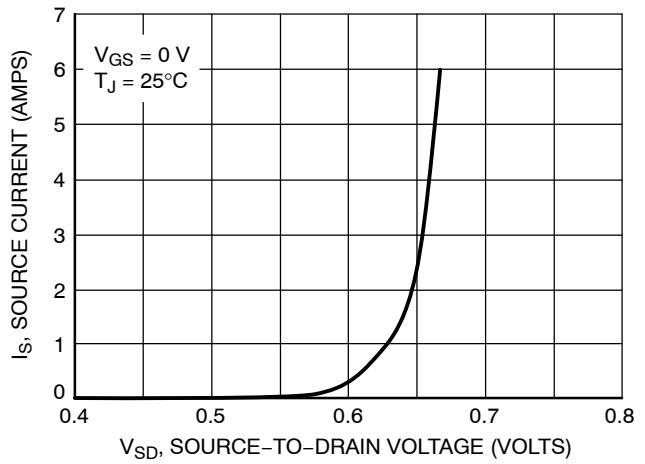


Figure 10. Diode Forward Voltage vs. Current

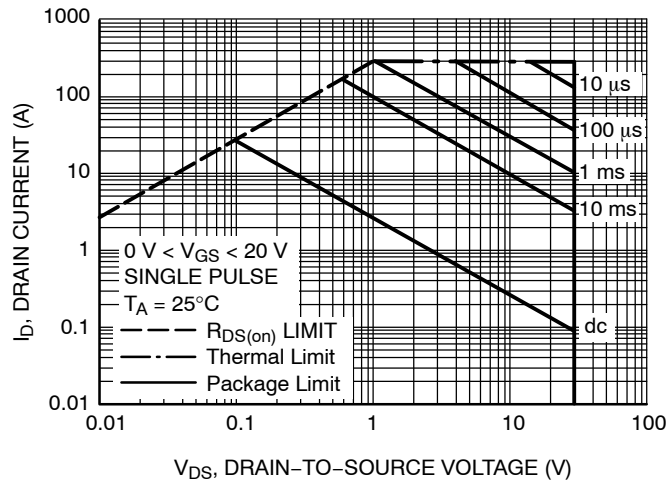


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTMFS4108N

TYPICAL PERFORMANCE CURVES

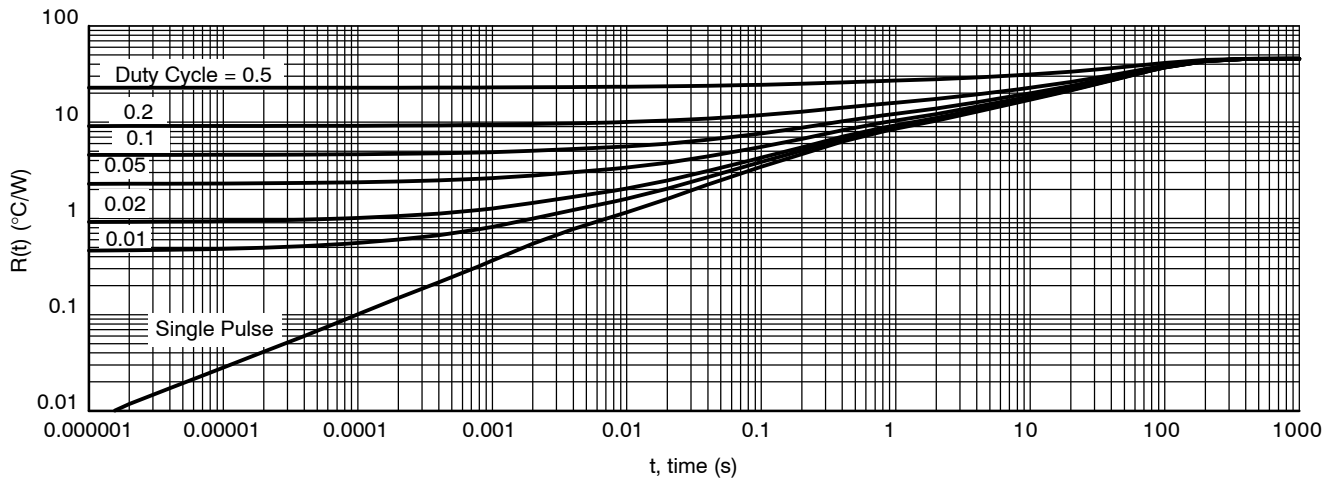


Figure 12. FET Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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