NCP1651

Single Stage Power Factor Controller

The NCP1651 is an active, power factor correction controller that can operate over a wide range of input voltages. It is designed for 50/60 Hz power systems. It is a fixed frequency controller that can operate in continuous or discontinuous conduction modes.

The NCP1651 provides a low cost, low component count solution for isolated AC−DC converters with mid−high output voltage requirements. The NCP1651 eases the task of meeting the IEC1000−3−2 harmonic requirements for converters in the range of 50 W − 250 W.

The NCP1651 drives a flyback converter topology to operate in continuous/discontinuous mode and programs the average input current to follow the line voltage in order to provide unity power factor. By using average current mode control CCM algorithm, the NCP1651 can help provide excellent power factor while limiting the peak primary current. Also, the fixed frequency operation eases the input filter design.

The NCP1651 uses a proprietary multiplier design that allows for much more accurate operation than with conventional analog multipliers.

Features

- Fixed Frequency Operation
- Average Current Mode PWM
- Internal High Voltage Startup Circuit
- Continuous or Discontinuous Mode Operation
- High Accuracy Multiplier
- Overtemperature Shutdown
- External Shutdown
- Undervoltage Lockout
- Low Cost/Parts Count Solution
- Ramp Compensation Does Not Affect Oscillator Accuracy
- This is a Pb−Free Device

Typical Applications

- High Current Battery Chargers
- Front Ends for Distributed Power Systems

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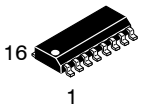
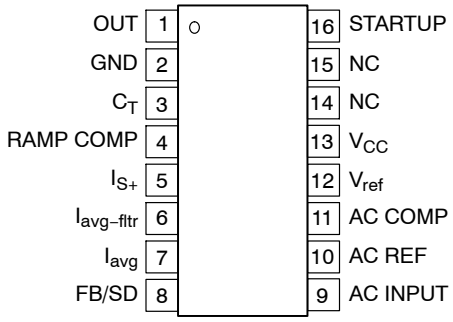
MARKING DIAGRAM



SOIC−16
D SUFFIX
CASE 751B

A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1651DR2G	SOIC−16 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Output	Drive output for power FET or IGBT. Capable of driving small devices, or can be connected to an external driver for larger transistors.
2	Ground	Ground reference for the circuit.
3	C_T	Timing capacitor for the internal oscillator. This capacitor adjusts the oscillator frequency.
4	Ramp Compensation	This pin biases the ramp compensation circuit, to adjust the amount of compensation that is added to the current signal for stability purposes.
5	I_{S+}	Positive current sense input. Designed to connect to the positive side of the current shunt.
6	$I_{avg-fltr}$	A capacitor connected to this pin filters the high frequency component from the instantaneous current waveform, to create a waveform that resembles the average line current.
7	I_{avg}	An external resistor with a low temperature coefficient is connected from this terminal to ground, to set and stabilize the gain of the Current Sense Amplifier output that drives the AC error amplifier.
8	Feedback/ Shutdown	The error signal from the error amplifier circuit is fed via an optocoupler or other isolation circuit, to this pin. A shutdown circuit is also connected to this pin which will put the unit into a low power shutdown mode if this voltage is reduced to less than 0.6 volts.
9	AC Input	The fullwave rectified sinewave input is connected to this pin. This information is used for the reference comparator and the average current compensation circuit.
10	AC Reference	A capacitor is connected to this pin to filter the modulated output of the reference multiplier.
11	AC Compensation	Provides pole for the AC Reference Amplifier. This amplifier compares the sum of the AC input voltage and the low frequency component of the input current to the reference signal. The response must be slow enough to filter out most of the high frequency content of the current signal that is injected from the current sense amplifier, but fast enough to cause minimal distortion to the line frequency information.
12	Vref	6.5 volt regulated reference output.
13	V_{CC}	Provides power to the device. This pin is monitored for undervoltage and the unit will not operate if the V_{CC} voltage is not within the UVLO range. Initial power is supplied to this pin via the high voltage startup network.
14	No Connection	This pin is not available due to spacing considerations of the startup pin.
15	No Connection	This pin is not available due to spacing considerations of the startup pin.
16	Startup	This pin connects to the rectified input signal and provides current to the internal bias circuitry for the startup period of operation.

NOTE: Pins 14 and 15 have not been used for clearance considerations due to the potential voltages present on pin 16. In order to maintain proper spacing between the high voltage and low voltage pins, traces should not be placed on the circuit board between pins 16 and 13.

MAXIMUM RATINGS (Maximum ratings are those that, if exceeded, may cause damage to the device. Electrical Characteristics are not guaranteed over this range.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Operating) Output (Pin 1)	V_{CC}	−0.3 to 18	V
Current Sense Amplifier Input (Pin 5)	$V(I_S+)$	−0.3 to 1.0	V
FB/SD Input (Pin 8)	$V_{FB/SD}$	−0.3 to 11	V
C_T Input (Pin 3)	V_{CT}	−0.3 to 4.5	V
Line Voltage	$V_{startup}$	−0.3 to 500	V
All Other Pins		−0.3 to 6.5	V
Thermal Resistance, Junction−to−Air 0.1 in^2 Copper 0.5 in^2 Copper	θ_{JA}	 130 110	°C/W
Thermal Resistance, Junction−to−Lead	θ_{JL}	50	°C/W
Maximum Power Dissipation @ T_A = 25°C	Pmax	0.77	W
Operating Temperature Range	T_j	−40 to 125	°C
Non−operating Temperature Range	T_j	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1−6: Human Body Model 2000 V per JEDEC Standard JESD22, Method A114E.
   Machine Model Method 200 V per JEDEC Standard JESD22, Method A115A.
   Pin 8 is the HV startup to the device and is rated to the maximum rating of the part, or 500 V.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 14 volts, C_T = 470 pF, C_{12} = 0.1 μF, T_j = 25°C for typical values. For min/max values T_j is the applicable junction temperature.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency T_j = −40°C to +125°C	F_{osc}	90	100	110	kHz
Frequency Range (Note 2)	–	25	–	250	kHz
Max Duty Cycle	dmax	0.95	–	–	–
Ramp Peak (Note 2)	V_{Rpeak}	–	4.0	–	V
Ramp Valley (Note 2)	$V_{Rvalley}$	–	0.100	–	V
Ramp Compensation Peak Voltage (Pin 4) (Note 2)	–	–	4.0	–	V
Ramp Compensation Current (Pin 4) (Note 2)	–	–	150	–	μA
AC ERROR AMPLIFIER (V_{comp} = 2.0 V)					
Input Offset Voltage	V_{IO}	–	20	–	mV
Transconductance	g_m	75	100	150	umho
Output Source	$I_{Osource}$	25	70	–	μA
Output Sink	I_{Osink}	−25	−70	–	μA
CURRENT AMPLIFIER					
Input Bias Current (Pin 5)	I_{bias}	40	60	80	μA
Input Offset Voltage (V_{comp} = 2.0) T_j = −40°C to +85°C T_j = −40°C to +125°C	VIO	0 0	3.0 3.0	10 20	mV
Current Limit Threshold	I_{LIMthr}	0.715	–	0.79	V
Output Gain (150 μA/0.150 V) (Voltage Loop Outputs)	–	–	1000	–	umho
Output Gain (150 μA/0.150 V) (AC E/A Output) (R_{10} = 15 kΩ)	–	–	1000	–	umho
Leading Edge Blanking Pulse (Note 2)	t_{LEB}	–	200	–	ns
Bandwidth (Note 2)	–	–	1.5	–	MHz
PWM Output Voltage Gain ($k = V_{PWM+} / (V_{sense+} - V_{sense-})$) ($V_{pin\ 3} = V_{pin\ 13} = 0$)	Av	4.0	5.0	6.0	V/V
Current Limit Voltage Gain ($k = Vac_{e/a-} / (V_{sense+} - V_{sense-})$) ($V_{pin5}9 = 0$) (R7 = 15 k)	Av	8.0	10	12	V/V
AVERAGE CURRENT COMPENSATION AMPLIFIER					
Voltage Gain	Av	–	0.75	–	V/V
REFERENCE MULTIPLIER					
Dynamic Input Voltage Range Ac Input (p−input) (Note 2) Offset Voltage (a−input)	V_{max}	 – –	 3.50 1.0	 – –	V
Multiplier Gain $k = \frac{V_{mult\ out}}{(V_{AC}/V_{ramp\ pk}) \times (V_{LOOPcomp} - V_{offset})}$ (Note 2)	k	–	7.5	–	–
AC INPUT (Pin 5)					
Input Bias Current (Total bias current for reference multiplier and current compensation amplifier) (Note 2)	I_{INbias}	–	0.01	–	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Verified by design.

ELECTRICAL CHARACTERISTICS (continued) (Unless otherwise noted: V_{CC} = 14 volts, C_T = 470 pF, C_{12} = 0.1 μF, T_j = 25°C for typical values. For min/max values T_j is the applicable junction temperature.)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVE OUTPUT					
Source Resistance (1.0 Volt Drop)	R_{source}	–	8.0	15	Ω
Sink Resistance (1.0 Volt Drop)	R_{sink}	–	8.0	15	Ω
Rise Time (C_L = 1.0 nF)	t_r	–	50	–	ns
Fall Time (C_L = 1.0 nF)	t_f	–	50	–	ns
Output Voltage in UVLO Condition (Drive out = 100 μA in, 1 nF load)	$V_{O(UV)}$	–	1.0	10	mV
VOLTAGE REFERENCE					
Buffered Output (I_{load} = 0 mA, V_{CC} = 12 VDC, Temperature)	$Vref_{OUT}$	6.24	6.50	6.76	V
Load Regulation (Buffered Output, Io = 0 to 10 mA, $V_{CC} \geq$ 10 V)	$DVref_{OUT}$	0	–	40	mV
FB/SD PIN					
Opto Current Source (Unit Operational, V_{FB} = 0.5 V)	I_{OPTO}	0.8	1.1	1.4	mA
Opto Current Source (Shutdown, V_{FB} = 0.1 V)	–	15	20	25	μA
Input Voltage for 0 Duty Cycle (Note 3)	–	1.5	–	–	–
Input Voltage for 95% Duty Cycle (Note 3)	–	–	–	4.0	V
Open Circuit Voltage (Device Operational) (Note 3)	V_{OC}	–	–	12	V
Clamp Voltage (Device in Shutdown Mode) (Note 3)	V_{CL}	0.9	1.5	1.6	V
Shutdown Start Up Threshold (Pin 8) (V_{out} Increasing)	V_{SD}	0.40	0.60	0.70	V
Shutdown Hysteresis (Pin 8)	V_H	30	75	130	mV
STARTUP/UVLO					
UVLO Startup Threshold (V_{CC} Increasing)	V_{SU}	10	10.75	11.5	V
UVLO Hysteresis (Shutdown Voltage = $V_{SU} - V_H$)	V_H	0.8	1.0	1.2	V
Overtemperature Trip Point (Note 3)	T_{SD}	140	160	180	°C
Overtemperature Hysteresis (Note 3)	–	–	30	–	°C
HIGH VOLTAGE STARTUP (Pin 16 = 50 V)					
Startup Current (out of pin 13) (V_{CC} = UVLO – 0.2 V)	I_{SU}	3.0	5.5	8.0	mA
Startup Current (out of pin 13) (V_{CC} = 0 V)		5.0	8.5	12	mA
Min. Startup Voltage (pin 16, pin 13 current = 1 mA)	V_{SU}	–	17	20	V
Line Pin Leakage (pin 16, Startup Circuit Inhibited) (V_{DS} = 400 V, T_A = +25°C) T_A = +125°C	I_{leak}	 – –	 25 15	 40 80	μA
TOTAL DEVICE					
Operational Bias Current ($C_{L(Driver)}$ = 1.0 nF, f_{osc} = 100 kHz)	I_{BIAS}	–	4.0	5.0	mA
Bias Current in Undervoltage Mode	$I_{Bshutdown}$	–	0.75	1.2	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Verified by design.

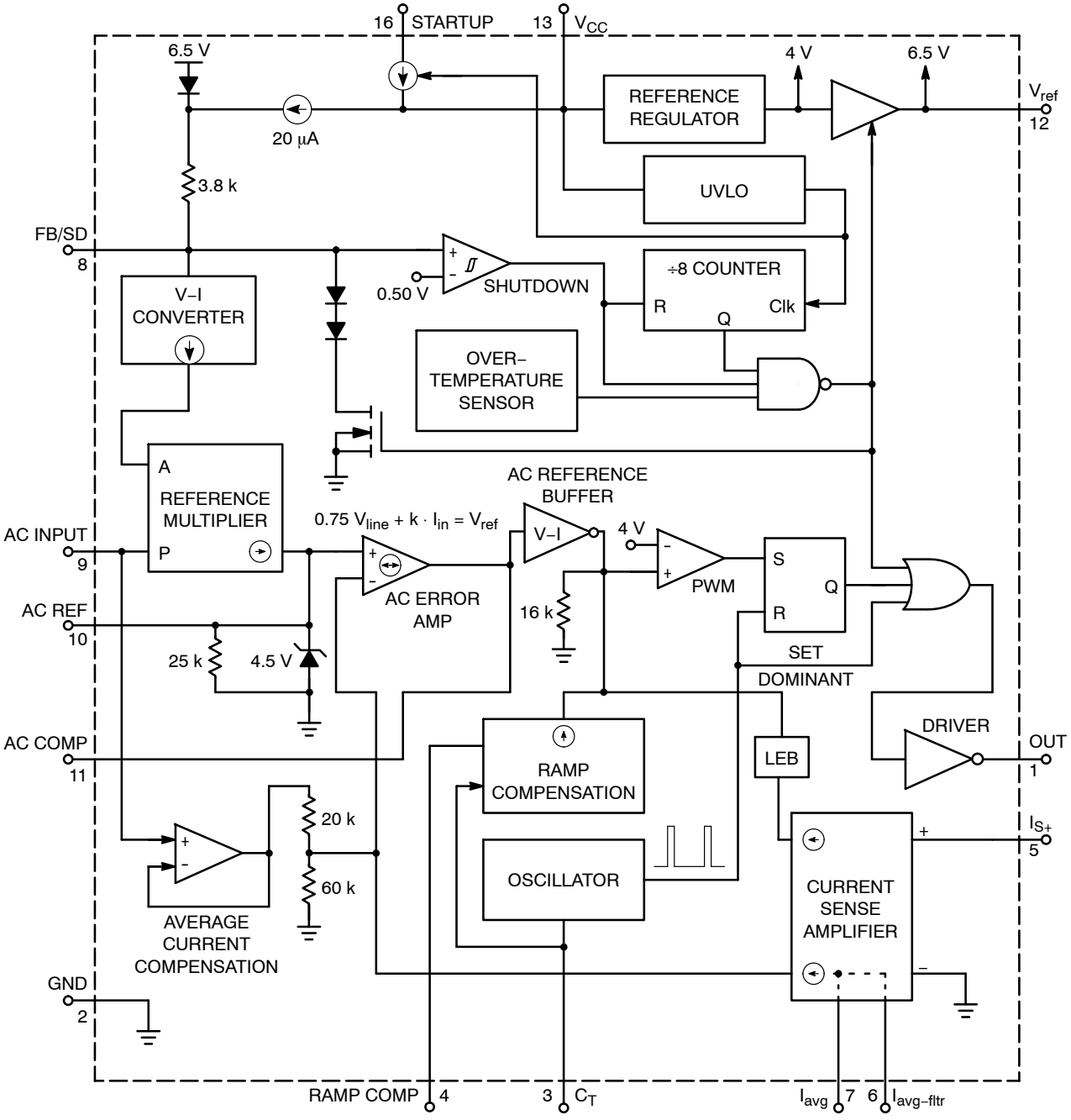


Figure 1. Block Diagram

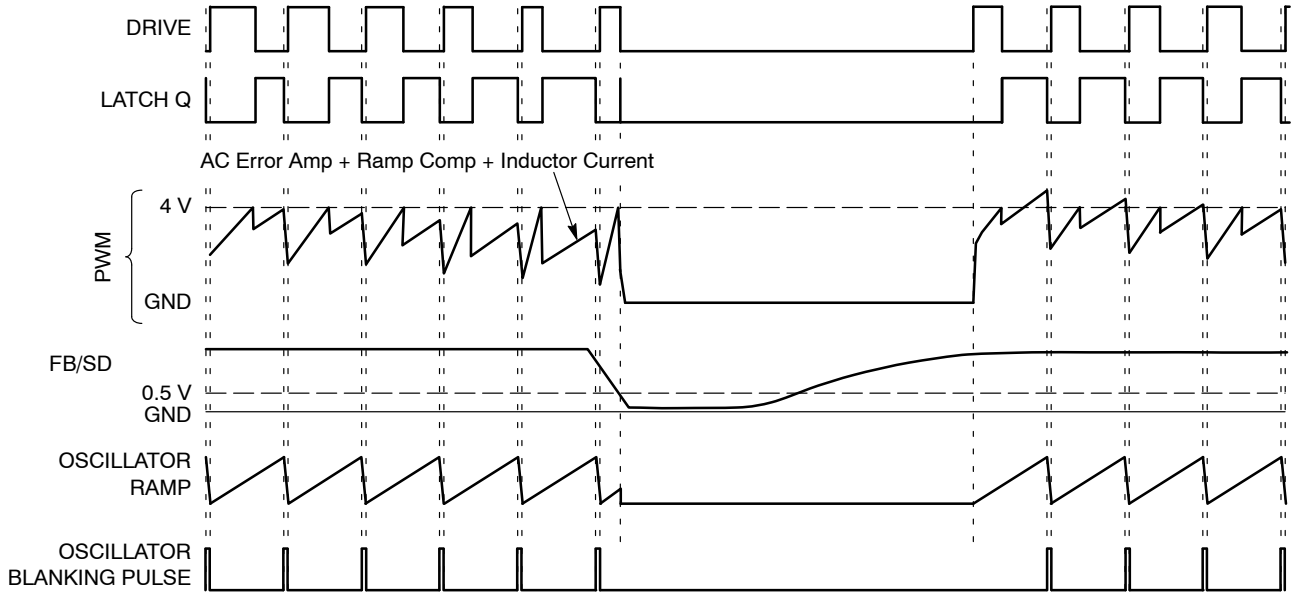


Figure 2. Switching Timing Diagram

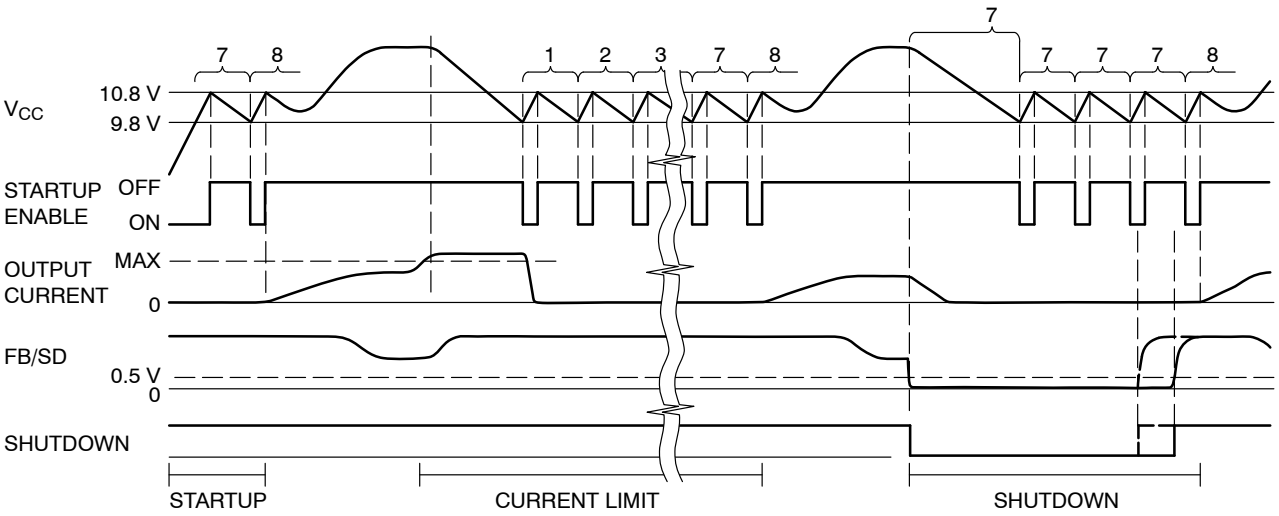


Figure 3. Divide−by−Eight Counter Timing Diagram

Typical Performance Characteristics

(Test circuits are located in the document TND308/D)

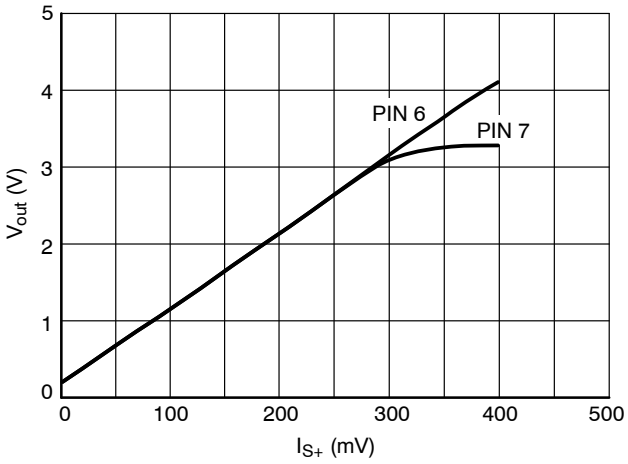


Figure 4. Current Sense Amplifier Gain

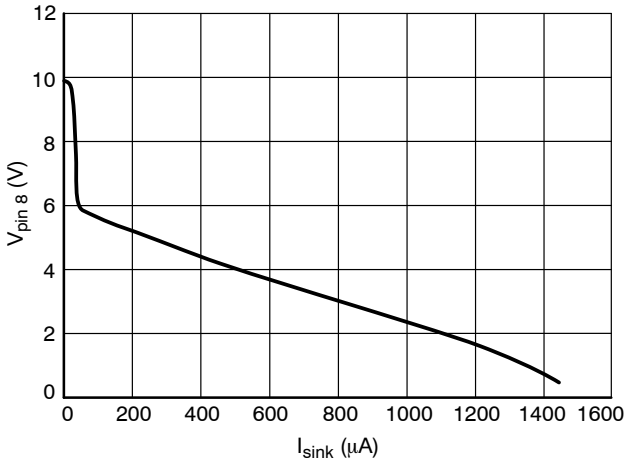


Figure 5. FB/SD V−I Characteristics

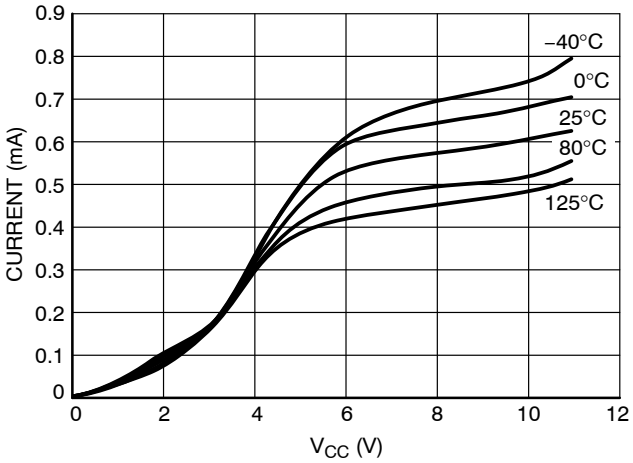


Figure 6. Bias Current in Shutdown Mode

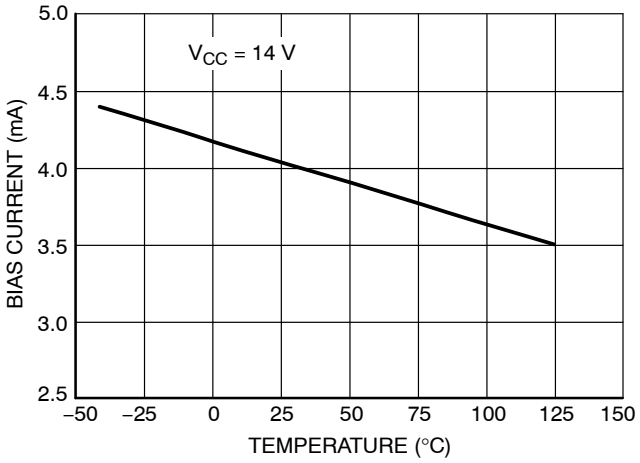


Figure 7. Bias Current in Operating Mode

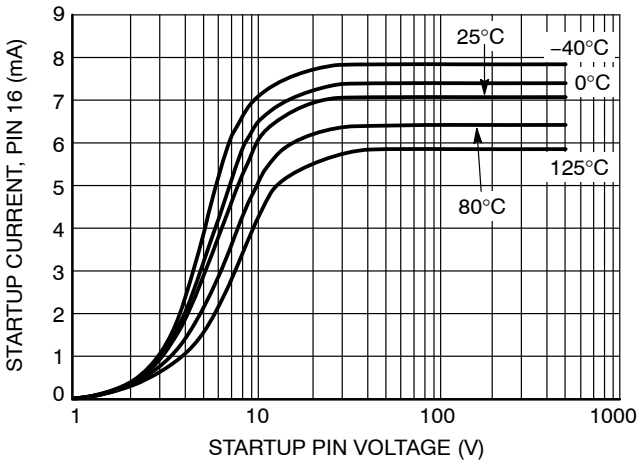


Figure 8. Startup Current versus High Voltage

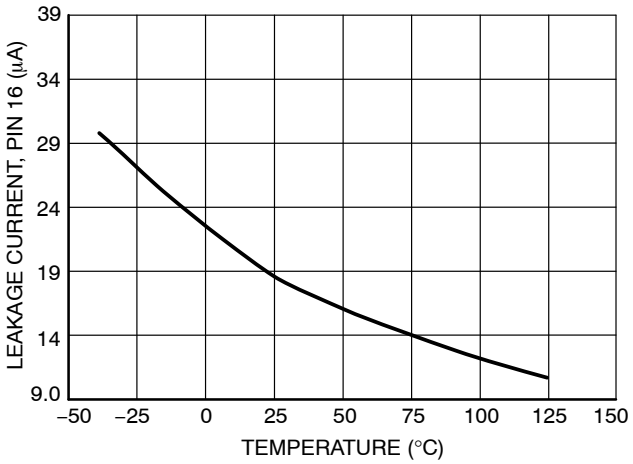


Figure 9. Startup Leakage versus Temperature

Typical Performance Characteristics

(Test circuits are located in the document TND308/D)

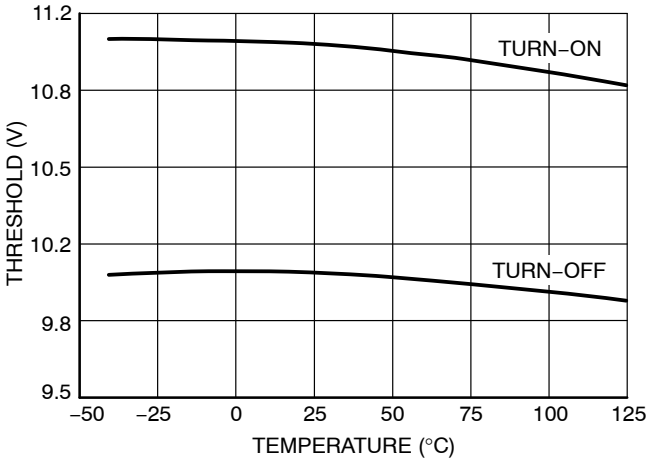


Figure 10. UVLO versus Temperature

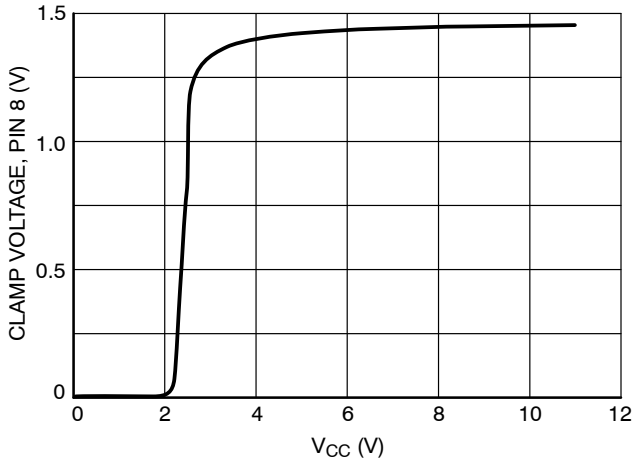


Figure 11. FB/SD Clamp Voltage versus V_{CC}

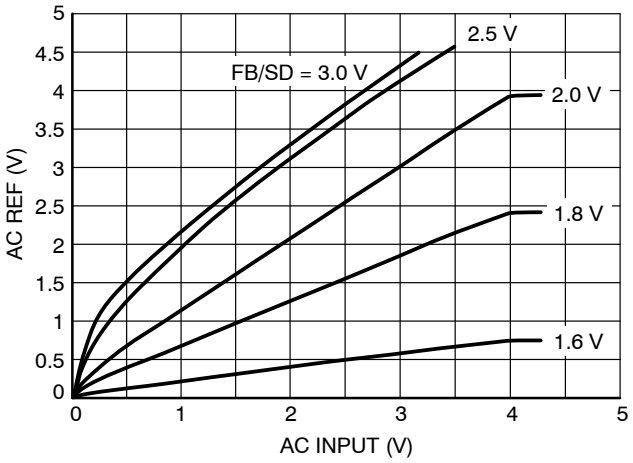


Figure 12. Reference Multiplier Gain

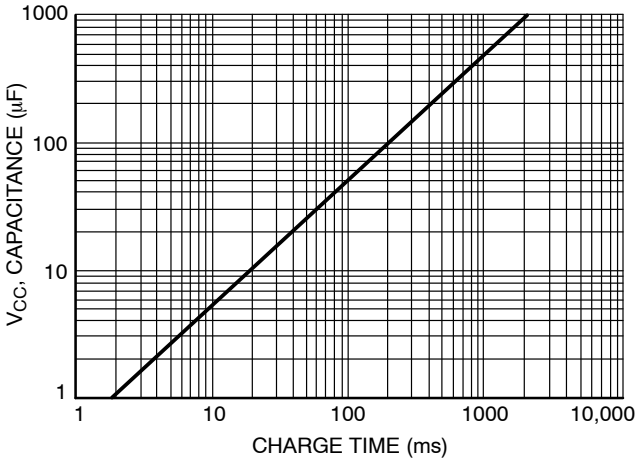


Figure 13. V_{CC} Cap Charge Time

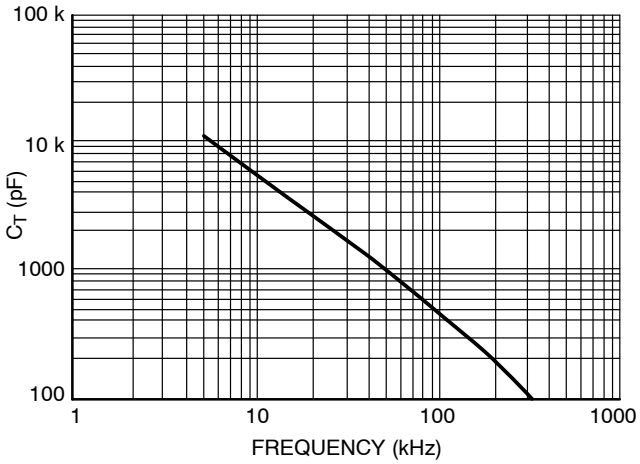


Figure 14. C_T versus Frequency

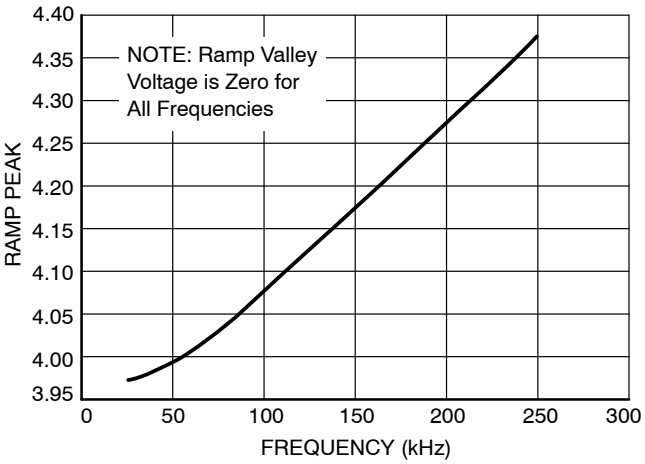


Figure 15. Ramp Peak versus Frequency

Typical Performance Characteristics

(Test circuits are located in the document TND308/D)

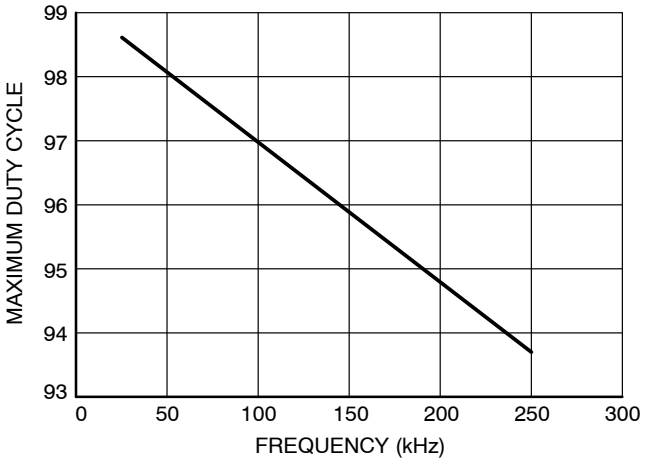


Figure 16. Maximum Duty Cycle versus Frequency

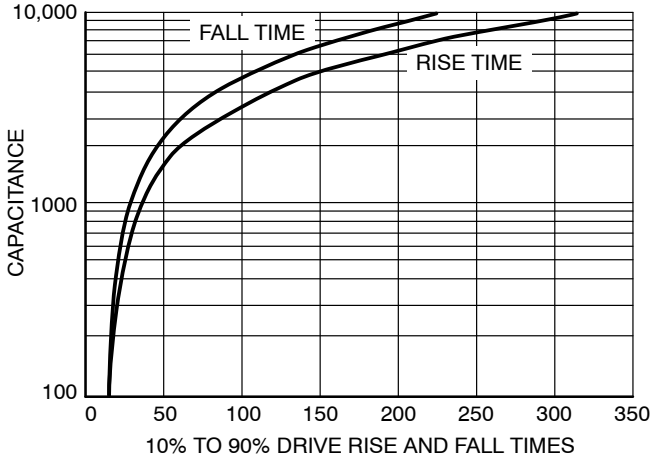


Figure 17. Capacitance versus 10% to 90% Drive Rise and Fall Times

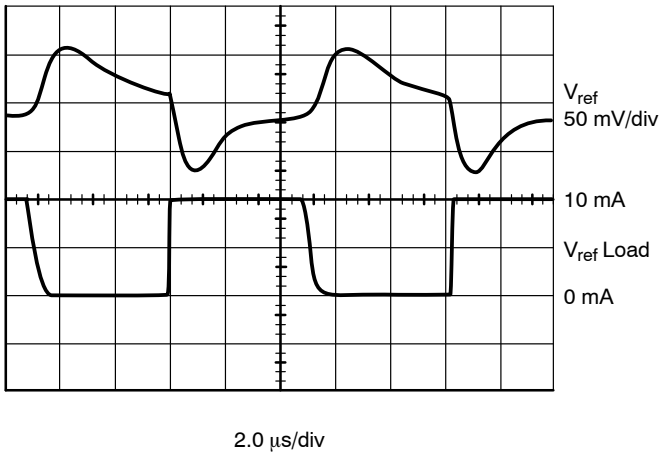


Figure 18. Transient Response for 6.5 Volt Reference

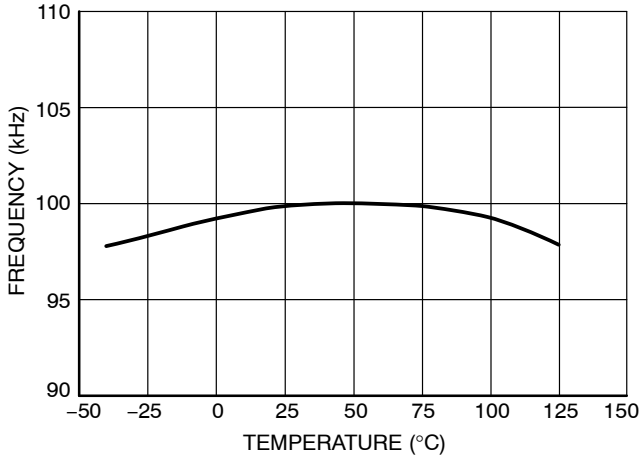


Figure 19. Frequency versus Temperature

Typical Performance Characteristics

(Test circuits are located in the document TND308/D)

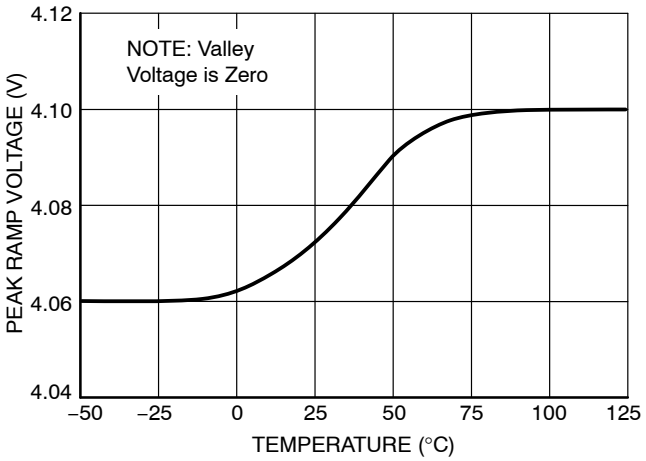


Figure 20. Peak Ramp Voltage versus Temperature

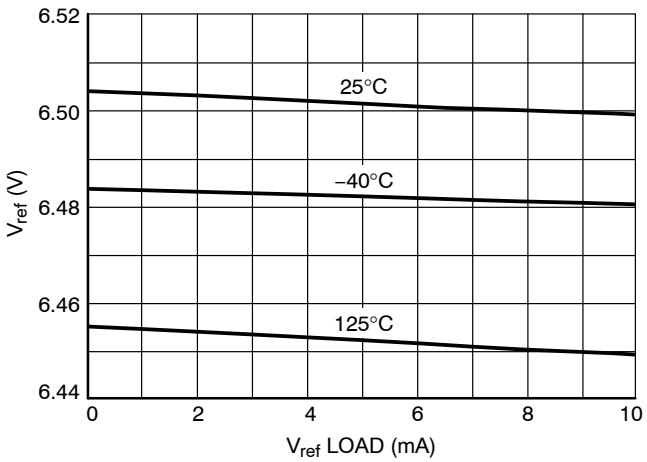


Figure 21. V_{ref} Load Regulation

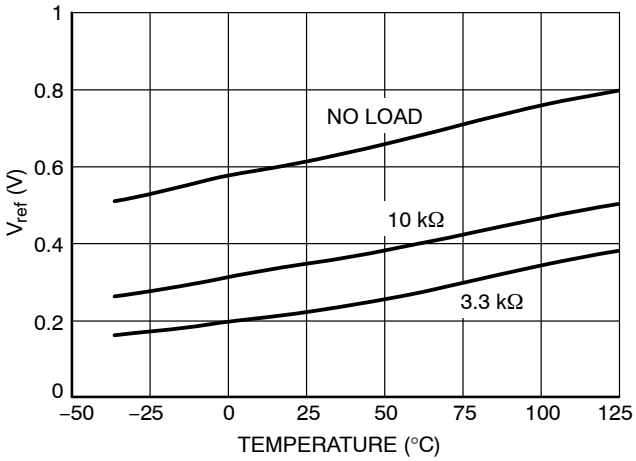
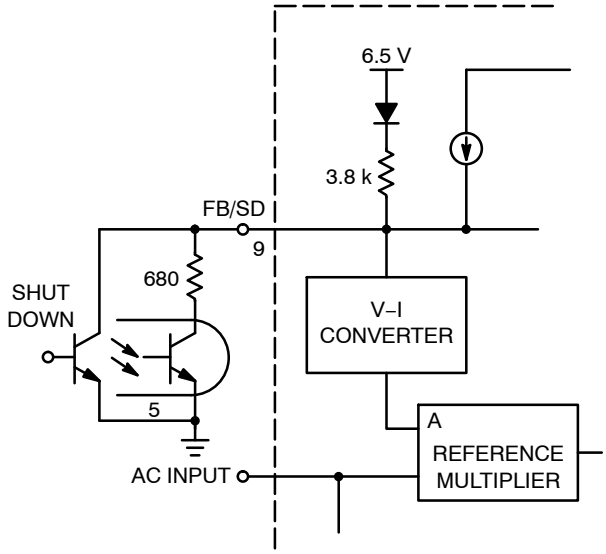


Figure 22. V_{ref} in Shutdown Condition



(Allows external converters to be synchronized to the switching frequency of this unit.)

Figure 23. External Shutdown Circuit

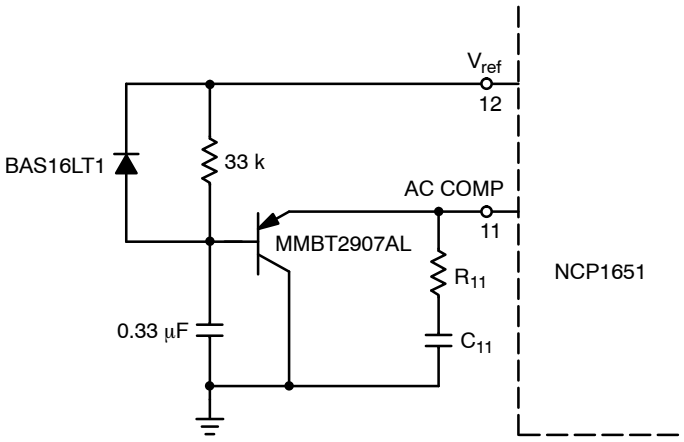


Figure 24. Soft–Start Circuit

THEORY OF OPERATION

Introduction

Optimizing the power factor of units operating off of AC lines is becoming more and more important. There are a number of reasons for this.

There are a growing number of government regulations requiring Power Factor Correction PFC. Many of these are originating in Europe. Regulations such as IEC1000−3−2 are forcing equipment to utilize input stages with topologies other than a simple off−line front end which contains a bridge rectifier and capacitor.

There are also system requirements that dictate the use of PFC. In order to obtain the maximum power from an existing circuit in a building, the power factor is very critical. The real power available from such a circuit is:

$$P_{real} = V_{rms} \times I_{rms} \times PF$$

A typical off−line converter will have a power factor of 0.5 to 0.6, which means that for a given circuit breaker rating only 50% to 60% of the maximum power is available. If the power factor is increased to unity, the maximum available power can be obtained.

There is a similar situation in aircraft systems, where a limited supply of power is available from the on−board generators. Increasing the power factor will increase the load on the aircraft without the need for a larger generator.

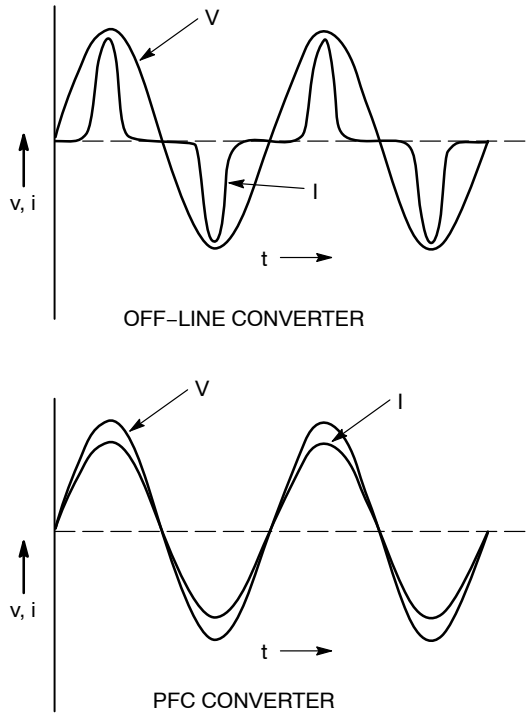


Figure 25. Voltage and Current Waveforms

Unity power factor is defined as the current waveform being in phase with the voltage, and undistorted. Therefore, there are two causes of power factor degradation – phase shift and distortion. Phase shift is normally caused by reactive loads such as motors which are inductive, or electroluminescent lighting which is highly capacitive. In such a case the power factor is relatively simple to analyze, and is determined by the phase shift.

$$PF = \cos\theta$$

Where θ is the phase angle between the voltage and the current.

Reduced power factor due to distortion is more complicated to analyze and is normally measured with AC analyzers, although most circuit simulation programs can also calculate power factor. One of the major causes of distortion is rectification of the line into a capacitive filter. This causes current spikes that do not follow the input voltage waveform. An example of this type of waveform is shown in the upper diagram in Figure 25.

A power converter with PFC forces the current to follow the input waveform. This reduces the peak current, the rms current and eliminates any phase shift.

In most modern PFC circuits, to lower the input current harmonics, and improve the input power factor, designers have historically used a boost topology. The boost topology can operate in the Continuous (CCM), Discontinuous (DCM), or Critical Conduction Mode.

Most PFC applications using the boost topology are designed to use the universal input ac power 85−265 Vac, 50 or 60 Hz, and provide a regulated DC bus (typically 400 Vdc). In most applications, the load can not operate off the high voltage DC bus, so a DC−DC converter is used to provide isolation between the AC source and load, and provide a low voltage output. The advantages to this system configuration are, low THD, a power factor close to unity, excellent voltage regulation, and transient response on the isolated DC output. The major disadvantage of the boost topology is that two power stages are required which lowers the systems efficiency, increases components count, cost, and increases the size of the power supply.

ON Semiconductor's NCP1651 offers a unique alternative for Power Factor Correction designs, where the NCP1651 has been designed to control a PFC circuit operating in a flyback topology. There are several major advantages to using the flyback topology. First, the user can create a low voltage isolated secondary output, with a single power stage, and still achieve a low input current distortion, and a power factor close to unity. A second advantage, compared to the boost topology with a DC−DC converter, is a lower component count which reduces the size and the cost of the power supply.

The NCP1651 can operate in either the Continuous or Discontinuous Mode of operation, the following analysis will help to highlight the advantages of Continuous versus Discontinuous Mode of operation.

If we look at a single application and compare the results.

P_O = 90 watts

Vin = 85−265 V_{rms} (analyzed at 85 V_{rms} input)

Efficiency = 80%

P_{in} = 108 W

V_O = 48 Vdc

Freq = 100 kHz

Transformer turns ration N = 4

Continuous Mode (CCM)

To force the inductor current to be continuous over the majority of the input voltage range (85−265 Vac), L_P needs to be at least 1 mH. Figure 26 shows the typical current through the windings of the flyback transformer. During switch on period, this current flows in the primary and during the switch off time it flows in the secondary.

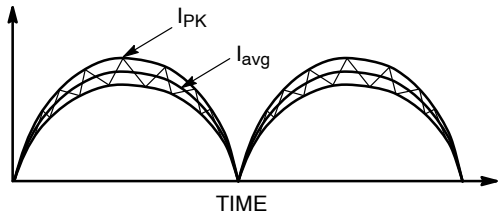


Figure 26.

The peak current is:

$I_{PK} = I_{avg} + ((1.414 \cdot V_{in} \sin \theta \cdot t_{on} \cdot 2)/L_P)$

where $I_{avg} = 1.414 \cdot P_{in}/V_{in} \sin \theta$

$T_{on} = T/((N_S/N_P \cdot 1.414 \cdot V_{in} \sin \theta /V_O) +1)$

T_{on} = 6.19 μs

$I_{PK} = (1.414 \cdot 113)/85 \sin \theta + (1.414 \cdot 85 \cdot 6.15\ \mu s \cdot 2)\ /1$ mH = 3.35 A

Discontinuous Mode (DCM)

In the discontinuous mode of operation, the inductor current falls to zero prior to the end of the switching period as shown in Figure 27.

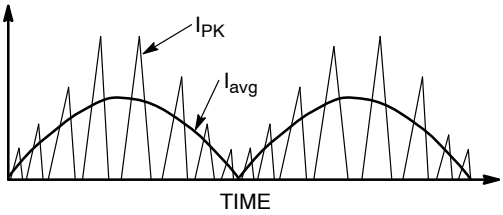


Figure 27.

To ensure DCM, LP needs to be reduced to approximately 100 μH.

$I_{PK} = (V_{in} \sin \theta \cdot 1.414 \cdot t_{on})/L_P$

$I_{PK} = 1.414 \cdot 85 \sin 90 \cdot 5.18\ \mu s/100\ \mu H$ = 6.23 A

The results show that the peak current for a flyback converter operating in the Continuous Conduction Mode is one half the peak current of a flyback converter operating in the Discontinuous Conduction Mode.

Continuous Conduction Mode

A second result of running in DCM can be higher input current distortion, EMI, and a lower Power Factor, in comparison to CCM. While the higher peak current can be filtered to produce the same performance result, it will require a larger filter.

A simple Fast Fourier Transform (FFT) was run in Spice to provide a comparison between the harmonic current levels for CCM and DCM. The harmonic current levels will affect the size of the input EMI filter which in some applications are required to meet the levels of C.I.S.P.R. In the SPICE FFT model we did not add any front end filtering so the result of the analysis could be compared directly.

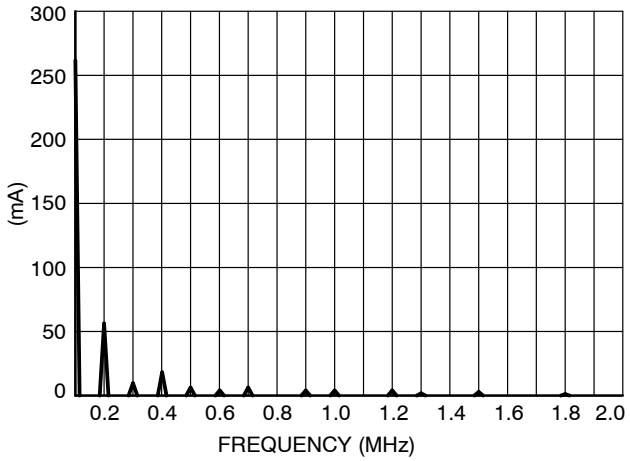


Figure 28. Continuous Conduction Mode

At the 100 kHz switching frequency, the rms value from the FFT is 260 mA, and the 2nd harmonic (200 kHz) is 55 mA rms.

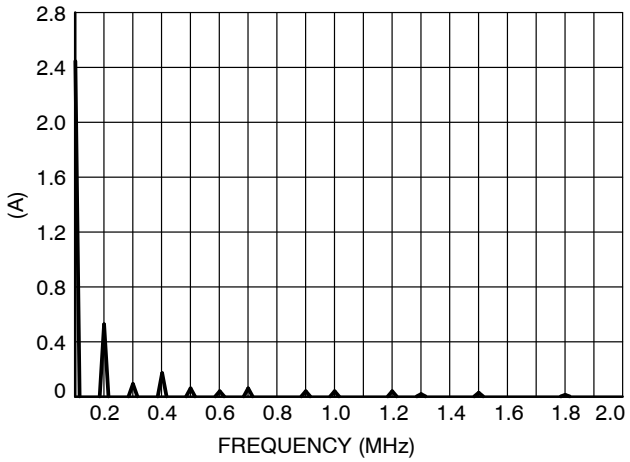


Figure 29. Discontinuous Conduction Mode

At 100 kHz the rms value from the FFT are 2.8 A, and the 2nd harmonic (200 kHz) is 500 mA rms.

Results

It is clear from the result of our analysis that a flyback PFC converter operating in CCM has half the peak current and one tenth the fundamental (100 kHz) harmonic current compared to a flyback PFC converter operating in DCM. The results are lower conduction losses in the MOSFET, and secondary rectifying diode, and a smaller input EMI filter if the designer needs to meet the requirements C.I.S.P.R. conducted emission levels. On the down side to CCM operation, the flyback transformer will be larger because of the required higher primary inductance.

The advantages to operating in DCM include lower switching losses because the current falls to zero prior to the next switching cycle, and smaller transformer size.

It will ultimately be up to the designer to perform a trade−off study to determine which topology, Boost versus Flyback, Continuous versus Discontinuous Mode of operation will meet all the system performance requirements. But the recent introduction of the NCP1651 allows the system designer one additional option.

For an average current mode flyback topology based PFC converter, determining the transformer parameters (primary inductance and turns ratio) involves several trade−offs. These include peak−to−average current ratio (higher inductance or turns ratio result in lower peak current), switching losses (higher turns ratio leads to higher peak voltage and higher switching losses), CCM vs. DCM operation (lower values of turns ratio or higher values of inductance extend the CCM range) and range of duty cycles over the operational line and load range. ON Semiconductor has designed an Excel−based spreadsheet to help design with the NCP1651 and balance these trade−offs. The design aid is downloadable free−of−charge from our website (www.onsemi.com).

The ideal solution depends on the specific application requirements and the relative priority between factors such as THD performance, cost, size and efficiency. The design aid allows the designer to consider different scenarios and settle on the best solution foe a given application. Following guidelines will help in settling towards the most feasible solution.

1. Turns Ratio Limitations: While higher turns ratio can limit the reflected primary voltage and current, it is constrained by the inherent limitations of the flyback topology. A turns ratio of higher than 20:1 will result in very high leakage inductance and lead to high leakage spikes on the primary switch. Thus, practical application of this approach is restricted to output voltages 12 V and above.
2. CCM Operation: The NCP1651 is designed to operate in both CCM and DCM modes. However, the CCM operation results in much better THD than the DCM operation. Thus, it is recommended that the circuit be designed to operate in CCM at the specified test condition for harmonics compliance (typically at 230 V, full load). Please keep in mind that at or near zero crossing (<10 deg angle), it is neither necessary nor feasible to maintain CCM operation.
3. Following key governing equations have been incorporated in the design aid:

PFC Operation

The basic PWM function of the NCP1651 is controlled by a small block of circuitry, which comprises the DC regulation loop and the PFC circuit. These components are shown in Figure 30.

There are three inputs to this loop. They are the fullwave rectified sinewave, the instantaneous input current and the error signal at the FB/SD pin.

The input current is forced to maintain a near unity power factor due to the control of the AC error amplifier. This amplifier uses information from the AC input voltage and the AC input current to control the power switch in a manner that gives good DC regulation as well as excellent power factor.

The reference multiplier sets a reference level for the input fullwave rectified sinewave. One of its inputs is connected to a scaled down fullwave rectified sinewave, and the other receives the error signal which has been converted to a current. The error signal adjusts the level of the fullwave rectified sinewave on the multiplier's output without distorting it. To accomplish this, it is necessary for the bandwidth of the DC error amp to be less than twice the lowest line frequency. Typically it is set at a factor of ten less than the rectified frequency (e.g. for a 60 Hz input, the bandwidth would be 12 Hz).

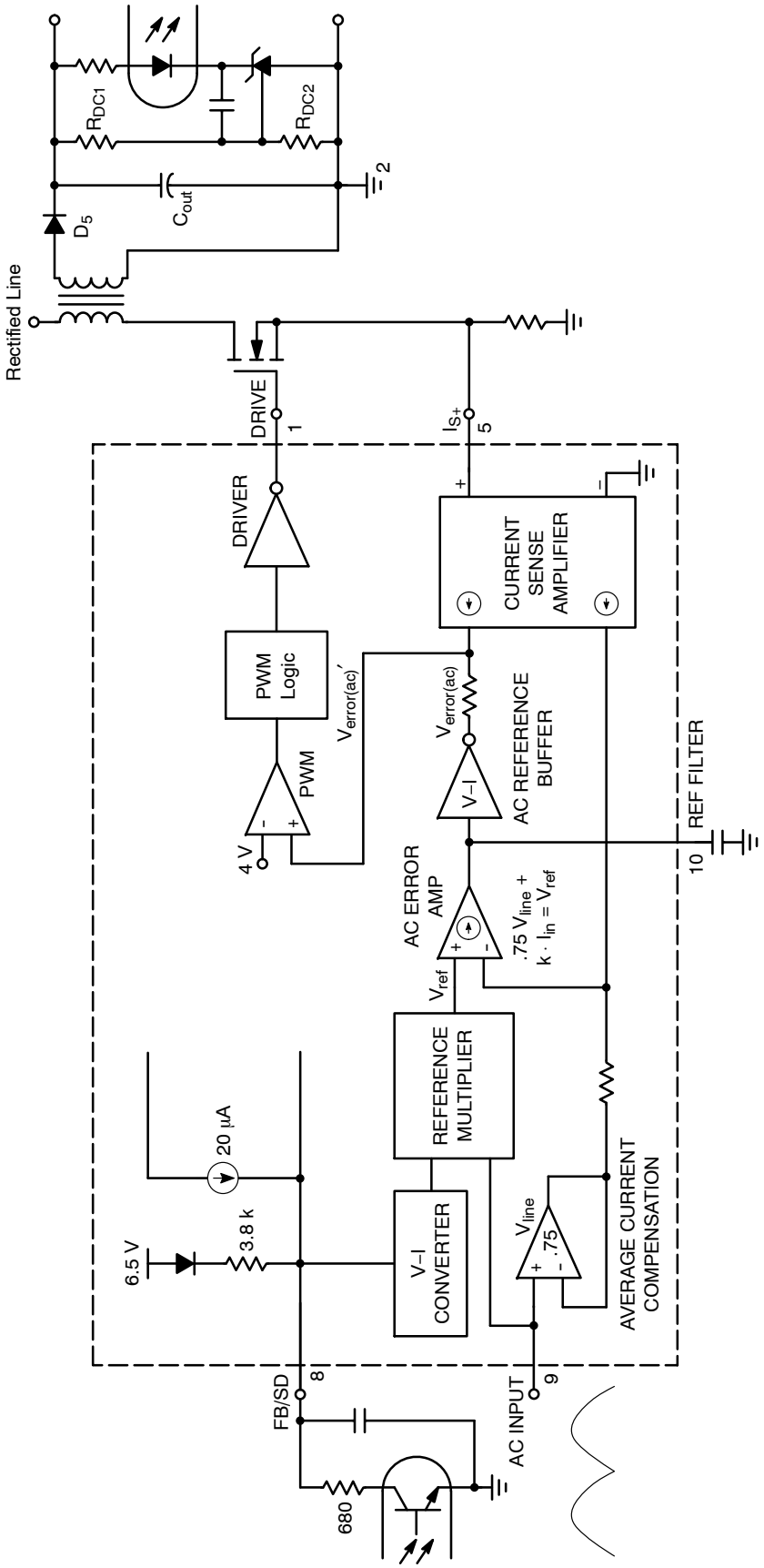


Figure 30. Simplified Block Diagram of Basic PFC Control Circuit

The key to understanding how the input current is shaped into a high quality sine wave is the operation of the AC error amplifier. The inputs of an operational amplifier operating in its linear range, must be equal. There are several secondary effects, that create small differences between the inverting and non−inverting inputs, but for the purpose of this analysis they can be considered to be equal.

The fullwave rectified sinewave output of the reference multiplier is fed into the non−inverting input of the AC error amplifier. The inverting input to the AC error amplifier receives a signal that is comprised of the input fullwave rectified sinewave (which is not modified by the reference multiplier), and summed with the filtered input current. Since the two inputs to this amplifier will be at the same potential, the complex signal at the non−inverting input will have the same waveshape as the AC reference signal. The AC reference signal (V_{ref}) is a fullwave rectified sinewave, and the AC input signal (V_{line}) is also a fullwave rectified sinewave, therefore, the AC current signal (I_{in}), must also be a fullwave rectified sinewave. This relationship gives the formula:

$$V_{ref} = .75 \cdot V_{ref} + (k \times I_{in})$$

The Iin signal has a wide bandwidth, and its instantaneous value will not follow the low frequency fullwave rectified sinewave exactly, however, the output of the AC error amplifier has a low frequency pole that allows the average value of the .75 V_{line} + (k x I_{in}) to follow V_{ref}. Since the AC error amplifier is a transconductance amplifier, it is followed by an inverting unity gain buffer stage with a low impedance output so that the signal can be summed with the instantaneous input switching current (I_{in}). The output of the buffer is still $V_{error(ac)}$.

The difference between $V_{error(ac)}$ and the 4.0 volt reference, sets the window that the instantaneous current will modulate in, to determine when to turn the power switch off.

Since the input current has a fundamental frequency that is twice that of the line, the output filter must have poles lower than the input current to create a reasonable DC waveform. The DC output voltage is compared to a reference voltage by a secondary side error amplifier, and the error signal out of the secondary side amplifier is fed back into the Feedback input through an optocoupler.

The switch is turned on by the oscillator, which makes this a fixed frequency controller. Under normal operation, the switch will remain on until the instantaneous value of $V_{error(ac)}'$ reaches the 4.0 volt reference level, at which time the switch will turn off.

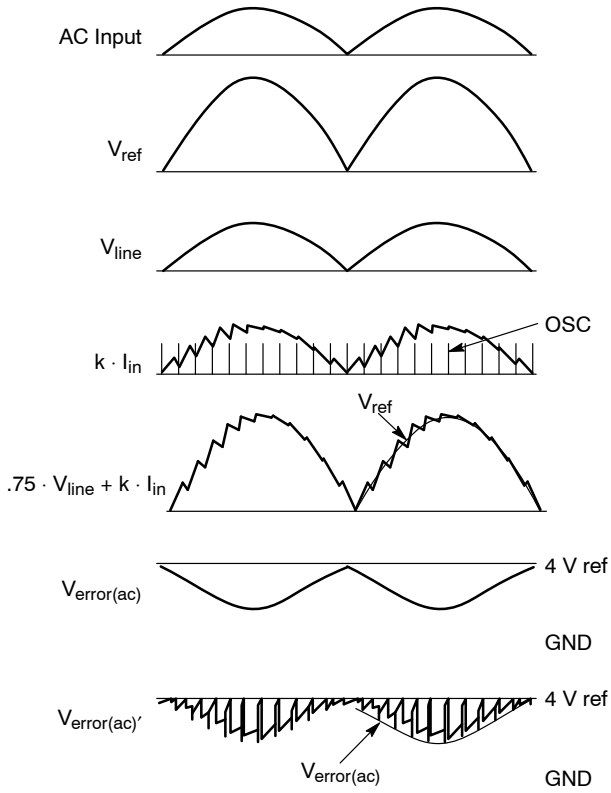


Figure 31. Typical Signals for PFC Circuit

OPERATING DESCRIPTION

DC Reference and Buffer

The internal DC reference is a precision bandgap design with a nominal output voltage of 4.0 volts. It is temperature compensated, and trimmed for a ±1% tolerance of its nominal voltage, with an overall tolerance of ±2%. To assure maximum stability, this is only used as a reference so there is minimal loading on this source.

The DC reference is fed into a buffer with a gain of 1.625 which creates a 6.5 volt supply. This is used as an internal voltage to power many of the blocks inside of the NCP1651 and is also available for external use. The 6.5 volt reference is designed to be terminated with at 0.1 μF capacitor for stability reasons.

There is no buffer between the internal and external 6.5 volt supply, so care should be used when connecting external loads. A short or overload on this voltage output will inhibit the operation of the chip.

Undervoltage Lockout

An Undervoltage Lockout circuit (UVLO) is provided to assure that the unit does not exhibit undesirable behavior at low V_{CC} levels. It also reduces power consumption to a level that allows rapid charging of the V_{CC} cap.

When the V_{CC} cap is initially charging, the UVLO will hold the unit off, and in a low bias current mode until the V_{CC} voltage reaches a nominal 10.8 volt level. At this point the unit will begin operation, and the UVLO will no longer be active. If the V_{CC} voltage falls to a level that is 1.0 volts below the turn−on point, the UVLO circuit will again become active.

When in the active (shutdown) state, the UVLO circuit removes power from all internal circuitry by shutting off the 6.5 volt supply. The 4.0 volt reference remains active, and the UVLO and Shutdown comparators are also active.

Multiplier

The NCP1651 uses a new proprietary concept for its Reference multiplier. This innovative design allows greatly improved accuracy compared to a conventional linear analog multiplier. The multiplier uses a PWM switching circuit to create a scalable output signal, with a very well defined gain.

One input (A) to the multiplier is a voltage−to−current (V−I) converter. By converting the input voltage into a current, an overall multiplier gain can be accomplished. In addition, there will be no error in the output signal due to the series rectifier.

The other signal (Input P) is input into the PWM comparator. This selects a pulse width for the comparator output. The current signal from the V−I converter is factored by the duty cycle of the PWM comparator, and then filtered by the RC network on the output. This network creates a low pass filter, and removes the high frequency content from the original waveform.

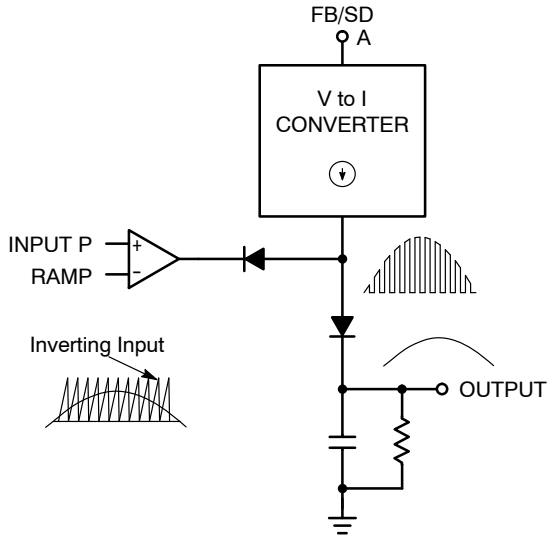


Figure 32. Simplified Multiplier Schematic

The multiplier ramp is generated by the internal oscillator, and is the same signal as is used in the PWM. It will therefore have the same frequency as the power stage.

It is not necessary for Input P (into the PWM comparator) to be a DC signal, low frequency AC signals (relative to the ramp frequency) work well also.

The gain of the multiplier is determined by the current−to−voltage ratio of the V−I converter, the load resistor of the output filter and the peak and valley points of the sawtooth ramp. When the P input signal is at the peak of the ramp waveform, the comparator will allow the A input signal to pass without chopping it at all. This gives an output voltage of the A current multiplied by the output filter resistance. When the P input signal is at the ramp valley voltage, the comparator is held low and no current is passed into the output filter. In between these two extremes, the duty cycle (and therefore, the output signal) is proportional to the level of the P input signal.

The output filter is a parallel RC network. The pole for this network needs to be greater than twice the highest line frequency (120 Hz for a 60 Hz line), and less than the switching frequency. A recommended starting point is a factor of 20 to 50 less than the switching frequency.

The pole is calculated by the formula:

$$f_o = \frac{1}{2 \times \pi \times R \times C}$$

So, for a 60 Hz line, and a 100 kHz switching frequency, a 2.0 kHz pole is a good starting point. This would be a factor of 50 below the switching frequency, and is still far enough above the 120 Hz rectified line frequency that it won't cause undesirable distortion.

The reference multiplier contains an internal loading resistor, with a nominal value of 25 kΩ. This is because the resistor that converts the A input voltage into a current is internal. Making both of these resistors internal, allows for good accuracy and good temperature performance. Only a capacitor needs to added externally to properly compensate this multiplier. It is not recommended that an external parallel resistor be used at the “Ref Gain” pin, due to tolerance variations of the internal resistor.

There is an offset in the compensation (A−input) to the reference multiplier. It is due to the V−I converter that feeds the input.

The FB/SD signal is buffered by a voltage−to−current converter for the appropriate signal into the multiplier. The schematic for that converter follows.

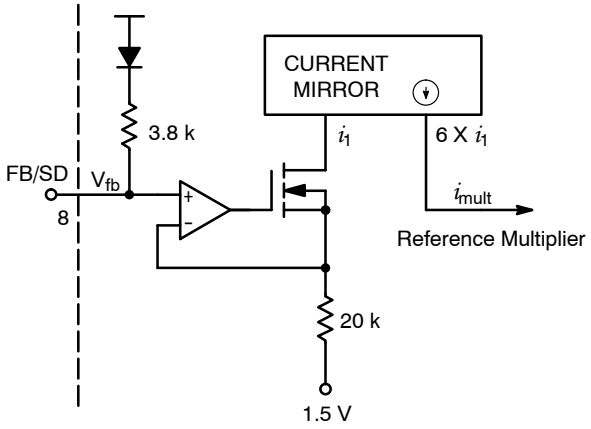


Figure 33. Multiplier V−I Converter

The output current for this stage is:

$$i_{mult} = \frac{6\ (V_{fb} - 1.5\ V)}{20\ k}$$

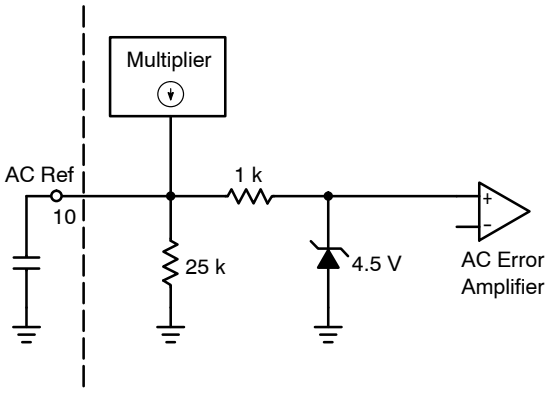


Figure 34. Reference Multiplier Clamp Circuit

There is a 1 k resistor between the AC Ref pin and the AC Error Amplifier for ESD protection. Due to this resistor, the voltage on pin 10 (AC Ref) will exceed 4.5 volts under some conditions, but the maximum voltage at the non−inverting AC Error Amplifier input will be clamped at 4.5 volts.

Feedback/Shutdown

The FB/SD pin is a multiple function pin. Its primary function is to port the error signal to the voltage−to−current converter that feeds the reference multiplier. The operating range for the feedback signal is from 1.0 to 4.0 volts. Below an input level of 1.5 volts, the PWM duty cycle is reduced to zero. At 4.0 volts the PWM is operating at its maximum duty cycle.

The signal at this pin is also sensed by an internal comparator that will shutdown the unit if the voltage falls below 0.60 volts. Under normal operating conditions the signal at this input will be 1.5 volts or greater, and the shutdown circuit will be inactive. This circuit is designed such that a 680 Ohm resistor in series with the optocoupler will assure that the converter will go to zero duty cycle when the opto is on full, but will not go low enough to put the unit into its shutdown mode.

The shutdown function can be used for multiple purposes including overvoltage, undervoltage or hot−swap control. An external transistor, open collector or open drain gate, connected to this pin can be used to pull it low, which will inhibit the operation of the chip, and change the operating state to a low power standby mode. An example of a shutdown circuit is shown in Figure 23.

Ramp Compensation

The Ramp Compensation pin allows the amount of ramp compensation to be adjusted for optimum performance. Ramp compensation is necessary in a current mode converter to stabilize the units operation when the duty cycle is greater than 50%.

The amount of compensation required is dependant on several variables, including the boost inductor value, and the desires of the designer. The value should be based on the falling di/dt of the inductor current. For a boost inductor with a variable input voltage, this will vary over the AC input cycle, and with changes in the input line. A di/dt chart is included in the design spreadsheet that is available for the NCP1651.

For optimum load transient performance, the ramp compensation should equal the falling di/dt at 100% duty cycle. For optimum line transient response, it should equal one half of the falling di/dt at 100% duty cycle.

This pin is a buffered output of the oscillator, which provides a voltage equal to the ramp on the oscillator C_T pin. A resistor from this pin to ground, programs a current that is transformed via a current mirror to the non−inverting input of the PWM comparator.

The ramp voltage due to the inductor di/dt at the input to the PWM comparator is the current shunt voltage at pin 5 multiplied by 10, which is the gain of the current amplifier output that feeds the PWM.

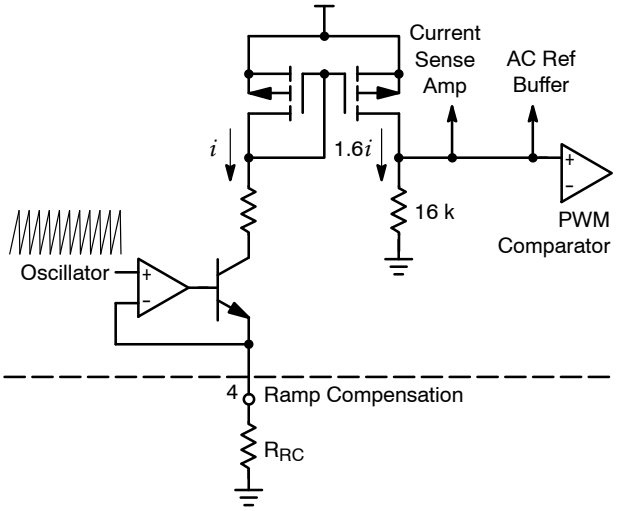


Figure 35. Ramp Compensation Circuit

The current mirror is designed with a 1:1.6 current ratio. The ramp signal injected can be calculated by the following formula:

$$V_{ramp} = \frac{1.6\ Vosc_{pk}\ 16\ k}{R_{RC}} = \frac{102,400}{R_{RC}} \quad \text{(eq. 1)}$$

Where:

V_{ramp} = Peak injected current signal (4 V)

R_{RC} = Ramp compensation resistor (kΩ)

Oscillator

The oscillator generates the sawtooth ramp signal that sets the switching frequency, as well as sets the gain for the multipliers. Both the frequency and the peak−to−peak amplitude are important parameters.

The oscillator uses a current source for charging the capacitor on the C_T pin. The charge rate is approximately 200 μA and is trimmed to maintain an accurate, repeatable frequency. Discharge is accomplished by grounding the C_T pin with a saturated transistor. A hysteretic comparator monitors that ramp signal and is used to switch between the current source and discharge transistor. While the cap is charging, the comparator has a reference voltage of 4.0 volts. When the ramp reaches that voltage, the comparator switches from the charging circuit to the discharge circuit, and its reference changes from 4.0 to ~0.5 volts (overshoot and delays will allow the valley voltage to reach 0 volts).

The relationship between the frequency and timing capacitor is:

$$C_T = 47,000/f$$

Where C_T is in pF and f is in kHz.

It is important not to load the capacitor on this pin, since this could affect the accuracy of the frequency as well as that of the multipliers which use the ramp signal. Any use of this signal should incorporate a high impedance buffer.

Due to the required accuracy of the peak and valley ramp voltages, the NCP1651 is not designed to be synchronized to the frequency of another oscillator.

Average Current Compensation

The input signal to this amplifier is the input fullwave rectified sinewave. The amplifier is a unity gain amplifier, with a voltage divider on the output that attenuates the signal by a factor of 0.75. This scaled down fullwave rectified sinewave is summed with the low frequency current signal out of the current sense amplifier.

The sum of these signals must equal the signal at the non−inverting input to the AC error amplifier, which is the output of the reference multiplier. Since there is a hard limit of 4.5 volts at the non−inverting input, the sum of the line voltage plus the current cannot exceed this level.

A typical universal input design operates from 85 to 265 vac, which is a range of 3.1:1. The output of the Current Compensation amplifier will change by this amount to allow the maximum current to vary inversely to the line voltage.

AC Error Amplifier

The AC error amplifier is a transconductance amplifier. This amplifier forces a signal which is the sum of the current and input voltage to equal the AC reference signal from the reference multiplier.

Transconductance amplifiers differ from voltage amplifiers in that the output is a high impedance with a controlled voltage−to−current gain. This amplifier has a nominal gain of 100 umhos (or 0.0001 amps/volt). This means that an input voltage differential of 10 mv would cause the output current to change by 1.0 μA. Its maximum output current is 30 μA.

Current Sense Amplifier

The current sense amplifier is a wide bandwidth amplifier with a differential input. It consists of a differential input stage, a high frequency current mirror (PWM output) and a low frequency current mirror (AC error amp output).

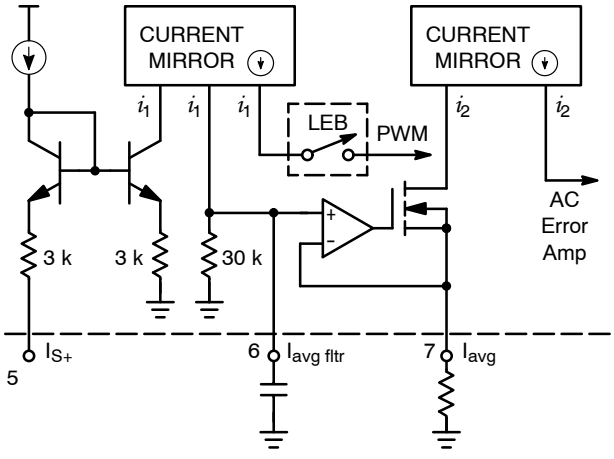


Figure 36. Current Sense Amplifier

The input to the current sense amplifier is a common base configuration. The voltage developed across the current shunt is sensed at the Is+ input. The amplifier input is designed for positive going voltages only; the power stage should resemble the configuration of the application circuit in Figure 38.

Caution should be exercised when designing a filter between the shunt resistor and this input, due to the low impedance of this amplifier. Any series resistance due to a filter, will create an offset of:

$$V_{OS} = 50\ \mu A \times R_{external}$$

which will add a positive offset to the current signal. The effect of this is that the AC error amplifier will try to compensate for the average output current which appears never to go to zero, and cause additional zero crossing distortion.

The voltage across the current shunt resistor is converted into a current (i_1), which drives a current mirror. The output of the i_1 current mirror is a high frequency signal that is a replica of the instantaneous current in the switch. The conversion of the current sense signal to current i_1 is:

$$i_1 = V_{is+}/3\ k$$

The PWM output sends that information directly to the PWM input where it is added to the AC error amp signal and the ramp compensation signal.

The Leading Edge Blanking circuit (LEB) interrupts the current signal to the PWM comparator for the first 200 ns of the switching pulse. This blanks out any spike that might occur at turn on, which could cause false triggering of the PWM comparator.

The other output of the i_1 mirror provides a voltage signal to a buffer amplifier. This signal is the result of i_1 dropped across an internal 30 kΩ resistor, and filtered by a capacitor at pin 6. This signal, when properly filtered, will be the 2x line frequency fullwave rectified sinewave. The filter pole on pin 6 should be far enough below the switching frequency to remove most of the high frequency component, but high enough above the line frequency so as not to cause significant distortion to the input fullwave rectified sinewave waveform.

For a 100 kHz switching frequency and a 60 Hz line frequency, a 10 kHz pole will normally work well. The capacitor at pin 6 can be calculated knowing the desired pole frequency by the equation:

$$C_6 = \frac{1}{2\ \pi\ f30k}$$

Where:

C_6 = Pin 6 capacitance (nF)

f = pole frequency (kHz)

or, for a 10 kHz pole, C_6 would be 0.5 nF.

The gain of the low frequency current buffer is set by the value of the resistor at pin 7. The value of R7 determines the scale factor between the peak current and the average current. The average current will be that of the primary waveform only, since the secondary current will not conduct across the shunt resistor.

PWM Logic

The PWM and logic circuits are comprised of a PWM comparator, an RS flip−flop (latch) and an OR gate. The latch is Set dominant which means that if both R and S are high the S signal will dominate and Q will be high, which will hold the power switch off.

The NCP1651 uses a voltage mode Pulse Width Modulation scheme based on a fixed frequency oscillator. The oscillator outputs a ramp waveform as well as a pulse which is coincident with the falling edge of the ramp. The pulse is fed into the PWM latch and OR gate that follows. During the pulse, the latch is reset, and the output drive is in its low state.

On the falling edge of the pulse, the output drive goes high and the power switch begins conduction. The instantaneous inductor current is summed with the AC error amplifier voltage and the ramp compensation signal to create a complex waveform that is compared to the 4.0 volt reference signal on the inverting input to the PWM comparator. When the signal at the non−inverting input to the PWM comparator exceeds 4.0 volts, the output of the PWM comparator changes to a high state which drives one of the Set inputs to the latch and turns the power switch off until the next oscillator cycle.

The OR gate that follows the PWM is used to inhibit the drive signal to the power switch. In addition to the oscillator pulse, this gate receives a signal from the shutdown OR gate, which can inhibit operation due to an overtemperature condition, shutdown signal, or insufficient V_{CC}.

Driver

The output driver can be used to directly drive a FET, for low and medium power applications, or a larger driver for high power applications.

It is a complementary MOS, totem pole design, and is capable of sourcing and sinking over 1.5 amps, with typical rise and fall times of 50 ns with a 1.0 nF load. The totem pole output has been optimized to minimize cross conduction current during high speed operation.

Additional internal circuitry has been added to keep the Driver in its low state whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pulldown resistor.

Shutdown Modes and Logic

Overtemperature A temperature sensor and reference is provided to monitor the junction temperature of the chip. The chip will operate to a nominal temperature of 160°C at which time the output of the temperature sensor will change to a low state. This will set the output of the shutdown NAND gate high, which in turn will set the output of the PWM OR gate high, and force the driver into a low state.

There is a hysteresis of 30°C on this circuit, which will allow the chip to cool down to 130°C before resuming operation.

While in the overtemperature shutdown mode, the startup circuit will be operational and the V_{CC} will cycle between 10.8 and 9.8 volts.

Insufficient V_{CC} If the level of the V_{CC} voltage is not sufficient to maintain operation, the drive of the chip will be inhibited and the divide−by−eight timer will be invoked. This will normally occur when the output is overloaded. Under this condition, the divide−by−eight counter will count for 8 V_{CC} cycles. At the end of the eighth cycle the driver will be enabled and the circuit will attempt to start. If the failure has been corrected, the output will come up and the circuit will resume normal operation. If not, another cycle will begin. The waveforms for overload timeout are shown in Figure 3.

Shutdown The NCP1651 has a shutdown circuit that can be used to inhibit the operation of the chip by reducing the FB/SD pin voltage to less than 0.6 volts. When a shutdown signal is issued, the output of the shutdown comparator goes low. This immediately ceases the operation of the unit by OR'ing that signal to the output of the PWM logic, and holding the driver in its low state.

The inverted output of the shutdown comparator is fed in to the reset pin of the divide−by−eight counter. The counter reset pin sets its count to seven. As long as the reset pin is low, the counter will remain at seven. When the shutdown signal is removed, the reset pin will go high, and the counter will continue to count to eight. The counter is triggered on the negative edge of the startup enable signal. This means that a shutdown signal that is removed on the upward V_{CC} slope will be in the 7 count for the remaining rise and fall of that V_{CC} cycle and will change to 8 on the next cycle.

This system assures that the unit will not be enabled until the V_{CC} voltage has a full discharge cycle available, and it also insures that the unit will commence operation in less than two V_{CC} cycles. A timing diagram of this mode of operation is shown in Figure 3. The count for the divide−by−eight counter is shown as 7, 7, 7, 8 which illustrates the operation of the reset function.

If the shutdown signal is terminated before the V_{CC} voltage reaches the lower UVLO limit (i.e. 9.8 volts), the unit will resume operation on the following V_{CC} down slope, and if the shutdown signal is terminated on the V_{CC} upward slope, the unit will resume operation on the second V_{CC} down slope.

AC Reference Buffer

The AC reference buffer converts the voltage generated by the AC error amplifier to be converted into a current to be summed with the ramp compensation signal and the instantaneous current signal.

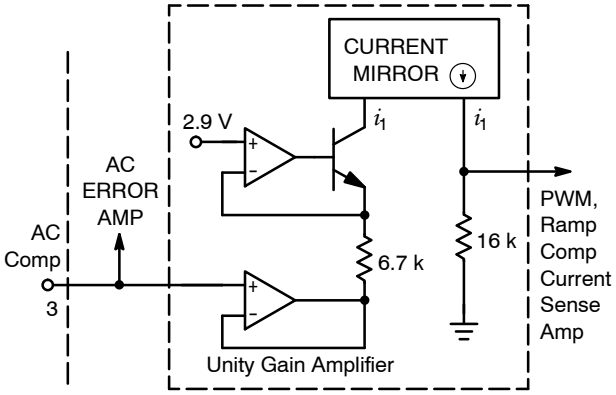


Figure 37. AC Reference Buffer Schematic

The buffer's transfer function is:

$$i_{out} = (2.9\ V - V_{ac(ea)})/6.7\ k$$

The buffer amplifier, converts the input voltage to a current by creating a current equal to the voltage difference between the AC error amplifier output and the 2.9 volt reference dropped across the 6.7 kΩ resistor. The bipolar transistor level shifts the voltage and maintains the proper current into the current mirror. The current mirror has a 1:1 ratio and delivers its output current to the PWM input. This current is summed with the currents of the ramp compensation signal and the instantaneous current signal to determine the turn−off point in the switching cycle.

Startup Circuit

The startup circuit serves several functions. In addition to providing the initial charge on the V_{CC} capacitor, it serves as a timer for the startup, overcurrent, and shutdown modes of operation. Due to the nature of this circuit, this chip must be biased using the startup circuit and an auxiliary winding on the power transformer. ***Attempting to operate this chip off of a fixed voltage supply will cause the chip to latch up in some modes of operation.***

A high voltage FET is biased as a current source to provide current for startup power. On the application of input voltage, the high voltage startup circuit is enabled and current is drawn from the rectified AC line to charge the V_{CC} cap.

When the voltage on the V_{CC} cap reaches the turn on point for the UVLO circuit (10.8 volts typical), the startup circuit is disabled, and the PWM circuit is enabled. With the NCP1651 enabled, the bias current increases from its standby level to the operational level. The divide−by−eight counter is preset to the count of 7, so that on startup the chip will not be operational on the first cycle. The second V_{CC} cycle will be number 8, and the chip will be allowed to start at this time. In the shutdown mode, the V_{CC} cycle is held in the 7 count state until the shutdown signal is removed. This

allows for a repeatable, fast restart. See Figure 3 for timing diagram.

The unit will remain operational as long as the V_{CC} voltage remains above the UVLO undervoltage trip point. If the V_{CC} voltage is reduced to the undervoltage trip point, operation of the unit will be disabled, the startup circuit will again be enabled, and will charge the V_{CC} cap up to the turn on voltage level. At this point the startup circuit will turn off and the unit will remain in the shutdown mode. This will continue for the next seven cycles. On the eighth cycle, the NPC1651 will again become operational. If the V_{CC} voltage remains above the undervoltage trip point the unit will continue to operate, if not the unit will begin another divide−by−eight cycle.

The purpose of the divide−by−eight counter is to reduce the power dissipation of the chip under overload conditions and allow it to recycle indefinitely without overheating the chip.

It is critical that the output voltage reaches a level that allows the auxiliary voltage to remain above the UVLO turn−off level before the V_{CC} cap has discharged to that level. If the bias voltage generated by the inductor winding fails to exceed the shutdown voltage before the capacitor reduces to the UVLO undervoltage turn−off level, the unit will shut down and go into a divide−by−eight cycle, and will never start. If this occurs, the V_{CC} capacitor value should be increased.

Soft−Start Circuit

The AC error amplifier has been configured such that a low output level will cause the output duty cycle to go to zero. This will have the effect of soft−starting the unit at turn−on, since the output is coupled to ground through a capacitor.

There will be an initial offset of the output voltage due to the output current and the resistor at pin 11. For example, if the output is saturated in the high state at turn on, it will source 50 μA. If pin 11 is terminated with a 2.2 kΩ resistor and a 0.01 F capacitor, the initial step will be:

$$50\ \mu A \times 2.2\ k = 0.11\ volts$$

and the rate of rise will be:

$$50\ \mu A/0.01\ \mu F = 5\ mV/\mu s$$

or, 560 μs until the output is at 2.8 volts, which corresponds to full duty cycle.

There is also a clamp on pin 8 that will keep the capacitance on that pin discharged to 1.5 volts so that the FB/SD signal will also slew up from a low power level to a high power level. When the unit is in standby mode, the clamp will be enabled. At the same time as the unit is enabled, the clamp will be disabled to allow the feedback signal to control the loop.

An external soft−start circuit can be added, as shown in Figure 24, if additional time is desired.

DESIGN GUIDELINES

NOTE: This is a theoretical design, and it is not implied that a circuit designed by this procedure will operate properly without normal troubleshooting and adjustments as are common with any power conversion circuit. ON Semiconductor provides a spread sheet that incorporates the relevant equations, and will calculate the bias components for a circuit using the schematic shown.

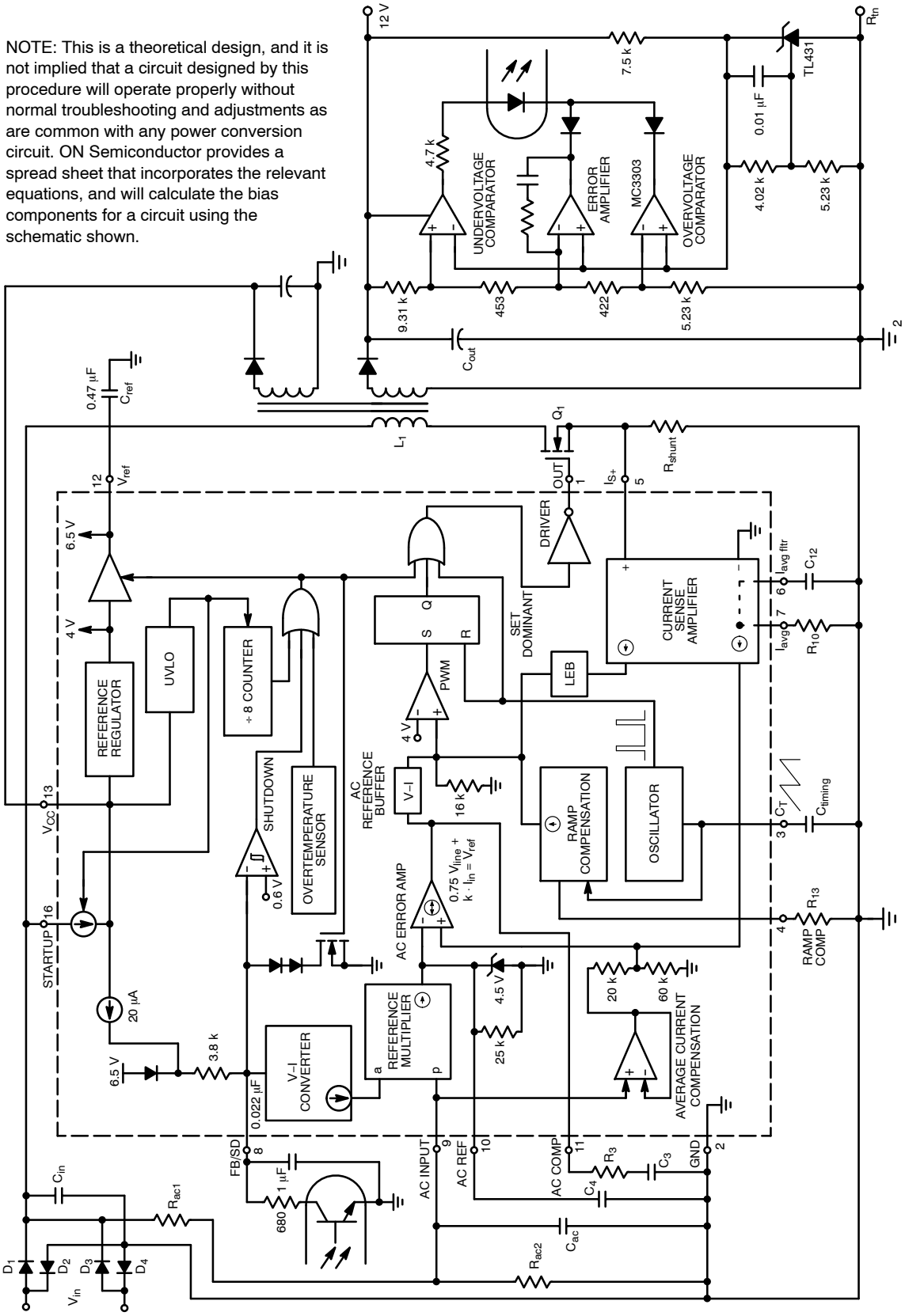


Figure 38. Typical Application Schematic

Basic Specifications

The design of any power converter begins with a basic set of specifications. The following parameters should be known before you begin:

Po_{max} (Maximum rated output power)

$Vrms_{min}$ (Minimum operational line voltage)

$Vrms_{max}$ (Maximum operational line voltage)

f_{switch} (Nominal switching frequency)

V_{out} (Nominal regulated output voltage)

Most of these parameters will be dictated by system requirements.

Transformer

For an average current mode, fixed frequency PFC converter, there is no magic formula to determine the optimum value of the transformer's primary inductance. There are several trade−offs that should be considered. These include peak current vs. average current, switching losses vs. core losses and range of duty cycles over the operational line and load range. All of these are a function of inductance, line and load. These parameters determine when the converter is operating in the continuous conduction mode and when it is operating in the discontinuous conduction mode.

If you are designing your own transformer, the ON Semiconductor spreadsheet (**NCP1651_Design.xls**) that is available as a design aid for this part can be of help. Enter various values of inductance as well as the turns ratio and observe the variation in duty cycle and peak current vs. average current.

The transformer's duty cycle is an important parameter. There are two main limitations for the duty cycle. The first is the output voltage reflected back to the primary, which is scaled by the turns ratio. This means that with a 10:1 (pri:sec) turns ratio, and a 12 volt output, the power switch will see the input voltage plus 120 volts (10 x 12 volts) plus leakage inductance spike. This reflected voltage determines the maximum voltage rating of the power switch.

The second, there are practical limits to the turns ratio. Given the flyback converter transfer function, continuous conduction mode,

$$V_O = V_{in}\, n\, (D/1 - D)$$

It is evident that there is a direct relationship between duty cycle and the turns ratio. In general, 10:1 is about the maximum, although some transformer manufacturers go as high as 12:1 or even 15:1. Turns ratios of 20:1 and above are not normally practical as they result in very high values of leakage inductance, which creates large spikes on the power switch. They also have a very large reflectovoltage associated with them.

The other option is to contact a transformer manufacturer such as Coiltronics (www.cooperet.com/) or Coilcraft (www.coilcraft.com/). These companies will design and manufacture transformers to your requirements.

Using the available spreadsheet, with the following parameters, a primary inductance of 330 μH and a turns ratio of 10:1 would be a good choice.

Limits

Po_{max} = 100 W

Vin_{max} = 265 V_{rms}

Vin_{min} = 85 V_{rms}

V_O = 12 V

L_P = 330 μH

f_{switch} = 100 kHz

N_p/N_s = 10

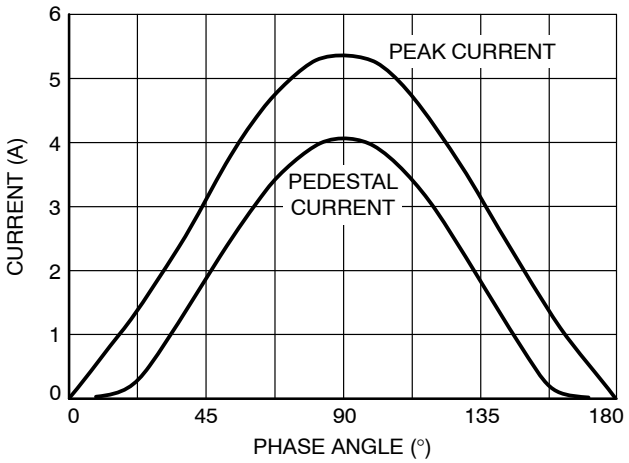


Figure 39. Switching Current versus Phase Angle

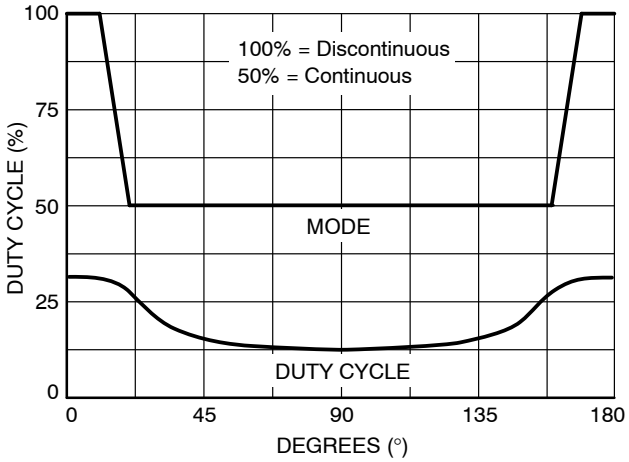


Figure 40. Continuous/Discontinuous and Duty Cycle

If an auxiliary winding is desired to provide a bias supply, it should provide a minimum of 12.1 volts (to exceed the UVLO spec) and a maximum of 18 volts. The auxiliary winding should be connected such that it conducts when the power switch is off. Near the zero crossings of the line frequency, the voltage will have a peak voltage equal to the regulated output voltage divided by the turns ratio. The filter cap on the V_{CC} pin needs to be of sufficient size to hold the voltage up over between the zero crossings.

Error Amplifier

The error amplifier resides on the secondary side of the circuit, and therefore is not part of the chip. A minimal solution would include either a discrete amplifier and reference, or an integrated circuit that combines both, such as the TL431 series of regulators.

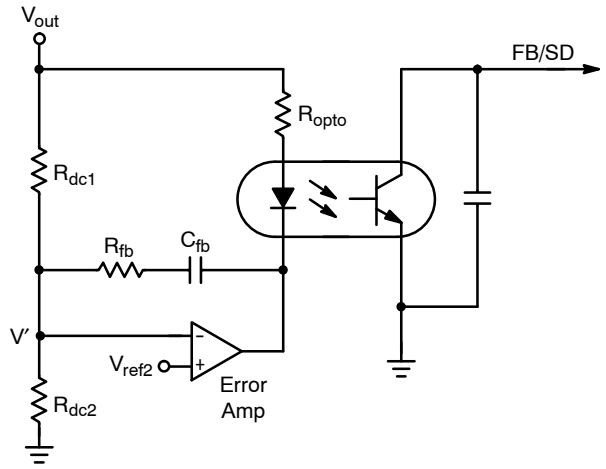


Figure 41. Error Amplifier Circuit

This configuration for the error amplifier will result in a low cost regulator, however, due to the slow loop response of a PFC regulator it will not protect against overvoltage conditions (e.g. load removal) or droop when a transient load is added.

The primary side circuit has been designed such that the PFC controller will operate at maximum duty cycle with the optocouple in a non−conducting state. This is necessary to allow the unit to bring up the output when the system is initially energized. At this time there is not output voltage available to drive the LED in the optocoupler.

In the circuit of Figure 41, the amplifier and reference need to be rated at the maximum voltage that the output will experience, including transient conditions. Resistors R_{dc1} and R_{dc2} need to be chosen such that the voltage at V′ is equal to V_{ref2} when V_{out} is at its regulated voltage. R_{opto} is a current limiting resistor that protects the optocoupler from current transients due to output surges.

This design also includes inherent compensation from transients. Since the bandwidth of the error amplifier is very low, its output can not respond rapidly to changes in the output voltage. A transient change in the output voltage will change the current through R_{opto}. Since the output of the error amplifier does not change immediately, if the output voltage increases, the voltage across R_{opto} will increase. This drives more current through the optocoupler, which in turn reduces the output of the converter.

An alternate regulator is recommended, which is only slightly more expensive, and offers excellent protection from positive transients, and quick recovery from negative transients.

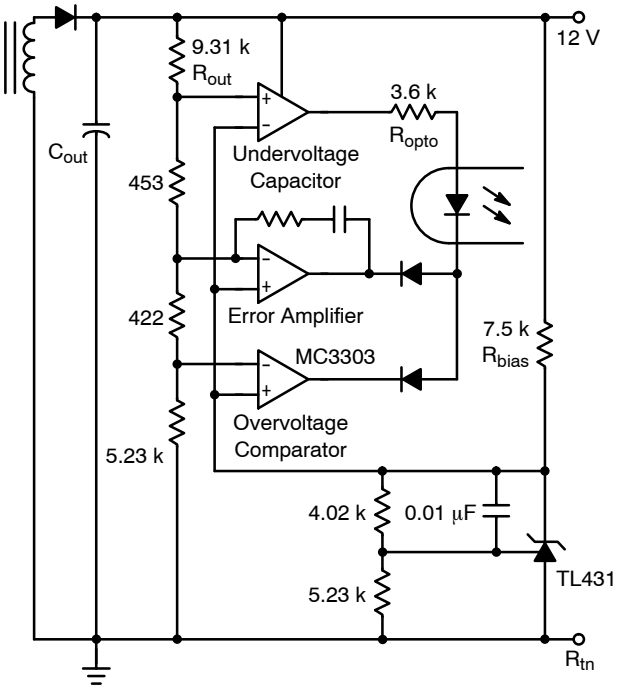


Figure 42. Error Amp with Over/Undershoot Protection

The configuration shown in Figure 42, incorporates an error amplifier with slow loop response, plus overvoltage and undervoltage comparators. Under normal operation the outputs of the Undervoltage and Overvoltage Comparators are high. The Undervoltage Comparator provides drive for the optocoupler, while the Overvoltage Comparator reverse biases the diode on its output and is out of the loop.

This circuit is designed with 8% trip points both above and below the regulation limit. If an overvoltage condition exists, the Overvoltage comparator will respond very quickly. When its output goes low, it will provide maximum drive to the optocoupler, which will shut off the output of the converter.

If the output voltage drops 8% or more below its regulated level, the Undervoltage Comparator will go low. This will remove the drive from the optocoupler, which will allow the regulator to increase the duty cycle and return the output to its regulation range much faster than the error amplifier could.

This configuration will work over a range of 5 to 30 volts, with the appropriate changes in R_{out}, R_{bias} and R_{opto}.

$$R_{out}\ (k\Omega) = (V_{out} - 4.753) / 0.7785$$

$$R_{bias}\ (k\Omega) = (V_{out} - 4.4)$$

$$R_{opto}\ (k\Omega) = (V_{out} - 3) / 2$$

The value for R_{opto} will allow a maximum of 2 mA to drive the optocoupler. If additional current is needed, change the 2 in the denominator of that equation to the current (in mA) that is desired.

AC Voltage Divider

The voltage divider from the input rectifiers to ground is a simple but important calculation. For this calculation it is necessary to know the maximum line that the unit can operate at. The peak input voltage will be:

Vin_{peak} = 1.414 x $Vrms_{max}$

The maximum voltage at the AC input (pin 5) is 3.75 volts (this is true for both multipliers).

If the maximum line voltage is 265 Vac, the peak input voltage is:

Vin_{peak} = 1.414 x 265 V_{rms} = 375 V_{pk}

To keep the power dissipation reasonable for a 1/2 watt resistor (R_{ac1}), it should dissipate no more than 1/4 watt. The power in this resistor is:

$PR_{ac1} = (375\ V - 3.75\ V)^2 / R_{ac1} = 0.25$ watts

so: R_{ac1} = 551 kΩ

To minimize dissipation, use the next largest standard value, or 560 kΩ.

Typically, two 1/4 resistors are used in series to handle the power.

Then, $R_{ac2} = 3.75\ V / ((375\ V - 3.75\ V) / 560\ k) = 5.6$ kΩ

Current Sense Resistor/Ramp Compensation

The combination of the voltage developed across the current sense resistor and ramp compensation signal, will determine the peak instantaneous current that the power switch will be allowed to conduct before it is turned off.

The vector sum of the three signals that combine to create the signal at the non−inverting input to the PWM comparator must add up to 4.0 volts in order to terminate the switch cycle. These signals are the error signal from the AC error amp, the ramp compensation signal, and the instantaneous current. For a worst case condition, the output of the AC error amp could be zero (current), which would require that the sum of the ramp compensation signal and current signal be 4.0 volts. This must be evaluated under full load and low line conditions.

For proper ramp compensation, the ramp signal should match the falling di/dt (which has been converted to a dv/dt) of the inductor at 50% duty cycle. 50% duty cycle will occur when the input voltage is 50% of the output voltage. Both the falling di/dt and output voltage need to be reflected by the transformer turns ratio to the primary side. Thus the following equations for R_S and R_{RC} must be satisfied:

di/dt primary = $V_{in}/L_P \cdot T/2$

di/dt secondary = $V_O/L_S \cdot T/2$

$$L_S = \left(\frac{N_S}{N_P}\right)^2 L_P$$

di/dt reflected to the primary:

$$\left(\frac{V_O}{L_P}\right)\left(\frac{N_P}{N_S}\right)^2 \cdot \frac{T}{2} \cdot \frac{N_S}{N_P}$$

Simplifies to:

$V_O/L_P \cdot N_P/N_S \cdot T/2$

di/dt primary = di/dt secondary

$V_{in}/L_P \cdot T/2 = V_O/L_P \cdot N_P/N_S \cdot T/2$

$V_{in}/L_P = V_O/L_P \cdot N_P/N_S$

Equation 2)

For proper slope compensation, the relationship between R_S and R_{RC} is:

di/dt (primary) · T · R_S · High Frequency Current Gain = V_{Rcomp}

$V_O/L_P \cdot T \cdot N_P/N_S \cdot R_S \cdot 16\ k/3\ k = 102.4\ k/R_{RC}$

$R_S = (19{,}200/R_{RC} \cdot T) \cdot (L_P/V_O) \cdot (N_S/N_P)$

Equation 3)

$t_{on} = T/(N_S/N_P \cdot (\sqrt{2} \cdot V_{LL}/V_O)) + 1$

For maximum output current, when the error amplifier is saturated in a low state, the ramp compensation signal plus the current signal must equal 4.0 volts (3.8 volts is used to avoid over driving the amplifier), which is the reference level for the PWM comparator. So:

Equation 4) $Vref_{PWM} = Vin_{ST} + V_{Rcomp}$

$3.8\ V = I_{PK} \cdot R_S \cdot 16\ k/3\ k + 102.4\ k/R_{RC} \cdot t_{on}/T$

$$R_{RC} = \frac{102.4\ k\ t_{on}}{(3.8 - 5.3\ I_{PK}\ R_S)}$$

Combining equations 2 and 4 gives:

$$R_S = \frac{3.8}{\frac{N_P}{N_S}\frac{t_{on}V_O}{0.1875\ L_P} + 5.33\ I_{pk}}$$

Where:

R_S is the current shunt resistor (Ohms)
R_{RC} is the ramp compensation resistor (Ohms)
t_{on} is the on time for the conditions given (μs)
T is the period for the switching frequency (μs)
L_P is the primary inductance of the transformer (μH)
V_{out} is the output voltage (VDC)
V_{rms} is the rms line voltage at low line (V_{rms})
P_{out} is the output power at full load (watts)
I_{avg} (T) is the average current for one switching cycle (A)
I_{pk} is the instantaneous peak primary side current (A)
$V_{(t)}$ is the peak line voltage (volts)
N_P/N_S is the transformer turns ratio (dimensionless)

Current Scaling Resistor & Filter Capacitor

R_7 sets the gain of the averaged current signal out of the current sense amplifier which is fed into the AC error amplifier. R_7 is used to scale the current to the appropriate level for protection purposes in the AC error amplifier circuit.

R_7 should be calculated to limit the maximum current signal at the input to the AC error amplifier to less than 4.5 volts at low line and full load. 4.5 volts is the clamp voltage at the output of the reference amplifier and limits the maximum averaged current that the unit can process. The equation for R_7 is:

$$R_7 = \frac{212\ k \cdot R_S \cdot P_{in}}{Vin_{LL}\left(4.5 - (0.75 \cdot AC_{ratio} \cdot Vin_{LL} \cdot \sqrt{2})\right)}$$

Where: P_{in} = rated input power (W)
R_S = Shunt resistance (W)
V_{inLL} = min. operating rms input voltage (W)
AC_{ratio} = AC attenuation factor at pin 9

This equation does not allow for tolerances, and it would be advisable to increase the input power to assure operation at maximum power over production tolerance variations.

The current sense filter capacitor should be selected to set its pole about a factor of 10 below the switching frequency.

$$C_6 = \frac{5.3}{f}$$

Where: C_6 = Pin 6 capacitance (nF)
f = pole frequency (kHz)

so, for a 100 kHz switching frequency, a 10 kHz pole is desirable, and C_6 would be 0.5 nF.

Reference Multiplier

The output of the reference multiplier is a pulse width modulated representation of the analog input. The multiplier is internally loaded with a resistor to ground which will set the DC gain. An external capacitor is required to filter the signal back into one that resembles the input fullwave rectified sinewave. The pole for this circuit should be greater than the line frequency and lower than the switching frequency.

1/15th of the switching frequency is a recommended starting value for a 60 Hz line frequency. The filter capacitor for pin 10 can be determined by the following equation:

$$C_{10} = \frac{1}{2\ 3.14\ 25\ k\ f_{pole}} = \frac{6.366E{-}6}{f_{pole}}$$

Where: C_{10} = Pin 10 capacitance (F)
f_{pole} = Ref gain pole freq (Hz)

AC Error Amplifier

The AC error amplifier is a transconductance amplifier that is terminated with a series R_C impedance. This creates a pole−zero pair.

To determine the values of R_3 and C_3, it is necessary to look at the two signals that reach the PWM inputs. The non−inverting input is a slow loop using the averaged current signal. It's gain is:

$$A_{lf} = \frac{30\ k}{3\ k} \cdot \frac{15\ k}{R_7} \cdot (g_m \cdot R_{11}) \cdot 2.3$$

Where the first two terms are the gains in the current sense amplifier averaging circuit. The next term is the gain of the transconductance amplifier and the constant is the gain of the AC Reference Buffer.

The high frequency path is that of the instantaneous current signal to the PWM non−inverting input. This gain is 16 k/3 k = 5.33, since the input signal is converted to a current through a 3 k resistor in the current sense amplifier, and then terminated by the 16 k resistor at the PWM input.

For stability, the gain of the low frequency path must be less than the gain of the high frequency path. This can be written as:

$$\frac{345,000 \cdot g_m \cdot R_{11}}{R_7} < 5.3$$

The suggested resistor and capacitor values are:

$$R_{11} = \frac{R_7}{130,000\ g_m}$$

and for a zero at 1/10th of the switching frequency

$$C_{11} = \frac{1.59}{f_{SW}\ R_{11}}$$

Where: R_7 & R_{11} are in units of Ohms
g_m is in units of mhos
C_{11} is in Farads
f_{sw} is in Hz

Loop Compensation

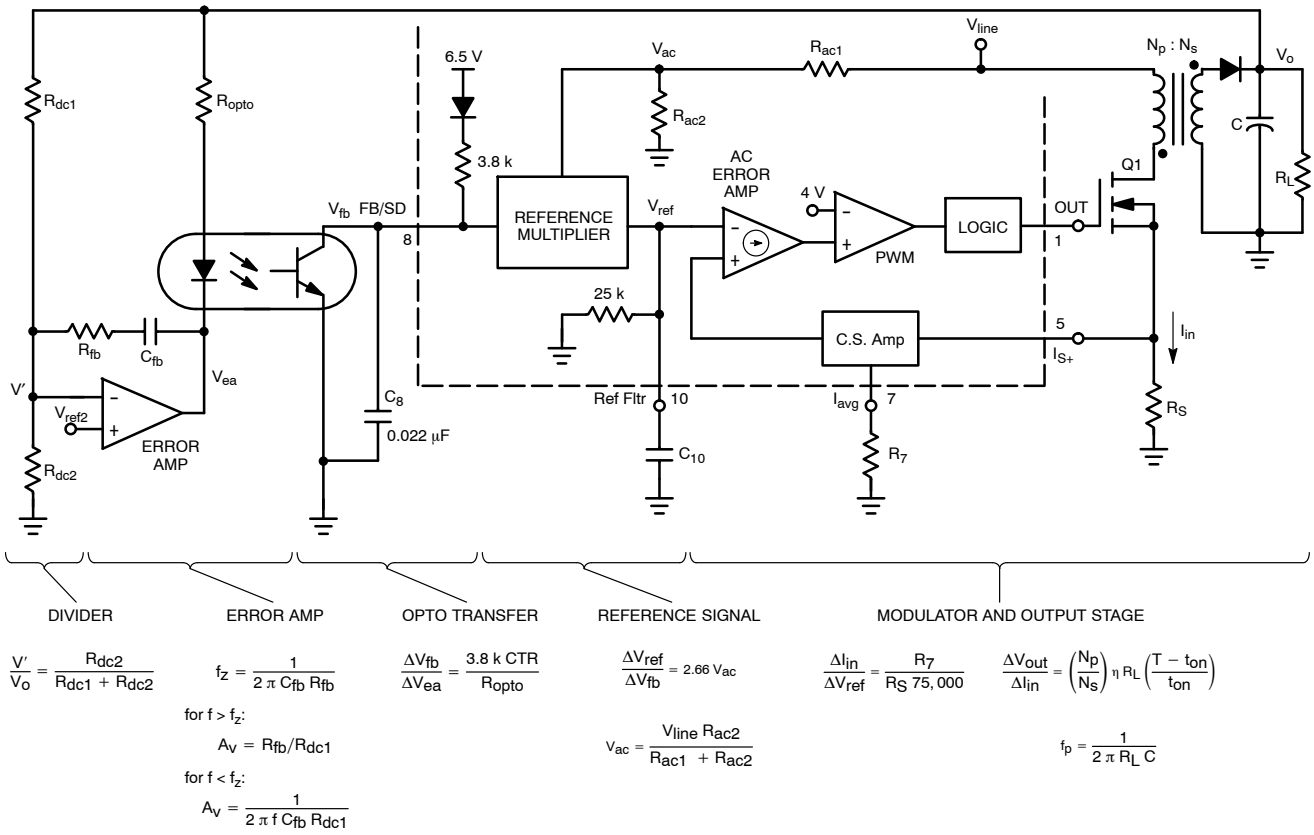


Figure 43. Voltage Regulation Loop

Loop Model

The model for the voltage loop has been broken down into six sections. The voltage divider, error amplifier, and opto Transfer are external to the chip, and the reference signal, modulator and output stage are internal.

The modulator and output stage circuitry is greatly simplified based on the assumption that that poles and zeros in the current feedback loop are considerably greater than the bandwidth of the overall loop. This should be a good assumption, because a bandwidth in the kilohertz is necessary for a good current waveform, and the voltage error amplifier needs to have a bandwidth of less than the lowest line frequency that will be used.

There are two poles in this circuit. The output filter has a pole that varies with the load. The pole on the voltage error amplifier will be determined by this analysis.

Voltage Divider

The voltage divider is located on the secondary side circuitry. It is a simple resistive divider that reduces the output voltage to the level required by the internal reference on the voltage error amplifier. If the amplifier circuit of Figure 42 is used, there are four resistors instead of 2. To determine the gain of this circuit, R_{dc1} is the equivalent of the upper two resistors, 9.31 k and 453 Ohms respectively, and R_{dc2} is the equivalent of the lower two resistors, 422 and 5.23 k respectively.

Voltage Error Amplifier

The voltage error amplifier is constrained by the two equations. When this amplifier is compensated with a pole−zero pair, there will be a unity gain pole which will be cancelled by the zero at frequency f_z. The corresponding bode plot would be:

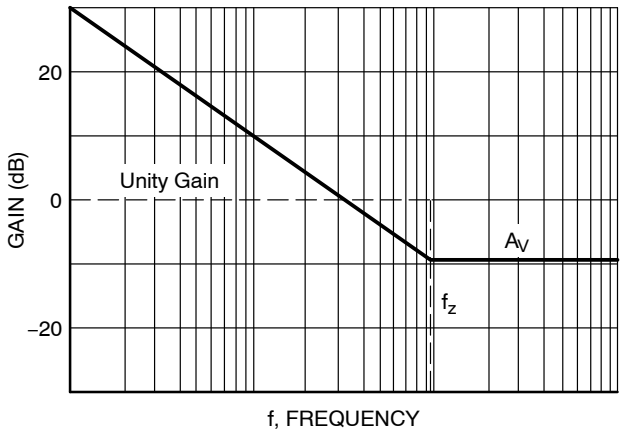


Figure 44. Pole−zero Bode Plot

The gain at frequencies greater than f_z is determined by R_{fb}. Once R_{fb} is determined, the value of C_{fb} can be easily calculated using the formula for f_z.

Optocoupler Transfer

The optocoupler is used to allow for galvanic isolation for the error signal from the secondary to primary side circuits. The gain is based on the Current Transfer Ratio of the device. This can change over temperature and time, but will not result in a large change in dB.

The recommended capacitor at pin 8 is 0.022 μF. If a larger capacitor is used, the pole may become low enough that it will have an effect on the gain phase plots near the unity gain crossover frequency. In this case and additional zero will be required in the error amplifier bias circuitry.

Reference Signal

The error signal is transmitted to the primary side circuit via. the optocoupler, is converted to a current by the V−I converter and is then used as an input to the reference multiplier. The gain of this block is dependent on the AC input voltage, because of the multiplier which requires two inputs for one output.

Modulator and Output Stage

The modulator receives an input from the reference multiplier and forces the current to follow the shape and amplitude. The is an internal loop within this section due to the current sense amplifier. Based on the assumptions listed in the introduction to this analysis, this is not analyzed separately.

The equation for the gain is good for frequencies below the pole. There is a single pole due to the output filter. Since the NCP1651 is a current mode converter, the inductor is not part of the output pole as can be seen in that equation.

The modulator and output stage transfer functions have been split into two sets of equations. The first defines the relationship between the input current and AC reference signal, and the later, define the output stage gain and pole. Due to the nature of a flyback transformer, the gain of the output stage is dependant on the duty cycle (t_{on}/T). For continuous mode operation, the on−time is:

$$t_{on} = \frac{T}{\frac{N_S}{N_P} \cdot \frac{\sqrt{2} \cdot V_{rms}}{V_{out}} + 1}$$

Calculating the Loop Gain

At this point in the design process, all of the parameters involved in this calculation have been determined with the exception of the pole−zero pair on the output of the voltage error amplifier.

All equations give gains in absolute numbers. It is necessary to convert these to the decibel format using the following formula:

$A(dB) = 20\ Log_{10}\ (A)$

For example, the voltage divider would be:

$$A = \frac{5.6\ k}{560\ k + 5.6\ k} = 0.0099$$

$A(dB) = 20\ Log_{10}\ 0.0099 = -40\ dB$

The gain of the loop will vary as the input voltage changes. It is recommended that the compensation for the error amplifier be calculated under high line, full load conditions. This should be the greatest bandwidth that the unit will see.

By necessity, the unity gain (0 dB) loop bandwidth for a PFC unit, must be less than the line frequency. If the bandwidth approaches or exceeds the line frequency, the voltage error amplifier signal will have frequency components in its output that are greater than the line frequency. These components will cause distortion in the output of the reference amplifier, which is used to shape the current waveform. This in turn will cause distortion in the current and reduce the power factor.

Typically the maximum bandwidth for a 60 Hz PFC converter is 10 Hz, and slightly less for a 50 Hz system. This can be adjusted to meet the particular requirements of a system. The unity gain bandwidth is determined by the frequency at which the loop gain passes through the 0 dB level.

For stability purposes, the gain should pass through 0 dB with a slope of −20 dB for approximately on decade on either side of the unity gain frequency. This assures a phase margin of greater than 45°.

The gain can be calculated graphically using the equations of Figure 18 as follows:

Divider: Calculate V'/V_o in dB, this value is constant so it will not change with frequency.

Optocoupler Transfer: Calculate V_{fb}/V_{ea} using the equation provided. Convert this value into dB.

Reference Signal: Calculate V_{ref}/V_{fb} using the peak level of the AC input signal at high line that will be seen on pin 9. Convert this to dB. This is also a constant value.

Modulator and Output Stage: Calculate the gain in dB for DI_o/DV_{ref} for the modulator, and also the gain in dB for the output stage (DV_{out}/DI_{in}). Calculate the pole frequency. The gain will be constant for all frequencies less than f_p. Starting at the pole frequency, this gain will drop off at a rate of 20 dB/decade.

Plot the sum of all of the calculated values. Be sure to include the output pole. It should resemble the plot of Figure 45. This plot shows a gain of 34 dB until the pole of the output filter is reached at 3 Hz. After that, the gain is reduced at a rate of 20 dB/decade.

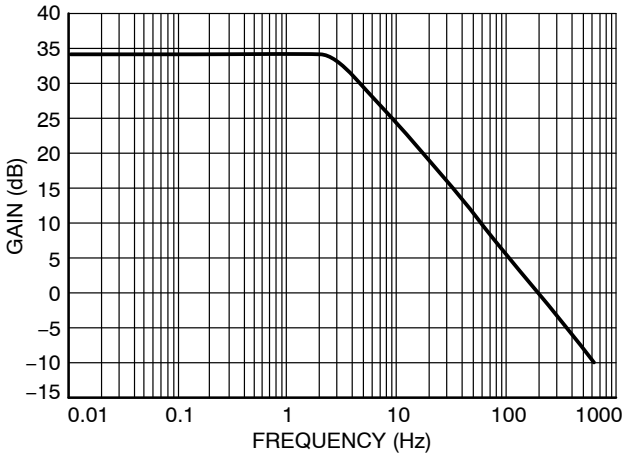


Figure 45. Forward Gain Plot

For a crossover frequency of 10 Hz, the error amplifier needs a gain of −25 dB at 10 Hz, since the forward gain is equal to 25 dB at this frequency. The high frequency gain of the error amplifier is:

$A_{Vhf} = R_{fb} / R_{dc1}$

Where R_{dc1} is the output voltage divider resistor that is connected from the output of the converter to the input of the error amplifier. If the output circuit of Figure 42 is used, R_{dc1} would be 9.31 k + 453 Ω, or 9.76 kΩ. A gain of −25 dB is equal to a divider ratio of:

$A_V = 10^{(-25/20)} = 0.056$

so, $R_{fb} / R_{dc1} = 0.056$

or, $R_{fb} = 0.056 \times 9.76\ k\Omega = 546\ \Omega$

The closest standard value resistor is 560 Ω.

To offset the 2 Hz pole of the output filter, the error amplifier should have a zero of 2 Hz or slightly higher. For a 2 Hz zero, the compensation capacitor, C_{fb} can be calculated by:

$$C_{fb} = \frac{1}{2\ \pi\ R_{fb}\ 3\ Hz} = 95\ \mu F$$

100 μF is the closest standard value capacitor and would be a good choice. This solution will provide a phase margin of close to 90°. In practice the value of capacitance could be cut in half or more and probably remain stable. This can be tested in the circuit, or simulated with a model in SPICE or a similar analysis program.

The gain and phase plots of the completed loop are shown in Figures 46 and 47. These include the effects of all of the stages shown.

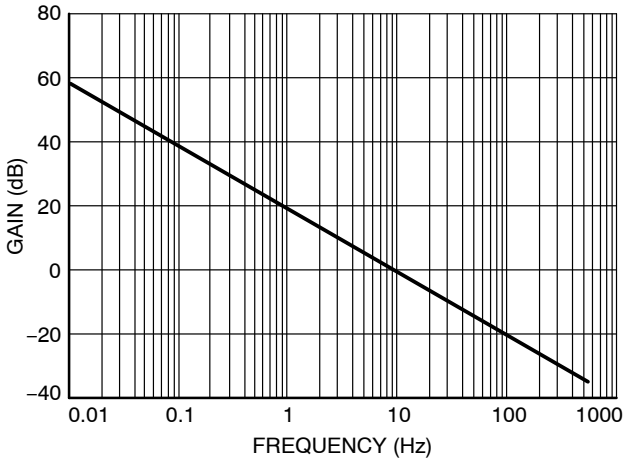


Figure 46. Loop Gain Plot

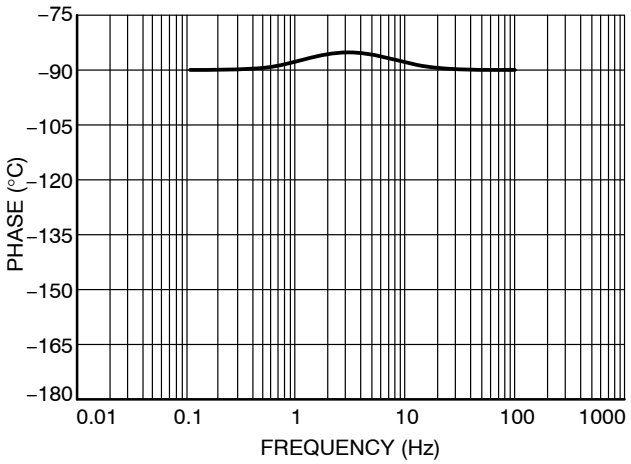
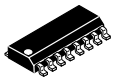


Figure 47. Loop Phase Plot



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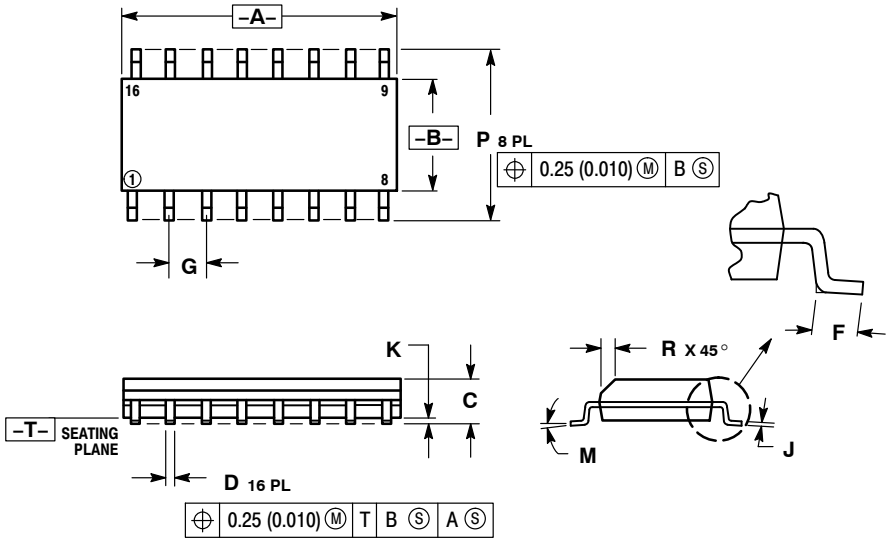


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

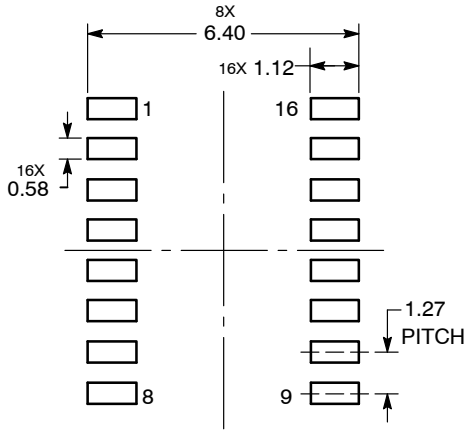
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



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