

# 2N5190G, 2N5191G, 2N5192G

## Silicon NPN Power Transistors

Silicon NPN power transistors are for use in power amplifier and switching circuits – excellent safe area limits. Complement to PNP 2N5194, 2N5195.

### Features

- Epoxy Meets UL 94 V-0 @ 0.125 in.
- These Devices are Pb-Free and are RoHS Compliant\*

### MAXIMUM RATINGS

| Rating  | Symbol         | Value          | Unit                      |
|---|----------------|----------------|---------------------------|
| Collector-Emitter Voltage<br>2N5190G<br>2N5191G<br>2N5192G                                | $V_{CEO}$      | 40<br>60<br>80 | Vdc                       |
| Collector-Base Voltage<br>2N5190G<br>2N5191G<br>2N5192G                                   | $V_{CBO}$      | 40<br>60<br>80 | Vdc                       |
| Emitter-Base Voltage  | $V_{EBO}$      | 5.0            | Vdc                       |
| Collector Current   | $I_C$          | 4.0            | Adc                       |
| Base Current  | $I_B$          | 1.0            | Adc                       |
| Total Device Dissipation<br>@ $T_C = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$          | 40<br>320      | W<br>mW/ $^\circ\text{C}$ |
| Operating and Storage Junction<br>Temperature Range                                       | $T_J, T_{stg}$ | -65 to +150    | $^\circ\text{C}$          |
| ESD – Human Body Model  | HBM            | 3B             | V                         |
| ESD – Machine Model   | MM             | C              | V                         |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Characteristic                       | Symbol          | Max  | Unit                      |
|--------------------------------------|-----------------|------|---------------------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 3.12 | $^\circ\text{C}/\text{W}$ |

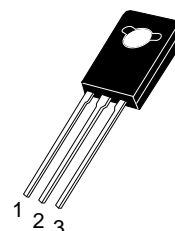
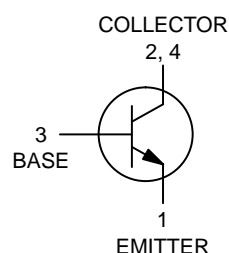
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

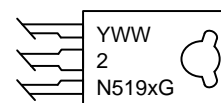
<http://onsemi.com>

**4.0 AMPERES  
NPN SILICON  
POWER TRANSISTORS  
40, 60, 80 VOLTS – 40 WATTS**



TO-225  
CASE 77-09  
STYLE 1

### MARKING DIAGRAM



Y = Year  
WW = Work Week  
2N519x = Device Code  
x = 0, 1, or 2  
G = Pb-Free Package

### ORDERING INFORMATION

| Device  | Package             | Shipping      |
|---------|---------------------|---------------|
| 2N5190G | TO-225<br>(Pb-Free) | 500 Units/Box |
| 2N5191G | TO-225<br>(Pb-Free) | 500 Units/Box |
| 2N5192G | TO-225<br>(Pb-Free) | 500 Units/Box |

## 2N5190G, 2N5191G, 2N5192G

### ELECTRICAL CHARACTERISTICS\* ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic   | Symbol        | Min                             | Max   | Unit |
|--|---------------|---------------------------------|---|------|
| <b>OFF CHARACTERISTICS</b>   |               |                                 |   |      |
| Collector–Emitter Sustaining Voltage (Note 1)<br>( $I_C = 0.1\text{ Adc}$ , $I_B = 0$ )<br>2N5190G<br>2N5191G<br>2N5192G   | $V_{CE(sus)}$ | 40<br>60<br>80                  | –<br>–<br>–                                   | Vdc  |
| Collector Cutoff Current<br>( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ )<br>2N5190G<br>( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )<br>2N5191G<br>( $V_{CE} = 80\text{ Vdc}$ , $I_B = 0$ )<br>2N5192G  | $I_{CEO}$     | –<br>–<br>–                     | 1.0<br>1.0<br>1.0                             | mAdc |
| Collector Cutoff Current<br>( $V_{CE} = 40\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ )<br>2N5190G<br>( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ )<br>2N5191G<br>( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ )<br>2N5192G<br>( $V_{CE} = 40\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )<br>2N5190G<br>( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )<br>2N5191G<br>( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )<br>2N5192G | $I_{CEX}$     | –<br>–<br>–<br>–<br>–<br>–<br>– | 0.1<br>0.1<br>0.1<br>0.1<br>2.0<br>2.0<br>2.0 | mAdc |
| Collector Cutoff Current<br>( $V_{CB} = 40\text{ Vdc}$ , $I_E = 0$ )<br>2N5190G<br>( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ )<br>2N5191G<br>( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ )<br>2N5192G  | $I_{CBO}$     | –<br>–<br>–                     | 0.1<br>0.1<br>0.1                             | mAdc |
| Emitter Cutoff Current<br>( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )  | $I_{EBO}$     | –                               | 1.0   | mAdc |
| <b>ON CHARACTERISTICS (Note 1)</b>   |               |                                 |   |      |
| DC Current Gain<br>( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )<br>2N5190G/2N5191G<br>2N5192G<br>( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )<br>2N5190G/2N5191G<br>2N5192G  | $h_{FE}$      | 25<br>20<br>10<br>7.0           | 100<br>80<br>–<br>–                           | –    |
| Collector–Emitter Saturation Voltage<br>( $I_C = 1.5\text{ Adc}$ , $I_B = 0.15\text{ Adc}$ )<br>( $I_C = 4.0\text{ Adc}$ , $I_B = 1.0\text{ Adc}$ )  | $V_{CE(sat)}$ | –<br>–                          | 0.6<br>1.4                                    | Vdc  |
| Base–Emitter On Voltage<br>( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )  | $V_{BE(on)}$  | –                               | 1.2   | Vdc  |
| <b>DYNAMIC CHARACTERISTICS</b>   |               |                                 |   |      |
| Current–Gain – Bandwidth Product<br>( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )   | $f_T$         | 2.0                             | –   | MHz  |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

\*JEDEC Registered Data.

1. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

# 2N5190G, 2N5191G, 2N5192G

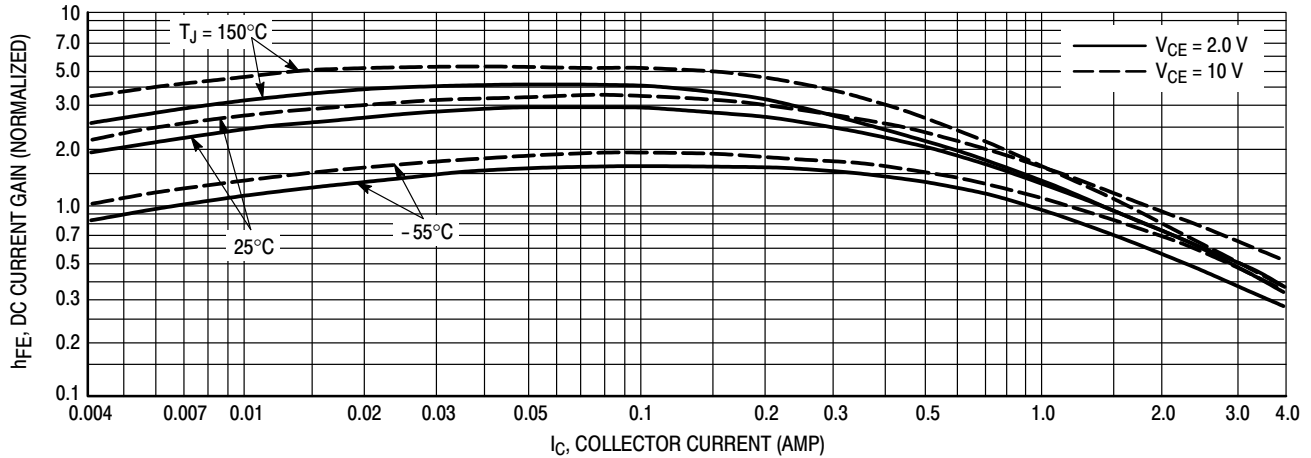


Figure 1. DC Current Gain

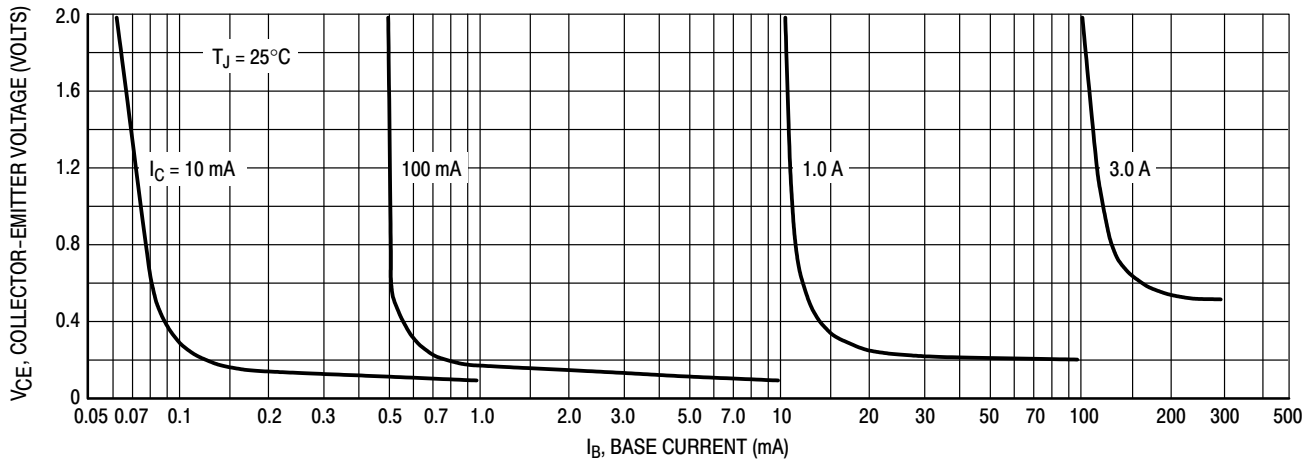


Figure 2. Collector Saturation Region

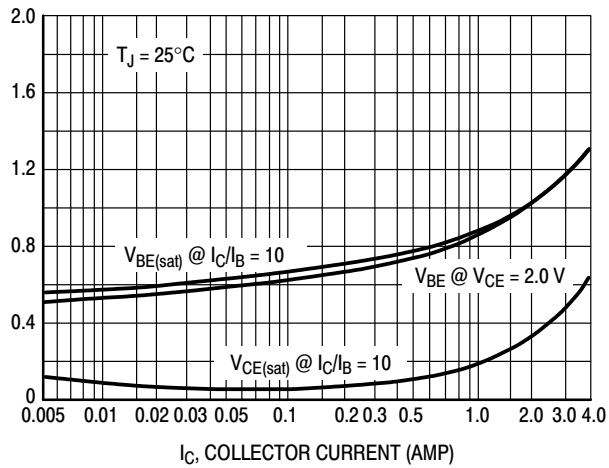


Figure 3. "On" Voltages

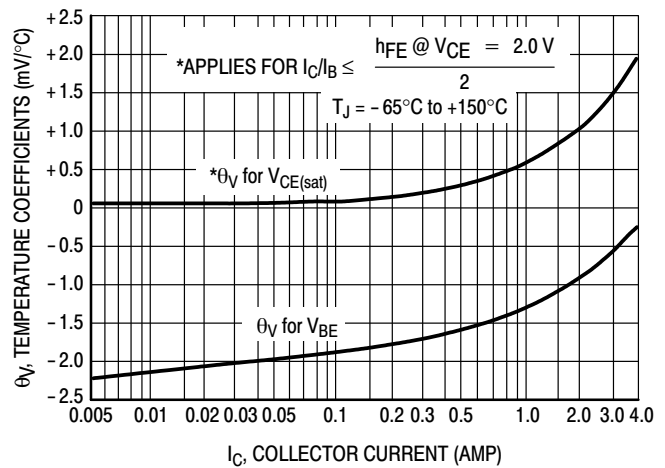


Figure 4. Temperature Coefficients

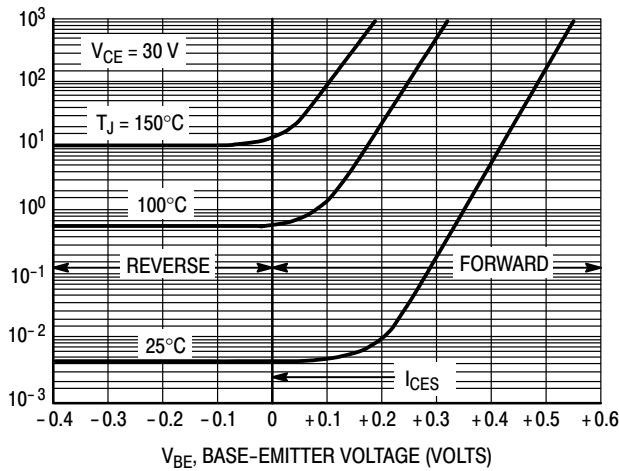


Figure 5. Collector Cut-Off Region

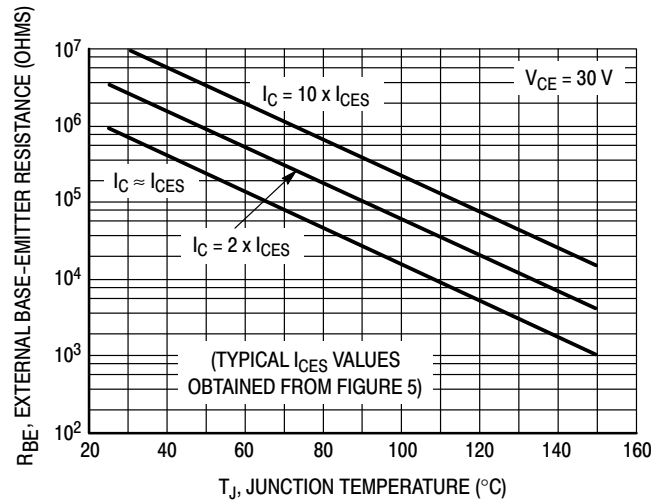


Figure 6. Effects of Base-Emitter Resistance

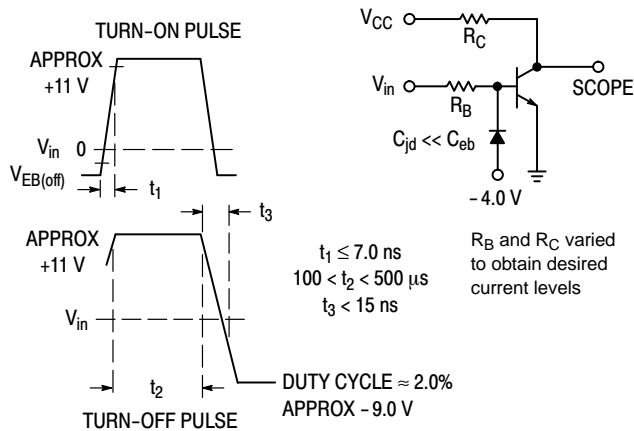


Figure 7. Switching Time Equivalent Test Circuit

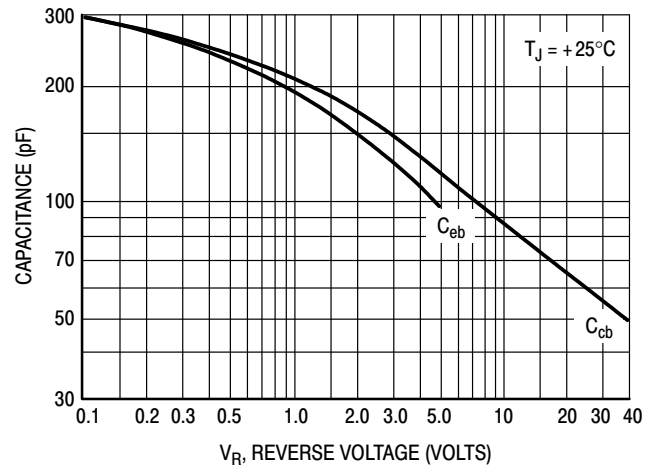


Figure 8. Capacitance

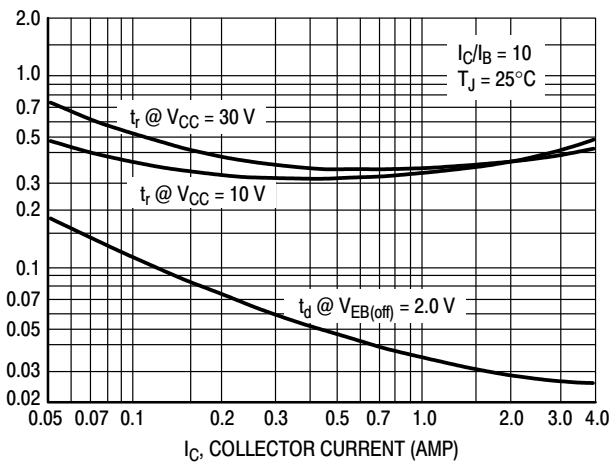


Figure 9. Turn-On Time

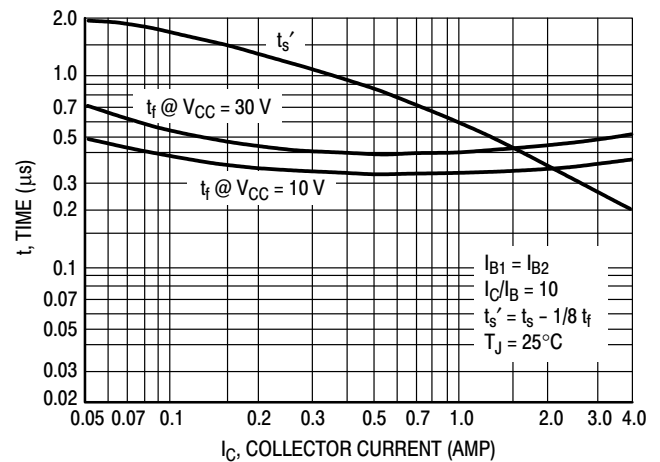
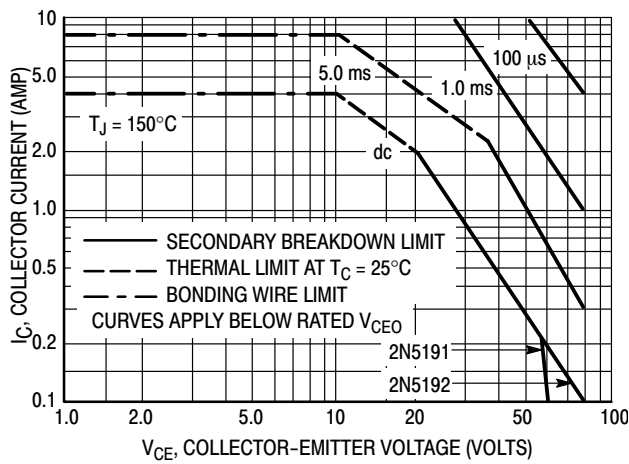
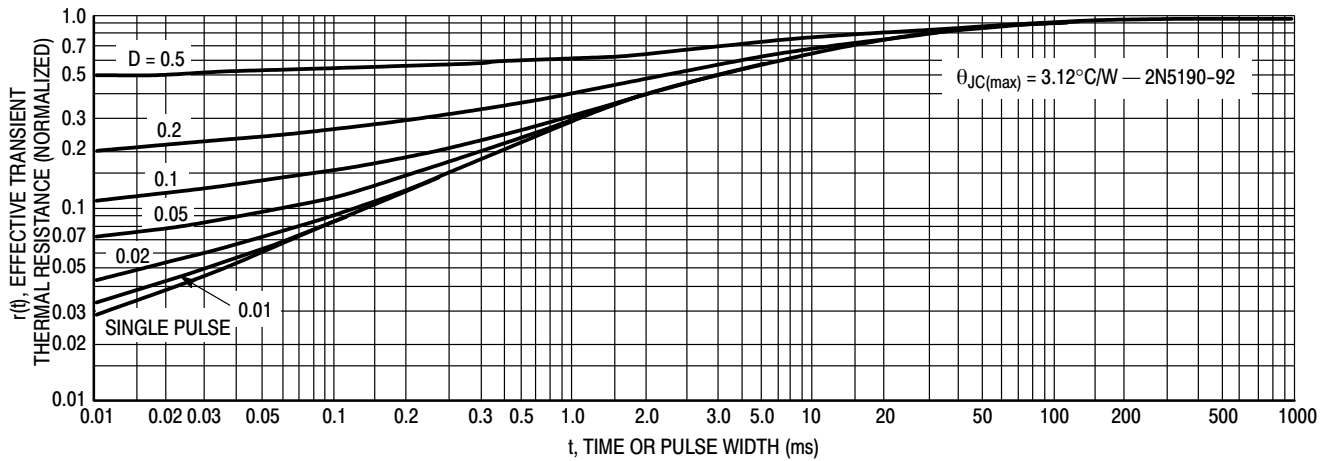


Figure 10. Turn-Off Time

## 2N5190G, 2N5191G, 2N5192G

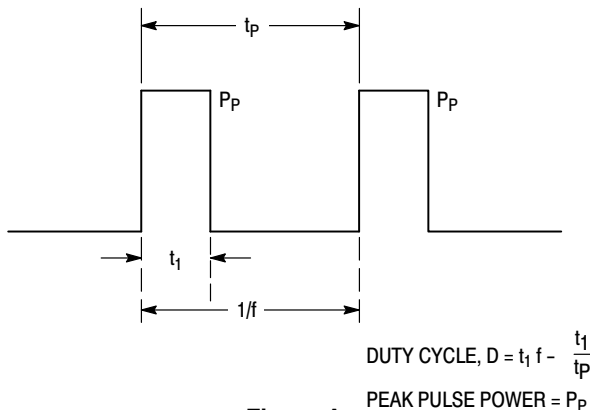


**Figure 11. Rating and Thermal Data  
Active-Region Safe Operating Area**



**Figure 12. Thermal Response**

### DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



**Figure A**

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find  $\theta_{JC}(t)$ , multiply the value obtained from Figure 12 by the steady state value  $\theta_{JC}$ .

Example:

The 2N5190 is dissipating 50 watts under the following conditions:  $t_1 = 0.1$  ms,  $t_p = 0.5$  ms. ( $D = 0.2$ ).

Using Figure 12, at a pulse width of 0.1 ms and  $D = 0.2$ , the reading of  $r(t_1, D)$  is 0.27.

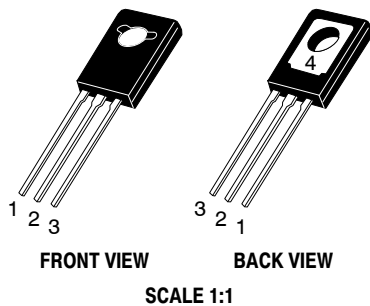
The peak rise in function temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ\text{C}$$

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

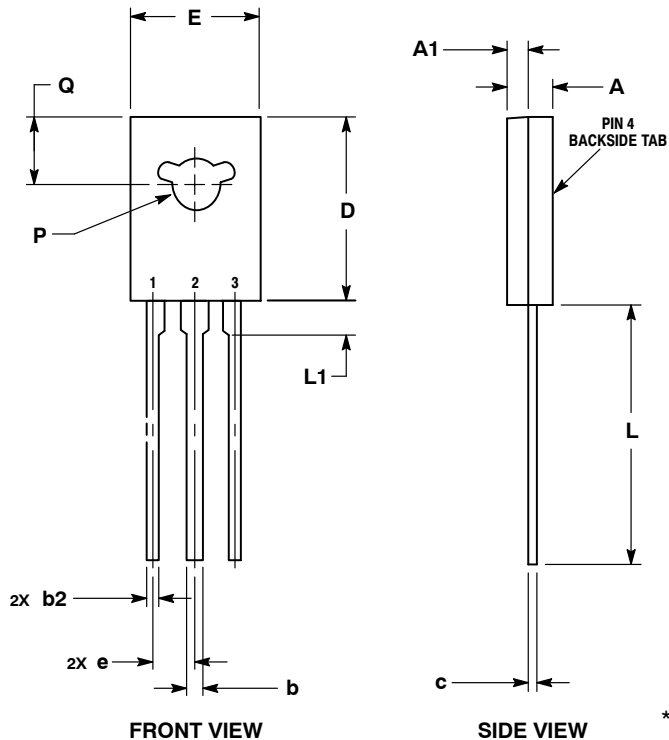
ON Semiconductor®

ON



TO-225  
CASE 77-09  
ISSUE AD

DATE 25 MAR 2015

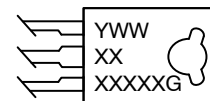


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

| MILLIMETERS |       |       |
|-------------|-------|-------|
| DIM         | MIN   | MAX   |
| A           | 2.40  | 3.00  |
| A1          | 1.00  | 1.50  |
| b           | 0.60  | 0.90  |
| b2          | 0.51  | 0.88  |
| c           | 0.39  | 0.63  |
| D           | 10.60 | 11.10 |
| E           | 7.40  | 7.80  |
| e           | 2.04  | 2.54  |
| L           | 14.50 | 16.63 |
| L1          | 1.27  | 2.54  |
| P           | 2.90  | 3.30  |
| Q           | 3.80  | 4.20  |

## GENERIC MARKING DIAGRAM\*



Y = Year  
WW = Work Week  
XXXXX = Device Code  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

|   |   |   |   |   |
|---|---|---|---|---|
| STYLE 1:<br>PIN 1. EMITTER<br>2., 4. COLLECTOR<br>3. BASE | STYLE 2:<br>PIN 1. CATHODE<br>2., 4. ANODE<br>3. GATE | STYLE 3:<br>PIN 1. BASE<br>2., 4. COLLECTOR<br>3. EMITTER | STYLE 4:<br>PIN 1. ANODE 1<br>2., 4. ANODE 2<br>3. GATE | STYLE 5:<br>PIN 1. MT 1<br>2., 4. MT 2<br>3. GATE     |
| STYLE 6:<br>PIN 1. CATHODE<br>2., 4. GATE<br>3. ANODE     | STYLE 7:<br>PIN 1. MT 1<br>2., 4. GATE<br>3. MT 2     | STYLE 8:<br>PIN 1. SOURCE<br>2., 4. GATE<br>3. DRAIN      | STYLE 9:<br>PIN 1. GATE<br>2., 4. DRAIN<br>3. SOURCE    | STYLE 10:<br>PIN 1. SOURCE<br>2., 4. DRAIN<br>3. GATE |

|                  |             |   |
|------------------|-------------|---|
| DOCUMENT NUMBER: | 98ASB42049B | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | TO-225      | PAGE 1 OF 1   |

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative