

# Low Voltage Compador

## SA575

The SA575 is a precision dual gain control circuit designed for low voltage applications. The SA575's channel 1 is an expander, while channel 2 can be configured either for expander, compressor, or automatic level controller (ALC) application.

### Features

- Operating Voltage Range from 3.0 V to 7.0 V
- Reference Voltage of  $100 \text{ mV}_{\text{RMS}} = 0 \text{ dB}$
- One Dedicated Summing Op Amp Per Channel and Two Extra Uncommitted Op Amps
- $600 \Omega$  Drive Capability
- Single or Split Supply Operation
- Wide Input/Output Swing Capability
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

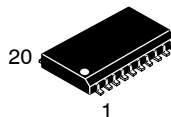
### Applications

- Portable Communications
- Cellular Radio
- Cordless Telephone
- Consumer Audio
- Portable Broadcast Mixers
- Wireless Microphones
- Modems
- Electric Organs
- Hearing Aids

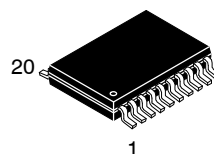


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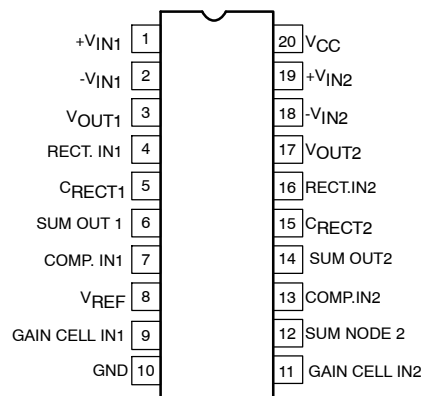
**SOIC-20 WB  
D SUFFIX  
CASE 751D**



**TSSOP-20  
DTB SUFFIX  
CASE 948E**

### PIN CONNECTIONS

#### D\* and DTB Packages



\*Available in large SOL package only.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 13 of this data sheet.

# SA575

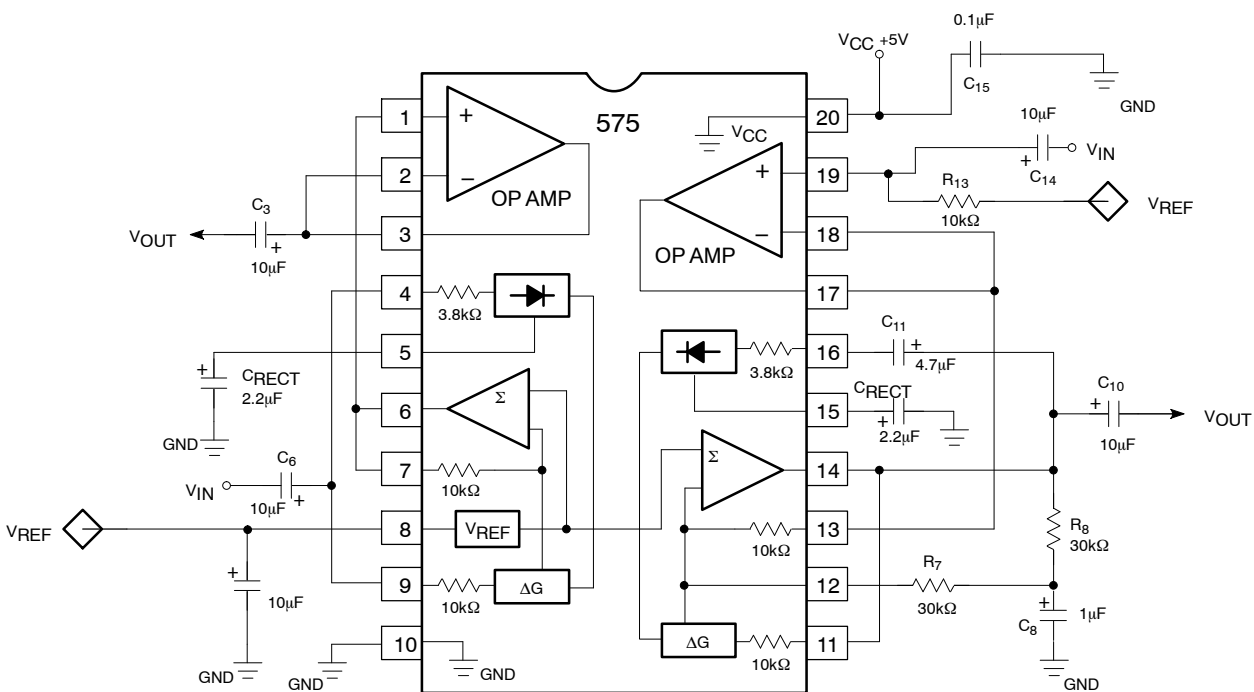


Figure 1. Block Diagram and Test Circuit

## PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	+VIN1	Non-Inverted Input 1
2	-VIN1	Inverted Input 1
3	VOUT	Output
4	RECT. IN1	Rectifier 1 Input
5	CRECT1	External Capacitor Pinout for Rectifier 1
6	SUM OUT1	Summation Output 1
7	COMP. IN1	Compensator Pin
8	VREF	Voltage Reference
9	GAIN CELL IN1	Variable Gain Cell Input 1
10	GND	Ground
11	GAIN CELL IN2	Variable Gain Cell Input 2
12	SUM NODE 2	Summation Node 2
13	COMP. IN2	Compensator Pin
14	SUM OUT2	Summation Output 2
15	CRECT2	External Capacitor Pinout for Rectifier 2
16	RECT. IN2	Rectifier 2 Input
17	VOUT2	Output 2
18	-VIN2	Inverted Input 2
19	+VIN2	Non-Inverted Input 2
20	VCC	Positive Power Supply

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Single Supply Voltage	$V_{CC}$	-0.3 to 8.0	V
Voltage Applied to Any Other Pin	$V_{IN}$	-0.3 to ( $V_{CC} + 0.3$ )	V
Operating Ambient Temperature Range	$T_A$	-40 to +85	°C
Operating Junction Temperature	$T_J$	150	°C
Storage Temperature Range	$T_{STG}$	150	°C
Thermal Impedance	SOIC TSSOP $\theta_{JA}$	87 124	°C/W
Maximum Power Dissipation	SOIC TSSOP $P_D$	1116 1068	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**DC ELECTRICAL CHARACTERISTICS** Typical values are at  $T_A = 25^\circ\text{C}$ . Minimum and Maximum values are for the full operating temperature range: -40 to +85°C for SA575, except SSOP package is tested at +25°C only.  $V_{CC} = 5.0\text{ V}$ , unless otherwise stated. Both channels are tested in the Expander mode (see Test Circuit).

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>FOR COMPANDOR, INCLUDING SUMMING AMPLIFIER</b>						
Supply Voltage (Note 1)	$V_{CC}$	–	3.0	5.0	7.0	V
Supply Current	$I_{CC}$	No Signal	3.0	4.2	5.5	mA
Reference Voltage (Note 2)	$V_{REF}$	$V_{CC} = 5.0\text{ V}$	2.4	2.5	2.6	V
Summing Amp Output Load	$R_L$	–	10	–	–	k $\Omega$
Total Harmonic Distortion	THD	1.0 kHz, 0 dB, BW = 3.5 kHz	–	0.12	1.5	%
Output Voltage Noise	$E_{NO}$	BW = 20 kHz, $R_S = 0\ \Omega$	–	6.0	30	$\mu\text{V}$
Unity Gain Level	0dB	1.0 kHz	-1.5	–	1.5	dB
Output Voltage Offset	$V_{OS}$	No Signal	-150	–	150	mV
Output DC Shift		No Signal to 0 dB	-100	–	100	mV
Tracking Error Relative to 0 dB		Gain Cell Input = 0 dB, 1.0 kHz Rectifier Input = 6.0 dB, 1.0 kHz	-1.0	–	1.0	dB
		Gain Cell Input = 0 dB, 1.0 kHz Rectifier Input = -30 dB, 1.0 kHz	-1.0	–	1.0	dB
Crosstalk		1.0 kHz, 0 dB, $C_{REF} = 220\ \mu\text{F}$	–	-80	-65	dB

**FOR OPERATIONAL AMPLIFIER**

Output Swing	$V_O$	$R_L = 10\text{ k}\Omega$	$V_{CC}-0.4$	$V_{CC}$	–	V
Output Load	$R_L$	1.0 kHz	600	–	–	$\Omega$
Input Common-Mode Range	CMR	–	0	–	$V_{CC}$	V
Common-Mode Rejection Ratio	CMRR	–	60	80	–	dB
Input Bias Current	$I_B$	$V_{IN} = 0.5\text{ V to }4.5\text{ V}$	-1.0	–	1.0	$\mu\text{A}$
Input Offset Voltage	$V_{OS}$	–	–	3.0	–	mV
Open-Loop Gain	$A_{VOL}$	$R_L = 10\text{ k}\Omega$	–	80	–	dB
Slew Rate	SR	Unity Gain	–	1.0	–	V/ $\mu\text{s}$
Bandwidth	GBW	Unity Gain	–	3.0	–	MHz
Input Voltage Noise	$E_{NI}$	BW = 20 kHz	–	2.5	–	$\mu\text{V}$
Power Supply Rejection Ratio	PSRR	1.0 kHz, 250 mV	–	60	–	dB

1. Operation down to  $V_{CC} = 2.0\text{ V}$  is possible, but performance is reduced. See curves in Figures 6 and 7.
2. Reference voltage,  $V_{REF}$  is typically at  $1/2\ V_{CC}$ .

## Functional Description

This section describes the basic subsystems and applications of the SA575 Compressor. More theory of operation on compressors can be found in AND8159 and AND8160. The typical applications of the SA575 low voltage compressor in an Expander (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 2, 3, and 4 respectively.

The SA575 has two channels for a complete compressing system. The left channel, A, can be configured as a 1:2 Expander while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expander or an ALC. Each channel consists of the basic compressing building blocks of rectifier cell, variable gain cell, summing amplifier and  $V_{REF}$  cell. In addition, the SA575 has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre-emphasis/de-emphasis or buffering.

Figure 5 shows the complete schematic for the applications demo board. Channel A is configured as an expander while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch,  $S_1$ , toggles the circuit between compressor and ALC mode. Jumpers  $J_1$  and  $J_2$  can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for  $R_1$ ,  $R_2$ ,  $C_1$ ,  $C_2$ ,  $R_{10}$ ,  $R_{11}$ ,  $C_{10}$  and  $C_{11}$  so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20 Hz to 20 kHz.

The most common configuration is as a unity gain non-inverting buffer where  $R_1$ ,  $C_1$ ,  $C_2$ ,  $R_{10}$ ,  $C_{10}$  and  $C_{11}$  are eliminated and  $R_2$  and  $R_{11}$  are shorted. Capacitors  $C_3$ ,  $C_5$ ,  $C_8$ , and  $C_{12}$  are for DC blocking. In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors  $C_4$  and  $C_9$  are for setting the attack and release time constant.

$C_6$  is for decoupling and stabilizing the voltage reference circuit. The value of  $C_6$  should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be.  $R_{12}$  provides DC reference voltage to the amplifier of channel B.  $R_6$  and  $R_7$  provide a DC feedback path for the summing amp of channel B, while  $C_7$  is a short-circuit to ground for signals.  $C_{14}$  and  $C_{15}$  are for power supply decoupling.  $C_{14}$  can also be eliminated if the power supply is well regulated with very low noise and ripple.

## Demonstrated Performance

The applications demo board was built and tested for a frequency range of 20 Hz to 20 kHz with the component values as shown in Figure 5 and  $V_{CC} = 5.0$  V. In the expander mode, the typical input dynamic range was from -34 dB to +12 dB where 0 dB is equal to 100 mV<sub>RMS</sub>. The typical unity gain level measured at 0 dB @ 1.0 kHz input was  $\pm 0.5$  dB and the typical tracking error was  $\pm 0.1$  dB for input range of -30 to +10 dB.

In the compressor mode, the typical input dynamic range was from -42 dB to  $\pm 18$  dB with a tracking error  $\pm 0.1$  dB and the typical unity gain level was  $\pm 0.5$  dB.

In the ALC mode, the typical input dynamic range was from -42 dB to +8.0 dB with typical output deviation of  $\pm 0.2$  dB about the nominal output of 0 dB. For input greater than +9.0 dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of  $R_6$  and  $R_7$  to 20 k $\Omega$  each. The second is to add a current limiting resistor in series with  $C_{12}$  at Pin 13. The third is to add a compensating capacitor of about 22 to 30 pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18 dB yielding a dynamic range of over 60 dB.

### Expander

The typical expander configuration is shown in Figure 2. The variable gain cell and the rectifier cell are in the signal input path. The  $V_{REF}$  is always  $1/2 V_{CC}$  to provide the maximum headroom without clipping. The 0 dB ref is 100 mV<sub>RMS</sub>. The input is AC coupled through  $C_5$ , and the output is AC coupled through  $C_3$ . If in a system the inputs and outputs are AC coupled, then  $C_3$  and  $C_5$  can be eliminated, thus requiring only one external component,  $C_4$ . The variable gain cell and rectifier cell are DC coupled so any offset voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the

accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.

The expander gain expression and the attack and release time constant is given by Equation 1 and Equation 2, respectively.

$$\text{Expander gain} = \left( \frac{4V_{IN(\text{avg})}}{3.8 \text{ k}\Omega \times 100 \mu\text{A}} \right)^2 \quad (\text{eq. 1})$$

$$\text{where } V_{IN(\text{avg})} = 0.95V_{IN(\text{RMS})}$$

$$\tau_R = \tau_A = 10 \text{ k}\Omega \times C_{RECT} = 10 \text{ k}\Omega \times C_4 \quad (\text{eq. 2})$$

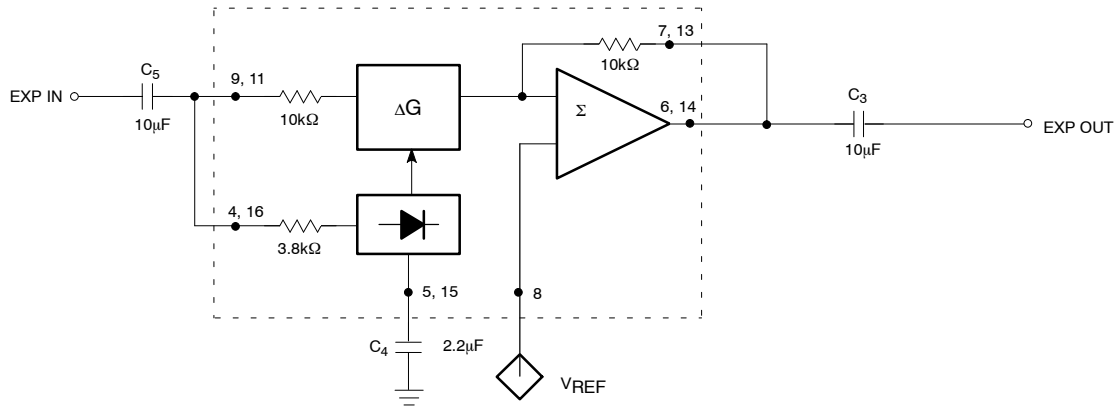


Figure 2. Typical Expander Configuration

### Compressor

The typical compressor configuration is shown in Figure 3. In this mode, the rectifier cell and variable gain cell are in the feedback path.  $R_6$  and  $R_7$  provide the DC feedback to the summing amplifier. The input is AC coupled through  $C_{12}$  and output is AC coupled through  $C_8$ . In a system with inputs and outputs AC coupled,  $C_8$  and  $C_{12}$  could be eliminated and only  $R_6$ ,  $R_7$ ,  $C_7$ , and  $C_{13}$  would be required. If the external components  $R_6$ ,  $R_7$  and  $C_7$  are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from

the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.

The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

$$\text{Compressor gain} = \left[ \frac{3.8 \text{ k}\Omega \times 100 \text{ }\mu\text{A}}{4V_{IN(\text{avg})}} \right]^{1/2} \quad (\text{eq. 3})$$

$$\text{where } V_{IN(\text{avg})} = 0.95V_{IN(\text{RMS})}$$

$$\tau_R = \tau_A = 10 \text{ k}\Omega \times C_{\text{RECT}} = 10 \text{ k}\Omega \times C_4 \quad (\text{eq. 4})$$

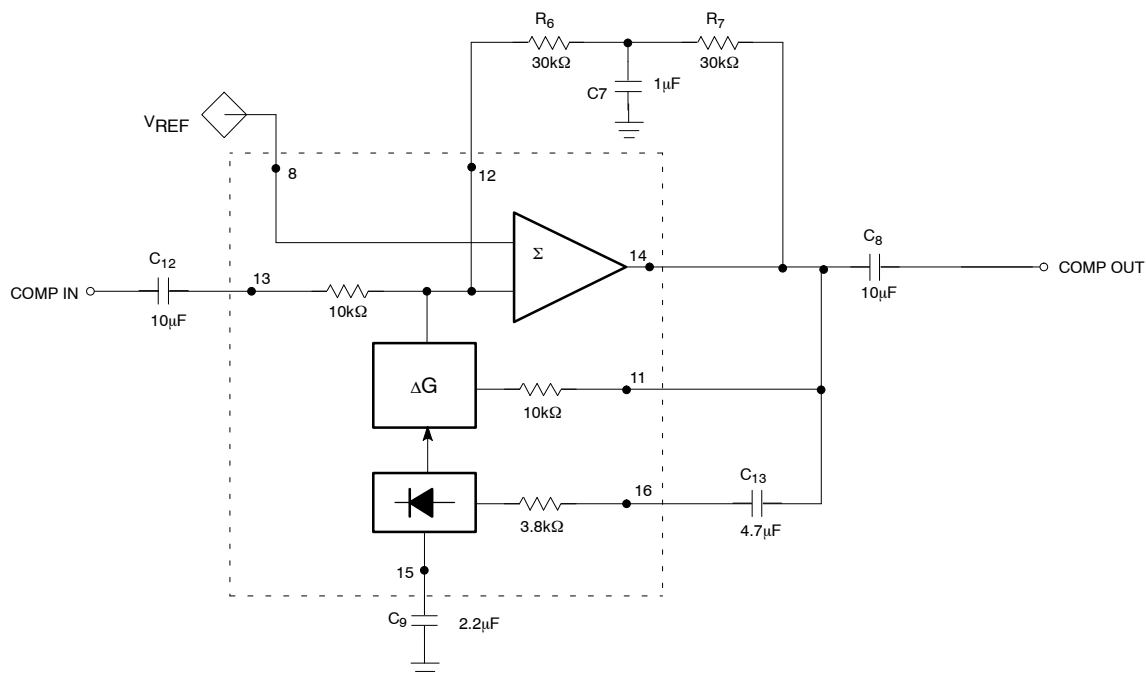


Figure 3. Typical Compressor Configuration

### Automatic Level Control

The typical Automatic Level Control circuit configuration is shown in Figure 4. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through  $C_{12}$  and  $C_{13}$  and the output is AC coupled through  $C_8$ . Once again, as in the previous cases, if the system input and output signals are already AC coupled, then  $C_{12}$ ,  $C_{13}$  and  $C_8$  could be eliminated. Concerning the compressor, removing  $R_6$ ,  $R_7$  and  $C_7$  will cause motor-boating in

absence of signals.  $C_{COMP}$  is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60 dB with the output within  $\pm 0.5$  dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

$$\text{ALC gain} = \frac{3.8 \text{ k}\Omega \times 100 \text{ }\mu\text{A}}{4V_{IN(\text{avg})}} \quad (\text{eq. 5})$$

$$\tau_R = \tau_A = 10 \text{ k}\Omega \times C_{RECT} = 10 \text{ k}\Omega \times C_9 \quad (\text{eq. 6})$$

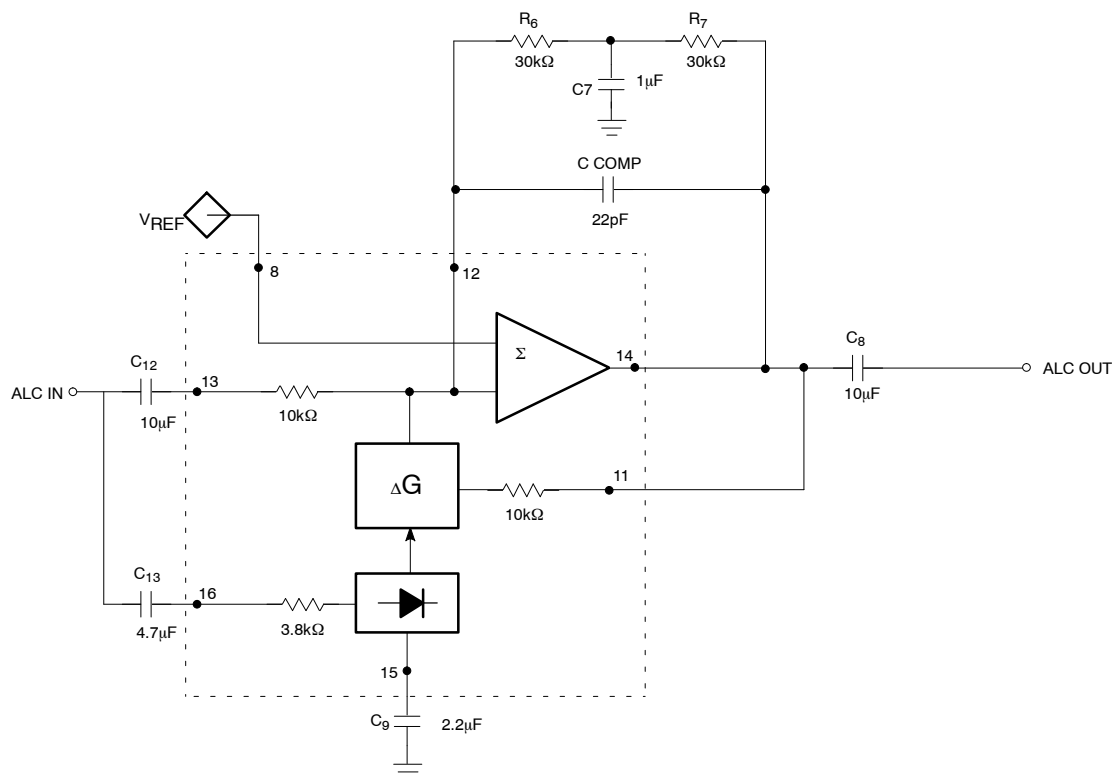


Figure 4. Typical ALC Configuration

# SA575

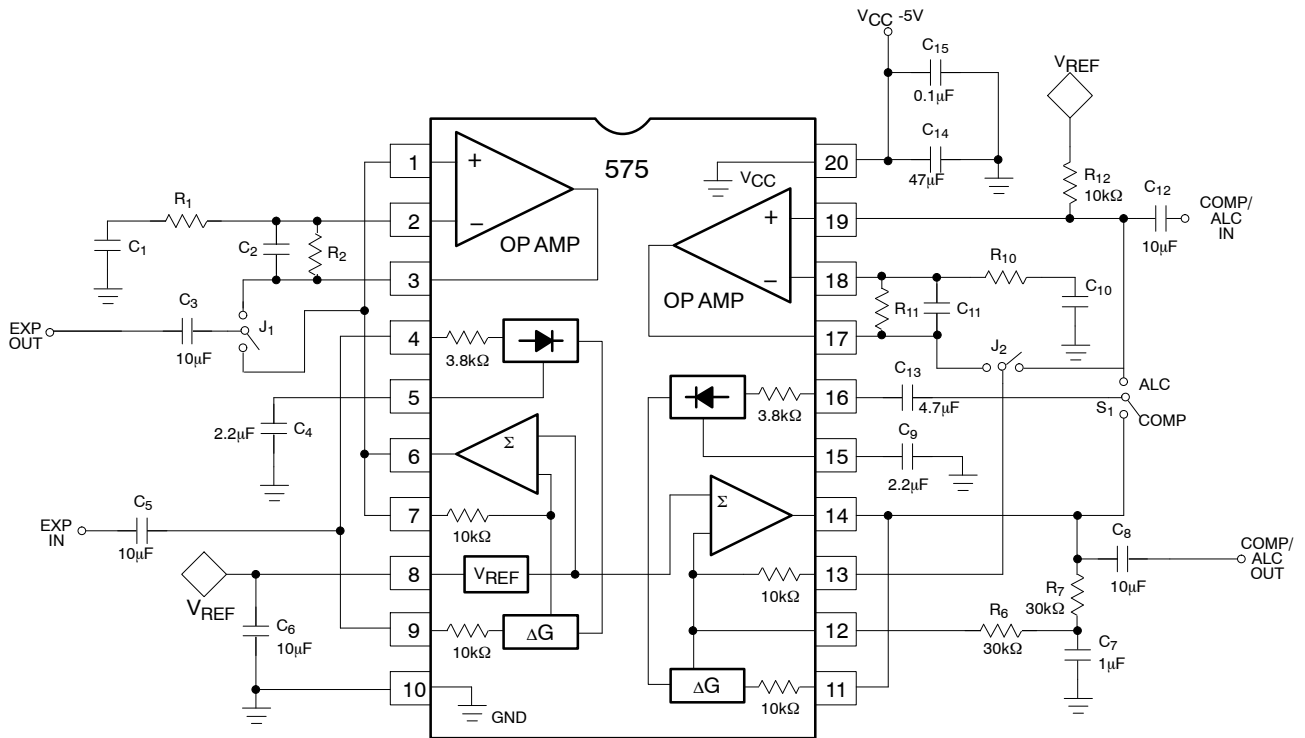


Figure 5. SA575 Low Voltage Expander/Compressor/ALC Demo Board



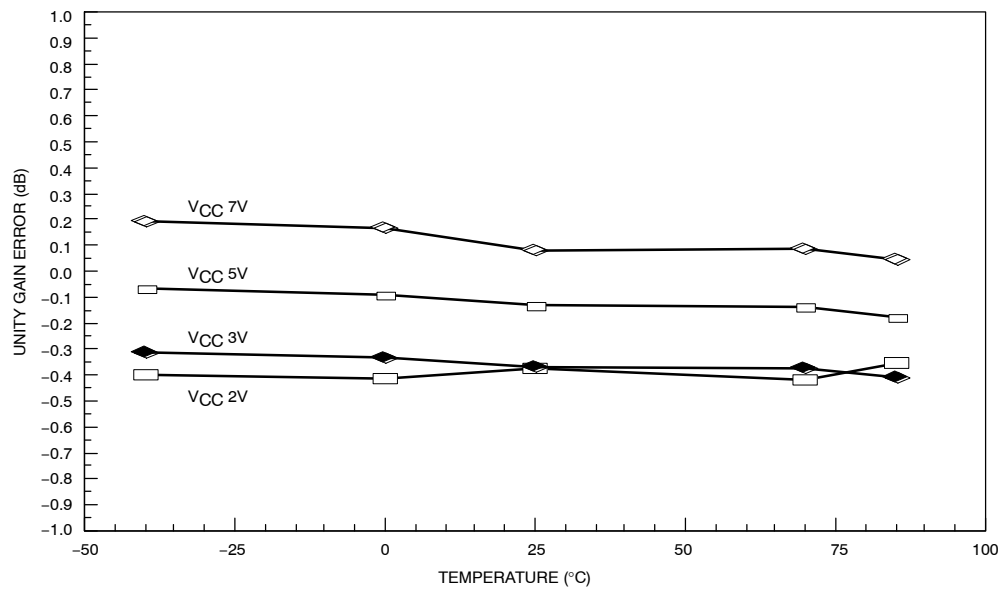


Figure 6. Unity Gain Error vs. Temperature and  $V_{CC}$

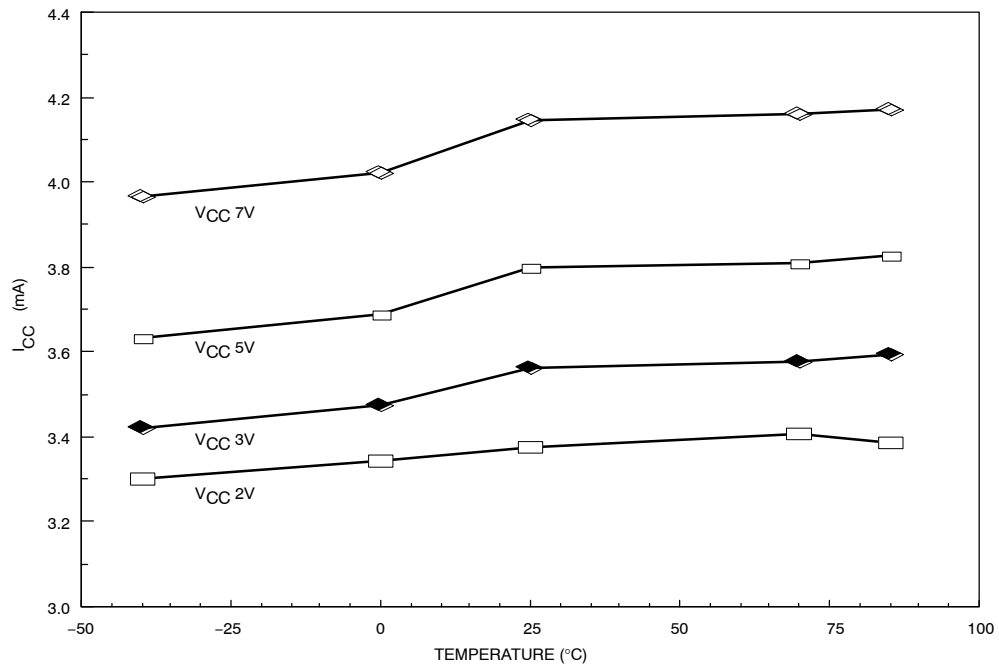


Figure 7.  $I_{CC}$  vs. Temperature and  $V_{CC}$

## TYPICAL PERFORMANCE CHARACTERISTICS

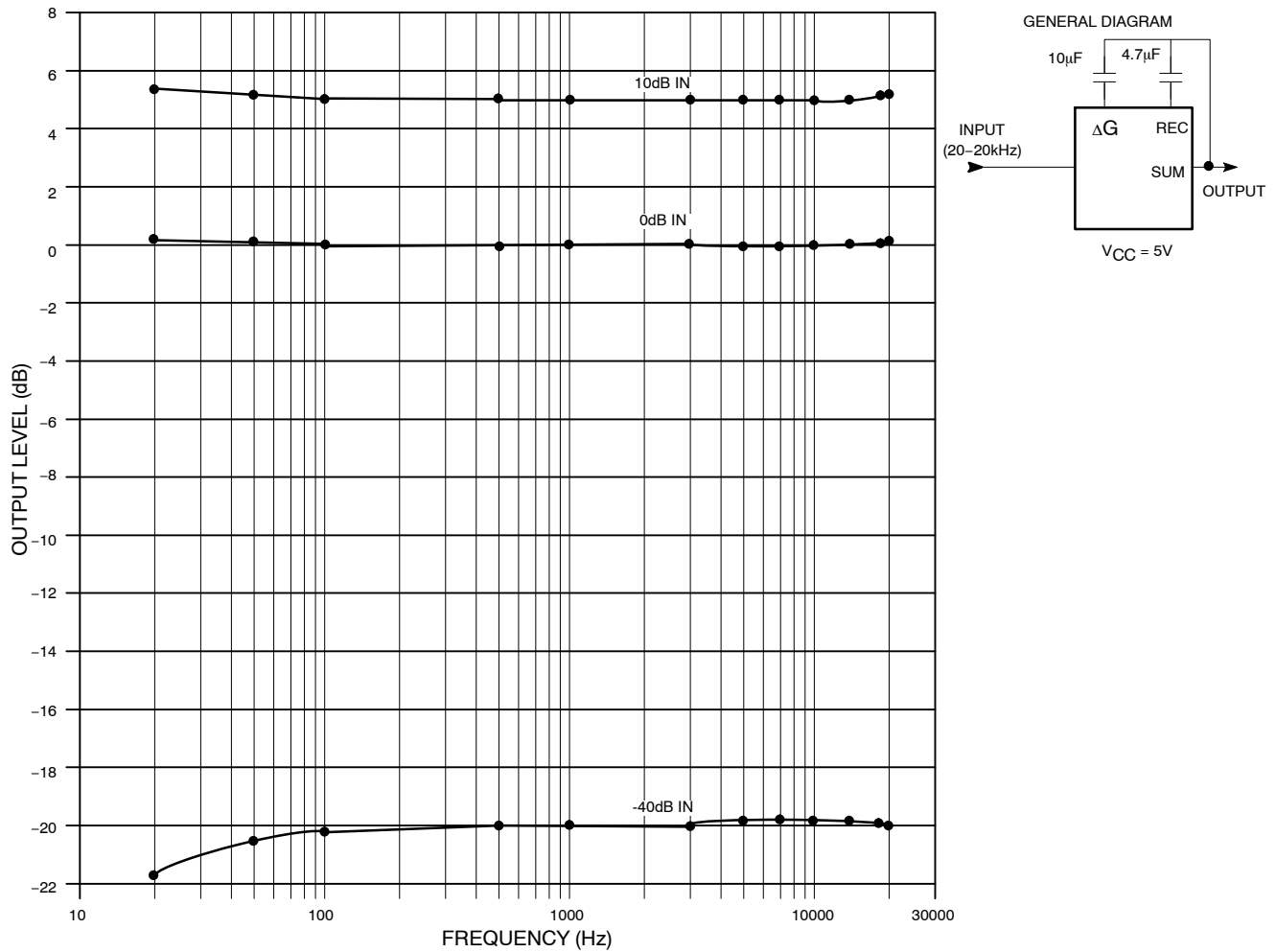


Figure 8. Compressor Output Frequency Response

## TYPICAL PERFORMANCE CHARACTERISTICS

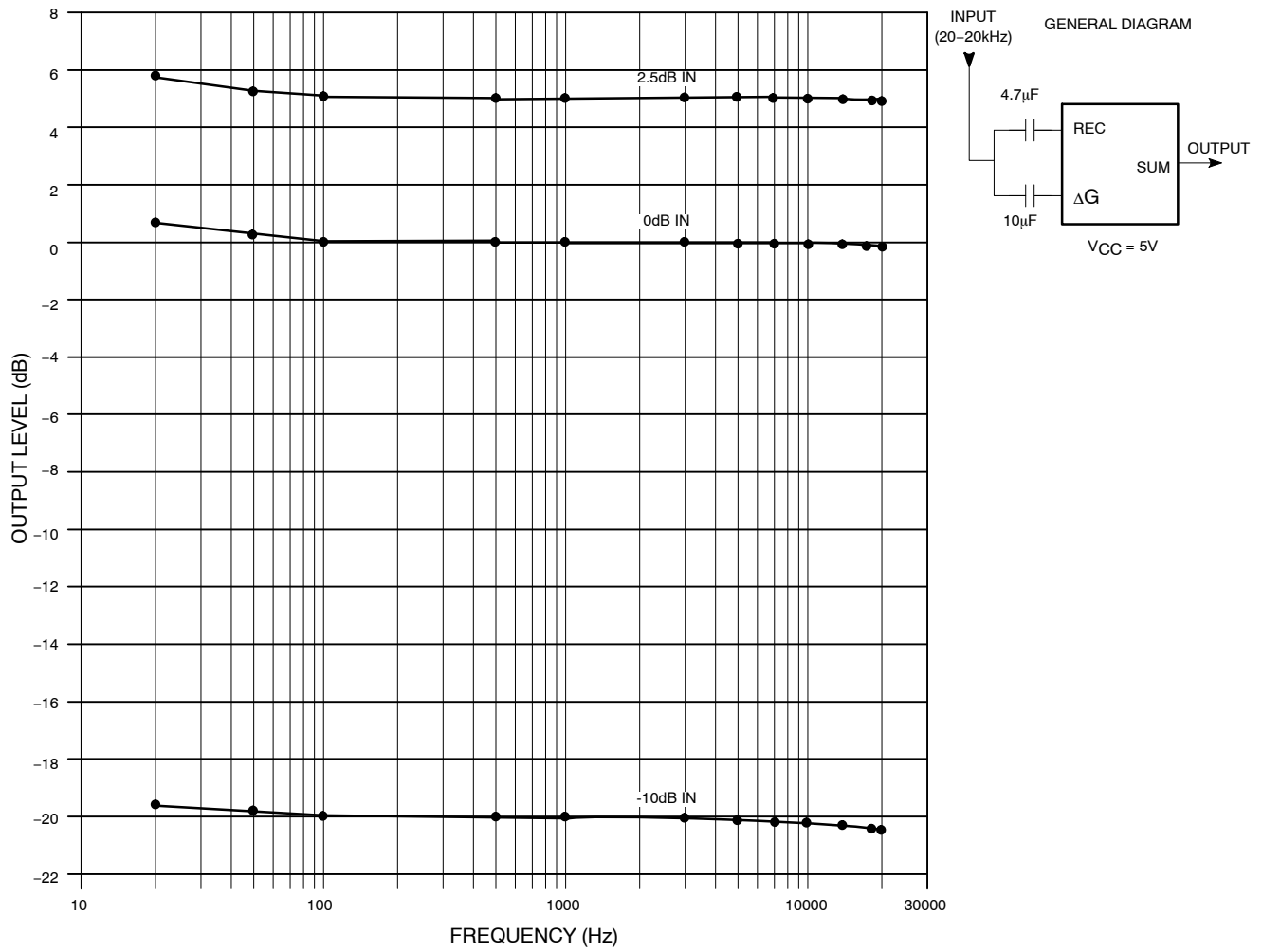


Figure 9. Expander Output Frequency Response

# SA575

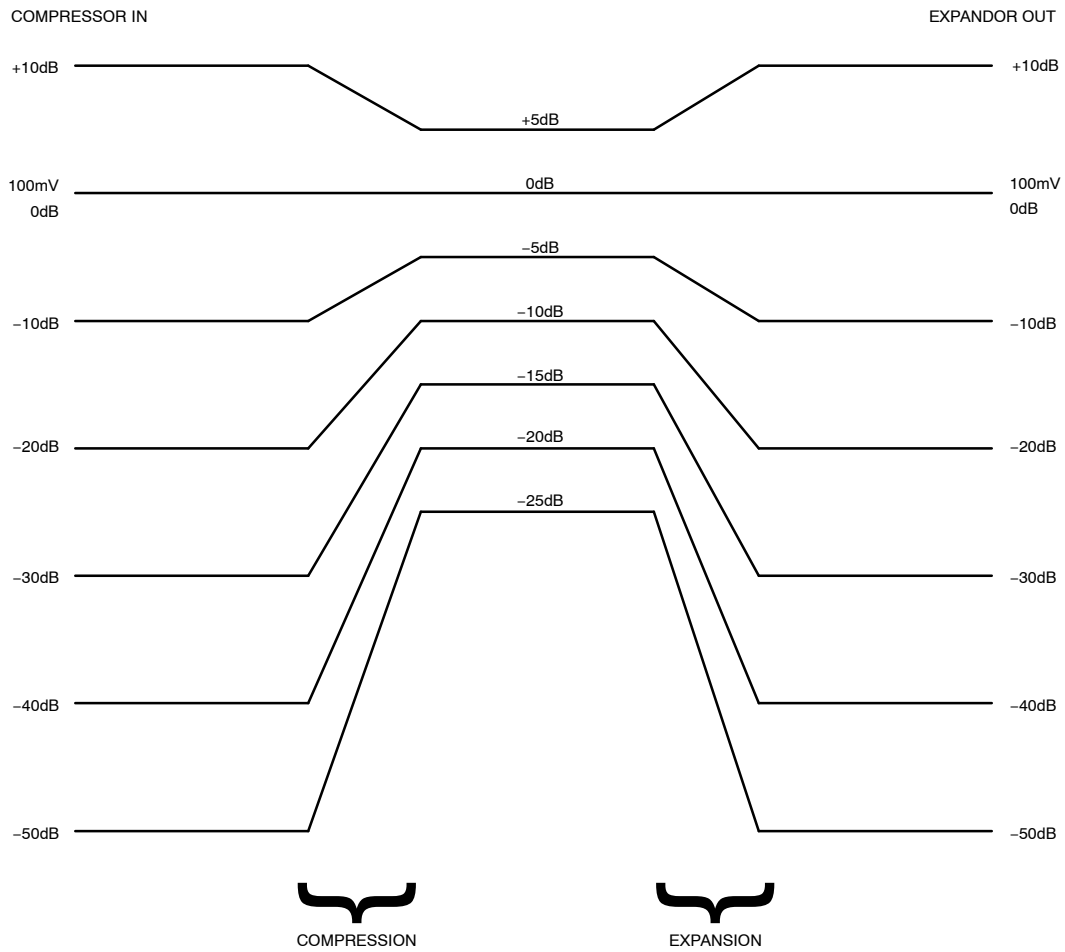


Figure 10. The Compressing Function

# SA575

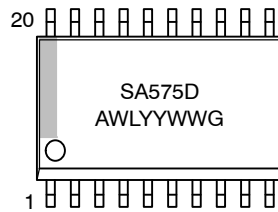
## ORDERING INFORMATION

Device	Package	Temperature Range	Shipping†
SA575DR2G	SOIC-20 WB (Pb-Free)	-40 to +85°C	1000 / Tape & Reel
SA575DTBR2G	TSSOP-20 (Pb-Free)	-40 to +85°C	2500 / Tape & Reel

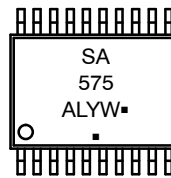
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## MARKING DIAGRAMS

**SOIC-20 WB  
D SUFFIX  
CASE 751D**

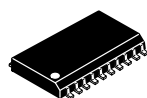


**TSSOP-20  
DTB SUFFIX  
CASE 948E**



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ▪ = Pb-Free Package

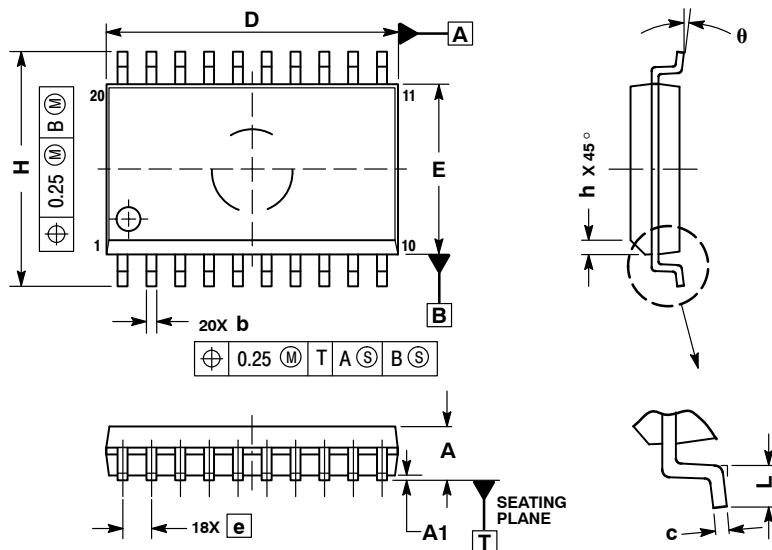
(Note: Microdot may be in either location)



SCALE 1:1

### SOIC-20 WB CASE 751D-05 ISSUE H

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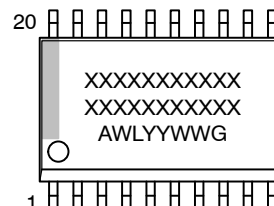


#### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

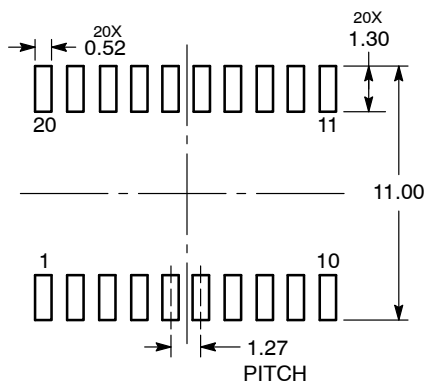
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

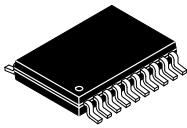
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DESCRIPTION:	SOIC-20 WB	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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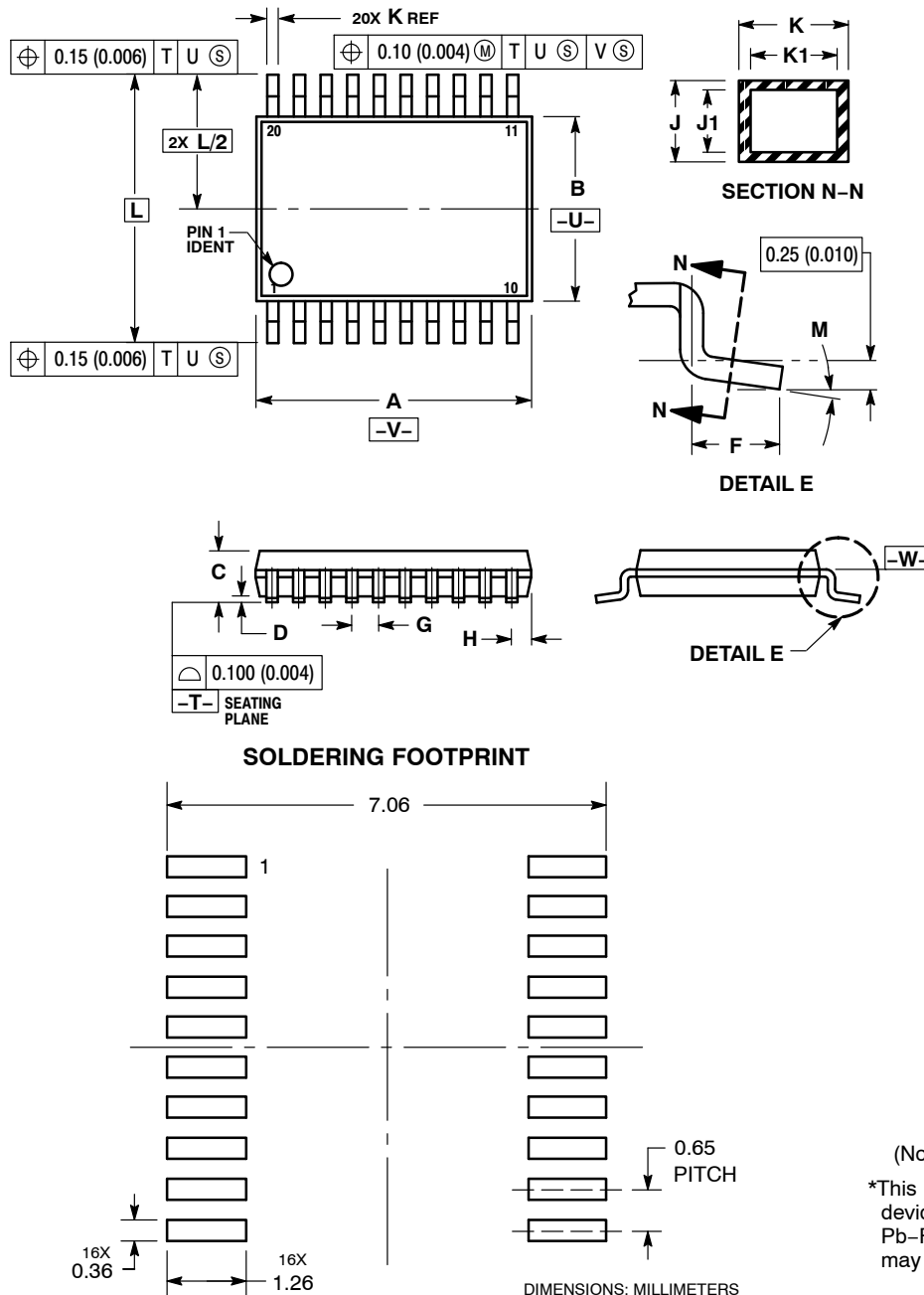
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SCALE 2:1

TSSOP-20 WB  
CASE 948E  
ISSUE D

DATE 17 FEB 2016

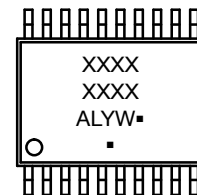


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

## GENERIC MARKING DIAGRAM\*



- A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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