

EMT2DXV6T5

Dual General Purpose Transistor

PNP Dual

This transistor is designed for general purpose amplifier applications. It is housed in the SOT-563 which is designed for low power surface mount applications.

- Lead-Free Solder Plating
- Low $V_{CE(SAT)}$, < 0.5 V

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--------------------------------|-----------|-------|------|
| Collector-Emitter Voltage | V_{CEO} | -60 | V |
| Collector-Base Voltage | V_{CBO} | -50 | V |
| Emitter-Base Voltage | V_{EBO} | -6.0 | V |
| Collector Current - Continuous | I_C | -100 | mAdc |

THERMAL CHARACTERISTICS

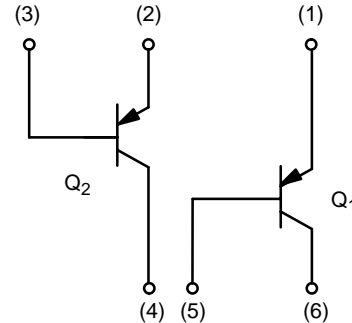
| Characteristic (One Junction Heated) | Symbol | Max | Unit |
|--|-----------------|------------------------------------|----------------------------|
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 357 (Note 1) 2.9 (Note 1) | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 350 (Note 1) | $^\circ\text{C}/\text{W}$ |
| Characteristic (Both Junctions Heated) | Symbol | Max | Unit |
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 500 (Note 1) 4.0 (Note 1) | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 250 (Note 1) | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |

1. FR-4 @ Minimum Pad.

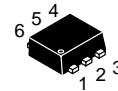


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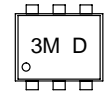
<http://onsemi.com>



MARKING DIAGRAM



SOT-563
CASE 463A
Style 2



3M = Specific Device Code
D = Date Code

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------|---------|--------------------------------|
| EMT2DXV6T5 | SOT-563 | 2 mm Pitch 8000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

EMT2DXV6T5

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---------------|------|-----|------|---------------|
| Collector–Base Breakdown Voltage ($I_C = -50 \mu\text{A}$, $I_E = 0$) | $V_{(BR)CBO}$ | -60 | - | - | Vdc |
| Collector–Emitter Breakdown Voltage ($I_C = -1.0 \text{mA}$, $I_B = 0$) | $V_{(BR)CEO}$ | -50 | - | - | Vdc |
| Emitter–Base Breakdown Voltage ($I_E = -50 \mu\text{A}$, $I_C = 0$) | $V_{(BR)EBO}$ | -6.0 | - | - | Vdc |
| Collector–Base Cutoff Current ($V_{CB} = -30 \text{Vdc}$, $I_E = 0$) | I_{CBO} | - | - | -0.5 | nA |
| Emitter–Base Cutoff Current ($V_{EB} = -5.0 \text{Vdc}$, $I_B = 0$) | I_{EBO} | - | - | -0.5 | μA |
| Collector–Emitter Saturation Voltage (Note 2) ($I_C = -50 \text{mA}$, $I_B = -5.0 \text{mA}$) | $V_{CE(sat)}$ | - | - | -0.5 | Vdc |
| DC Current Gain (Note 2) ($V_{CE} = -6.0 \text{Vdc}$, $I_C = -1.0 \text{mA}$) | h_{FE} | 120 | - | 560 | - |
| Transition Frequency ($V_{CE} = -12 \text{Vdc}$, $I_C = -2.0 \text{mA}$, $f = 30 \text{MHz}$) | f_T | - | 140 | - | MHz |
| Output Capacitance ($V_{CB} = -12 \text{Vdc}$, $I_E = 0 \text{A}$, $f = 1 \text{MHz}$) | C_{OB} | - | 3.5 | - | pF |

2. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, D.C. $\leq 2\%$.

EMT2DXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS

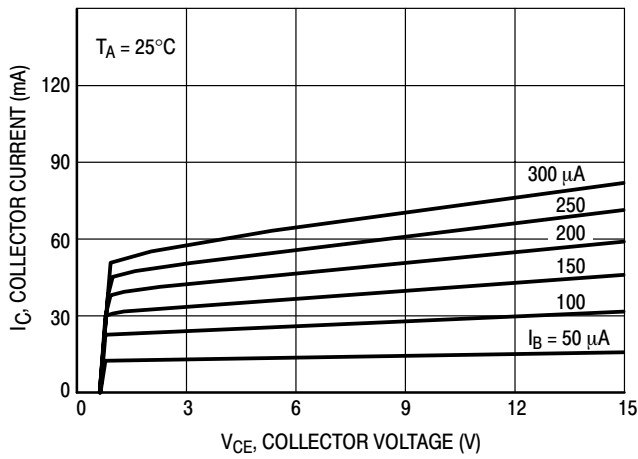


Figure 1. $I_C - V_{CE}$

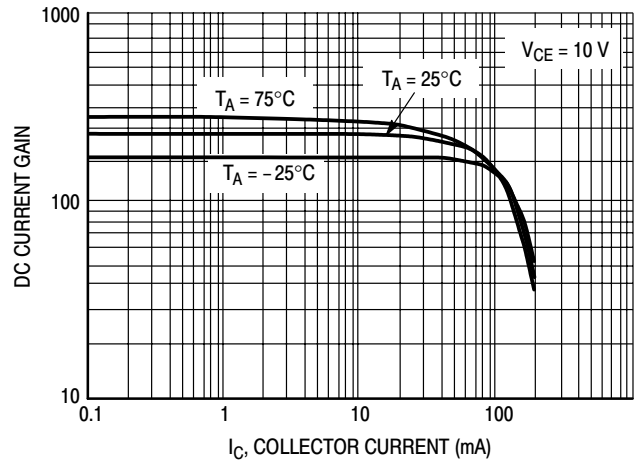


Figure 2. DC Current Gain

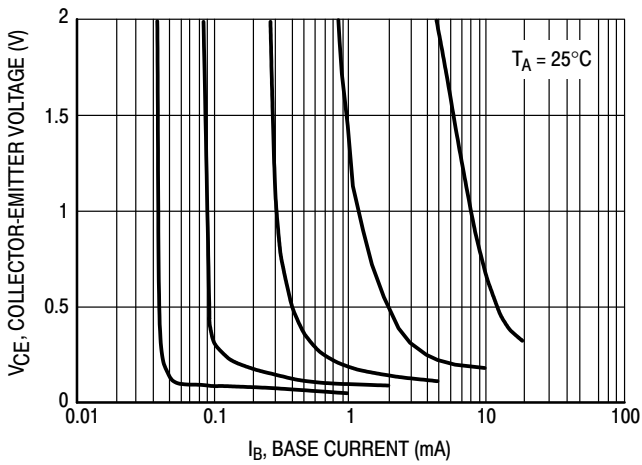


Figure 3. Collector Saturation Region

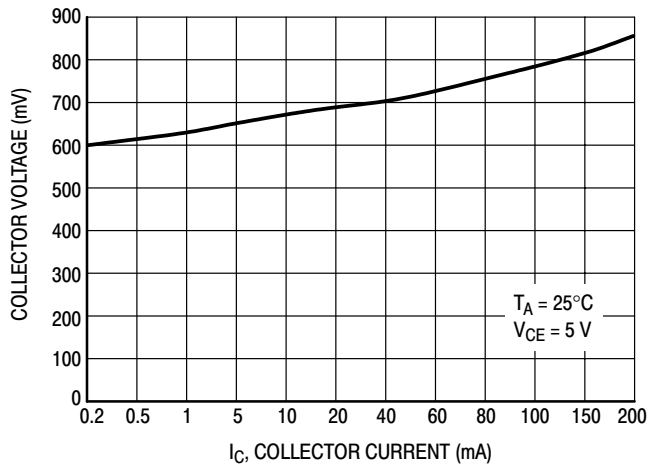


Figure 4. On Voltage

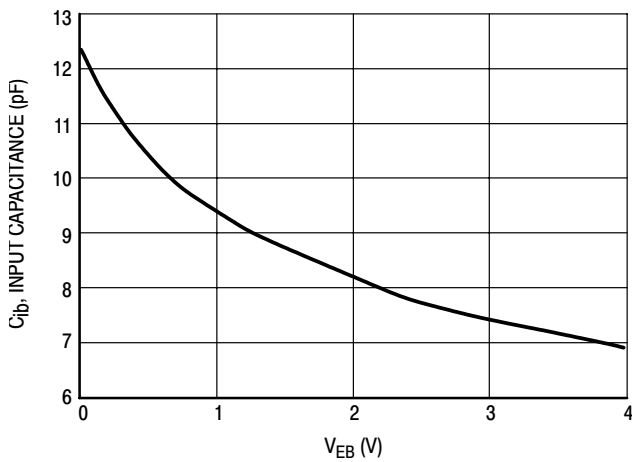


Figure 5. Capacitance

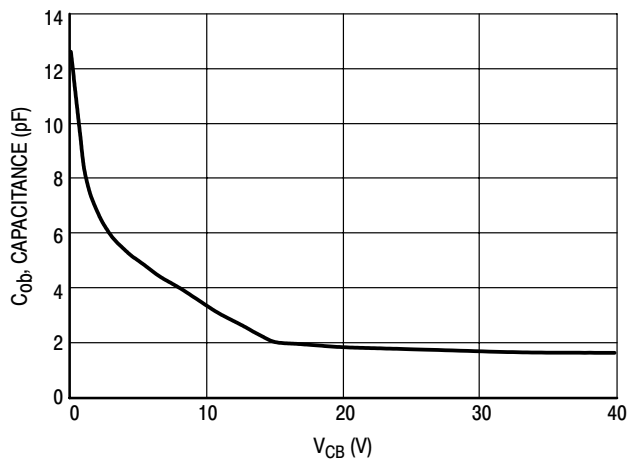


Figure 6. Capacitance

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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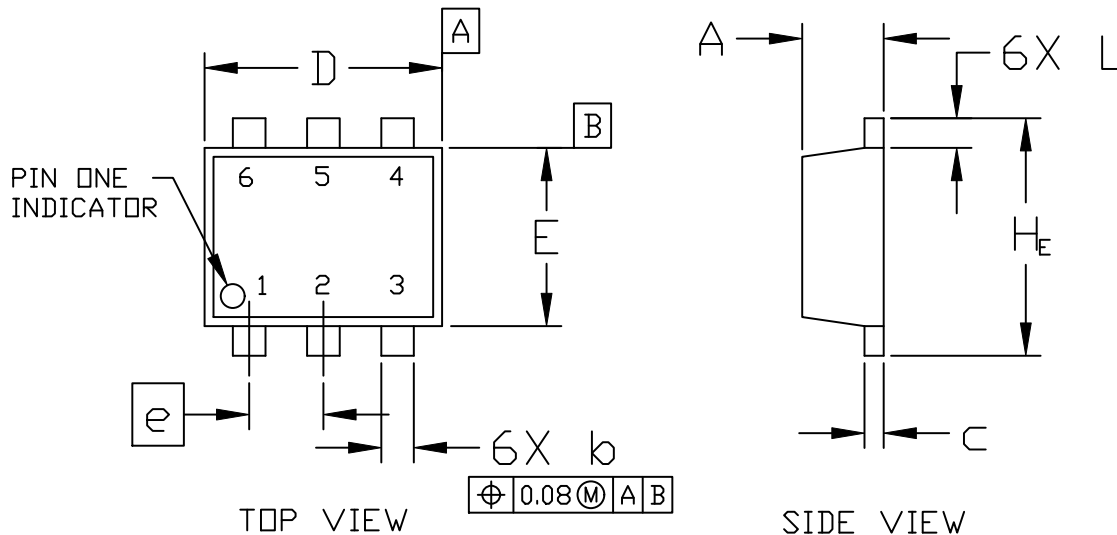
SCALE 4:1

SOT-563, 6 LEAD
CASE 463A
ISSUE H

DATE 26 JAN 2021

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



| DIM | MILLIMETERS | | |
|----------------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.08 | 0.13 | 0.18 |
| D | 1.50 | 1.60 | 1.70 |
| E | 1.10 | 1.20 | 1.30 |
| e | 0.50 BSC | | |
| L | 0.10 | 0.20 | 0.30 |
| H _E | 1.50 | 1.60 | 1.70 |

RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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SOT-563, 6 LEAD
CASE 463A
ISSUE H

DATE 26 JAN 2021

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

**GENERIC
MARKING DIAGRAM***



XX = Specific Device Code
M = Month Code
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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