

# MC74HC589A

## 8-Bit Serial or Parallel-Input/Serial-Output Shift Register with 3-State Output

### High-Performance Silicon-Gate CMOS

The MC74HC589A device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see the Function Table). The shift register output,  $Q_H$ , is a 3-state output, allowing this device to be used in bus-oriented systems.

The HC589A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

#### Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 526 FETs or 131.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

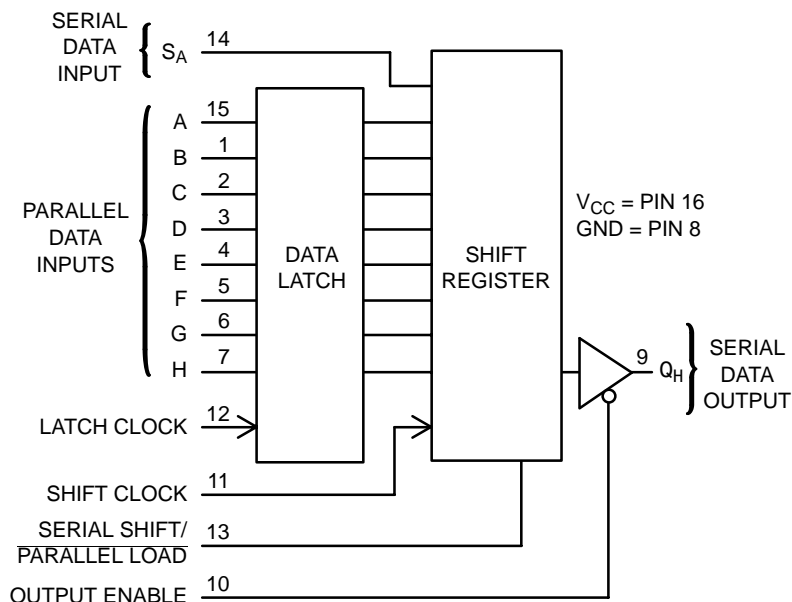
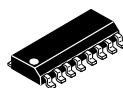


Figure 1. Logic Diagram

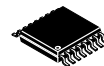


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SOIC-16  
D SUFFIX  
CASE 751B

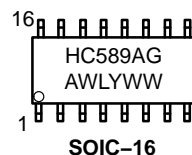


TSSOP-16  
DT SUFFIX  
CASE 948F

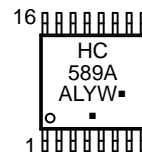
#### PIN ASSIGNMENT

B	1	16	V <sub>CC</sub>
C	2	15	A
D	3	14	S <sub>A</sub>
E	4	13	SERIAL SHIFT/ PARALLEL LOAD
F	5	12	LATCH CLOCK
G	6	11	SHIFT CLOCK
H	7	10	OUTPUT ENABLE
GND	8	9	Q <sub>H</sub>

#### MARKING DIAGRAMS



SOIC-16



TSSOP-16

A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

# MC74HC589A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	$-0.5 \leq V_{CC} + 0.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	$-0.5 \leq V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 35$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 75$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
$T_J$	Junction Temperature Under Bias	+150	°C
$\theta_{JA}$	Thermal Resistance	PDIP SOIC TSSOP 78 112 148	°C/W
$P_D$	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP 750 500 450	mW
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating	Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3) > 4000 > 200 > 1000	V
$I_{Latchup}$	Latchup Performance	Above $V_{CC}$ and Below GND at 85°C (Note 4) $\pm 300$	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 2)	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 3.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$ 0 0 0 0	1000 800 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55°C to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA	3.0	2.48	2.34	2.20	
		I <sub>out</sub>   ≤ 6.0 mA	4.5	3.98	3.84	3.70	
		I <sub>out</sub>   ≤ 7.8 mA	6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA	3.0	0.26	0.33	0.40	
		I <sub>out</sub>   ≤ 6.0 mA	4.5	0.26	0.33	0.40	
		I <sub>out</sub>   ≤ 7.8 mA	6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

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## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 3 and 9)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Clock to Q <sub>H</sub> (Figures 2 and 9)	2.0 3.0 4.5 6.0	175 100 40 30	225 110 50 40	275 125 60 50	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Shift Clock to Q <sub>H</sub> (Figures 3 and 9)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Serial Shift/Parallel Load to Q <sub>H</sub> (Figures 5 and 9)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q <sub>H</sub> (Figures 4 and 10)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Q <sub>H</sub> (Figures 4 and 10)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 9)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns
C <sub>in</sub>	Maximum Input Capacitance	–	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	–	15	15	15	pF

C <sub>PD</sub>	Power Dissipation Capacitance (per Package)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		50	

\*Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

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## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, A–H to Latch Clock (Figure 6)	2.0	100	125	150	ns
		3.0	40	50	60	
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>su</sub>	Minimum Setup Time, Serial Data Input S <sub>A</sub> to Shift Clock (Figure 7)	2.0	100	125	150	ns
		3.0	40	50	60	
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>su</sub>	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 8)	2.0	100	125	150	ns
		3.0	40	50	60	
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Latch Clock to A–H (Figure 6)	2.0	25	30	40	ns
		3.0	10	12	15	
		4.5	5	6	8	
		6.0	5	6	7	
t <sub>h</sub>	Minimum Hold Time, Shift Clock to Serial Data Input S <sub>A</sub> (Figure 7)	2.0	5	5	5	ns
		3.0	5	5	5	
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>w</sub>	Minimum Pulse Width, Shift Clock (Figure 3)	2.0	75	95	110	ns
		3.0	40	50	60	
		4.5	15	19	23	
		6.0	13	16	19	
t <sub>w</sub>	Minimum Pulse Width, Latch Clock (Figure 2)	2.0	80	100	120	ns
		3.0	40	50	60	
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 5)	2.0	80	100	120	ns
		3.0	40	50	60	
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 2)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

## FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Output Enable	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input $S_A$	Parallel Inputs A–H	Data Latch Contents	Shift Register Contents	Output $Q_H$
Force Output into High Impedance State	H	X	X	X	X	X	X	X	Z
Load Parallel Data into Data Latch	L	H	$\nearrow$	L, H, $\nearrow$	X	a–h	a–h	U	U
Transfer Latch Contents to Shift Register	L	L	L, H, $\nearrow$	X	X	X	U	$LR_N \rightarrow SR_N$	$LR_H$
Contents of Input Latch and Shift Register are Unchanged	L	H	L, H, $\nearrow$	L, H, $\nearrow$	X	X	U	U	U
Load Parallel Data into Data Latch and Shift Register	L	L	$\nearrow$	X	X	a–h	a–h	a–h	h
Shift Serial Data into Shift Register	L	H	X	$\nearrow$	D	X	*	$SR_A = D, SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$
Load Parallel Data in Data Latch and Shift Serial Data into Shift Register	L	H	$\nearrow$	$\nearrow$	D	a–h	a–h	$SR_A = D, SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$

LR = latch register contents

SR = shift register contents

a–h = data at parallel data inputs A–H

D = data (L, H) at serial data input  $S_A$ 

U = remains unchanged

X = don't care

Z = high impedance

\* = depends on Latch Clock input

## SWITCHING WAVEFORMS

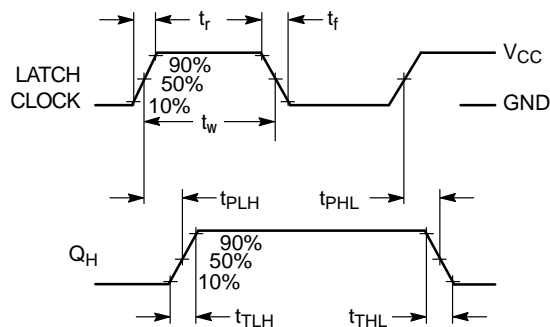


Figure 2. (Serial Shift/Parallel Load = L)

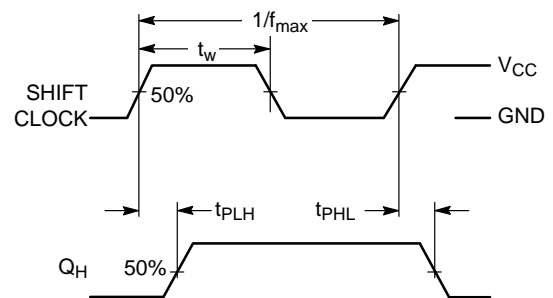


Figure 3. (Serial Shift/Parallel Load = H)

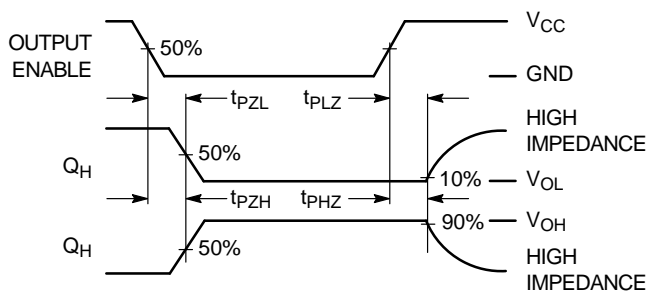


Figure 4.

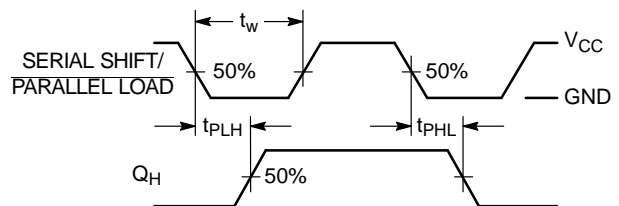


Figure 5.

## SWITCHING WAVEFORMS

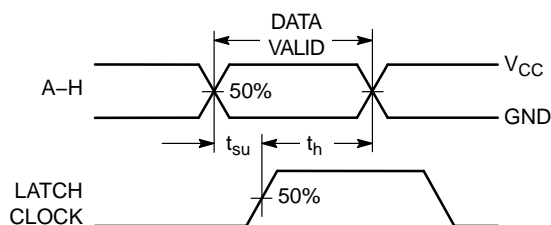


Figure 6.

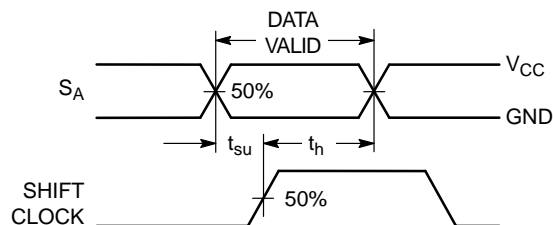


Figure 7.

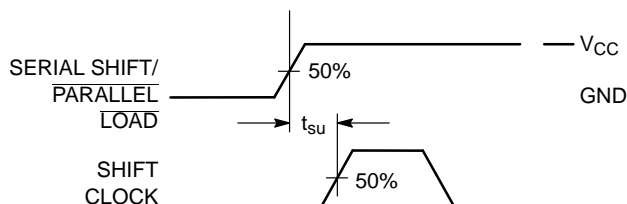
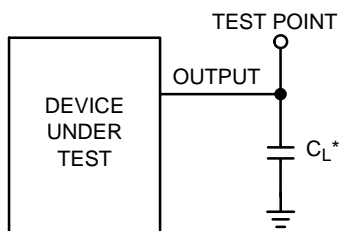
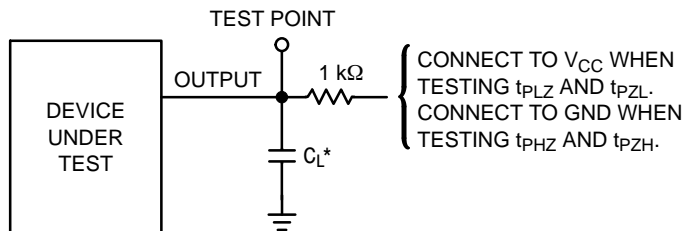


Figure 8.



\*Includes all probe and jig capacitance.

Figure 9. Test Circuit



\*Includes all probe and jig capacitance.

Figure 10. Test Circuit

## PIN DESCRIPTIONS

## Data Inputs

**A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)**

Parallel data inputs. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.

**S<sub>A</sub> (Pin 14)**

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

## Control Inputs

**Serial Shift/Parallel Load (Pin 13)**

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.

**Shift Clock (Pin 11)**

Serial shift clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and

data in stage H is shifted out Q<sub>H</sub>, being replaced by the data previously stored in stage G.

**Latch Clock (Pin 12)**

Data latch clock. A low-to-high transition on this input loads the parallel data on inputs A–H into the data latch.

**Output Enable (Pin 10)**

Active-low output enable A high level applied to this pin forces the Q<sub>H</sub> output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.

## Output

**Q<sub>H</sub> (Pin 9)**

Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.

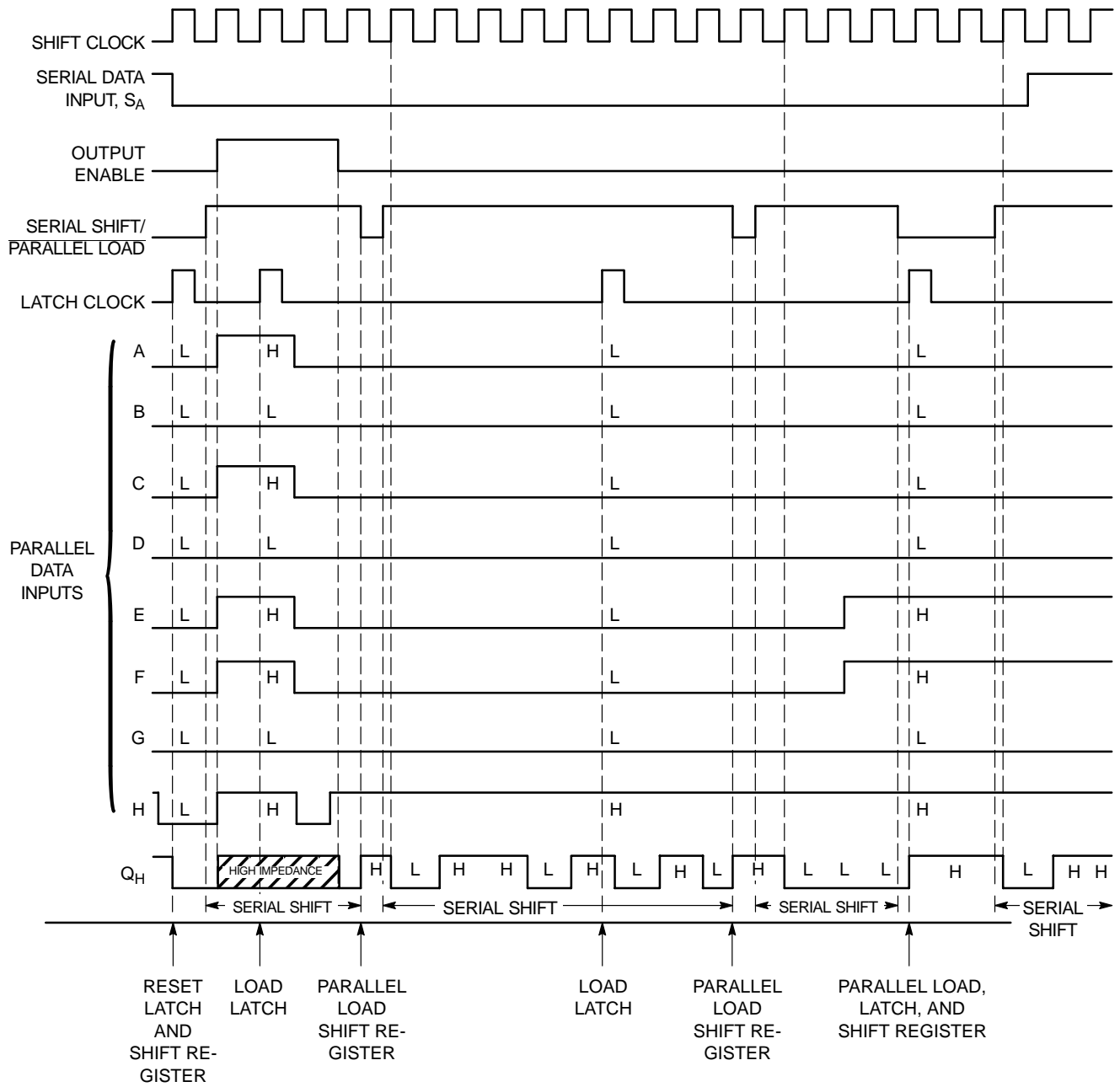
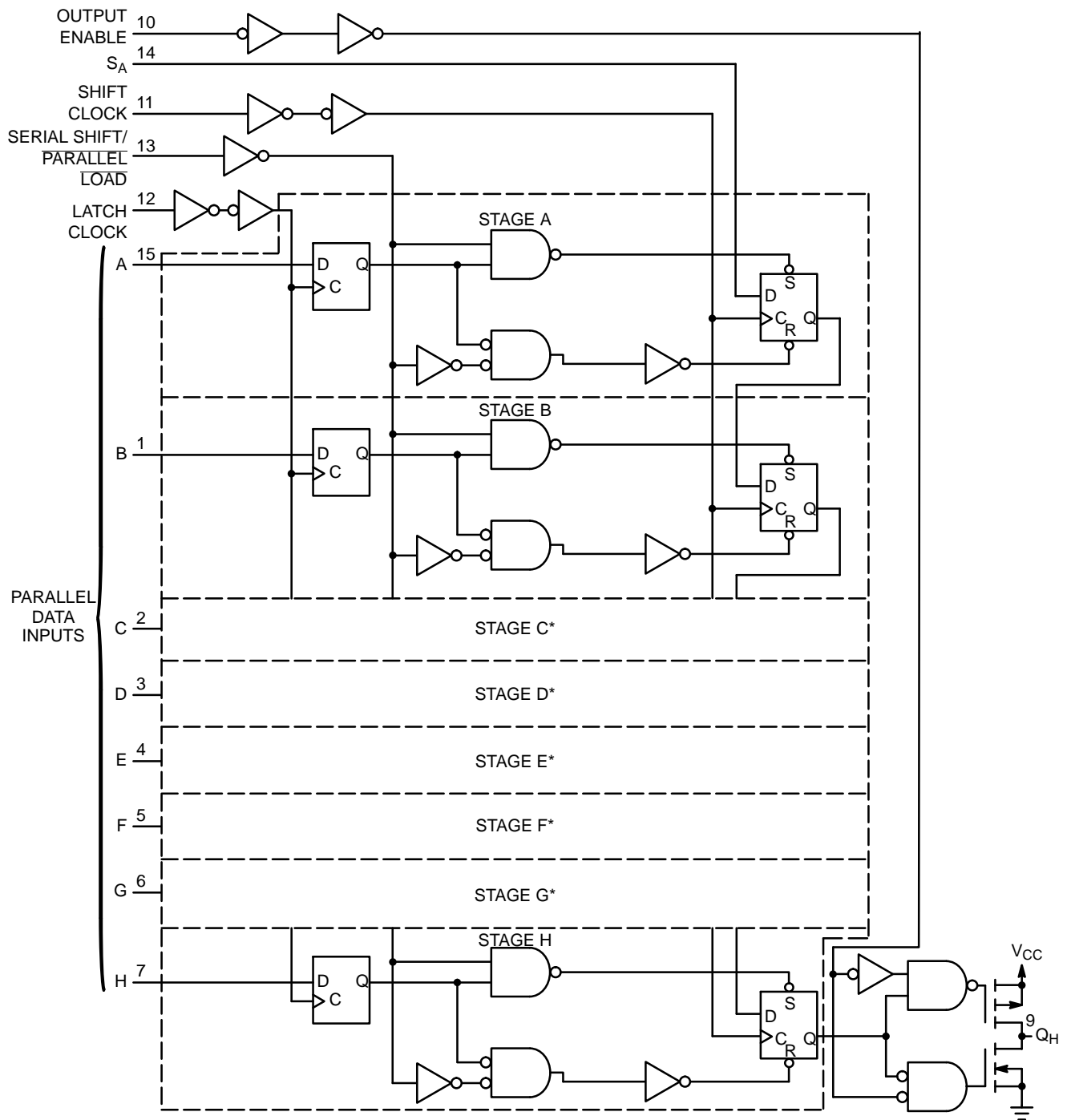


Figure 11. Timing Diagram



# MC74HC589A



\*Stages C thru G (not shown in detail) are identical to stages A and B above.

**Figure 12. Logic Detail**

## MC74HC589A

### ORDERING INFORMATION

Device	Package	Shipping†
MC74HC589ADG	SOIC-16 (Pb-Free)	48 Units / Rail
NLV74HC589ADG*	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC589ADR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
NLV74HC589ADR2G*	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74HC589ADTR2G	TSSOP-16 (Pb-Free)	2500 Tape & Reel
NLV74HC589ADTR2G*	TSSOP-16 (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

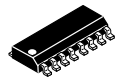
\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

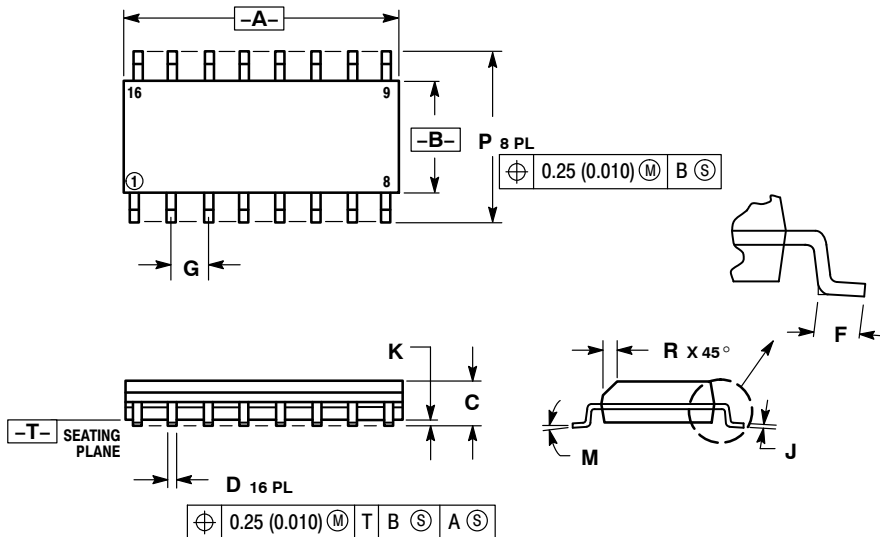
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SCALE 1:1

### SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



#### NOTES:

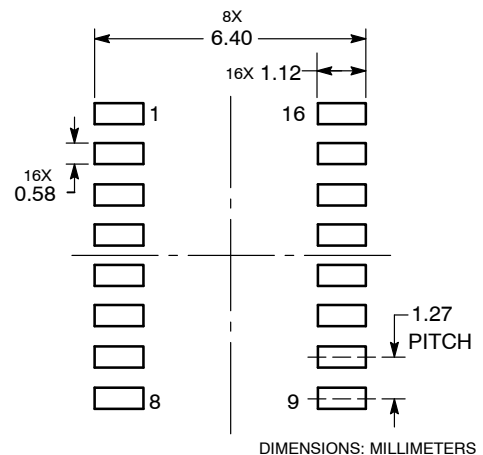
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
E	0.40	1.25	0.016	0.049
F	1.27 BSC		0.050 BSC	
G	0.19	0.25	0.008	0.009
H	0.10	0.25	0.004	0.009
I	0°	7°	0°	7°
J	5.80	6.20	0.229	0.244
K	0.25	0.50	0.010	0.019

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1. COLLECTOR	PIN 1. CATHODE	PIN 1. COLLECTOR, DYE #1	PIN 1. COLLECTOR, DYE #1
2. BASE	2. ANODE	2. BASE, #1	2. COLLECTOR, #1
3. EMITTER	3. NO CONNECTION	3. EMITTER, #1	3. COLLECTOR, #2
4. NO CONNECTION	4. CATHODE	4. COLLECTOR, #1	4. COLLECTOR, #2
5. EMITTER	5. CATHODE	5. COLLECTOR, #2	5. COLLECTOR, #3
6. BASE	6. NO CONNECTION	6. BASE, #2	6. COLLECTOR, #3
7. COLLECTOR	7. ANODE	7. EMITTER, #2	7. COLLECTOR, #4
8. COLLECTOR	8. CATHODE	8. COLLECTOR, #2	8. COLLECTOR, #4
9. BASE	9. CATHODE	9. COLLECTOR, #3	9. BASE, #4
10. EMITTER	10. ANODE	10. BASE, #3	10. EMITTER, #4
11. NO CONNECTION	11. NO CONNECTION	11. EMITTER, #3	11. BASE, #3
12. EMITTER	12. CATHODE	12. COLLECTOR, #3	12. EMITTER, #3
13. BASE	13. CATHODE	13. COLLECTOR, #4	13. BASE, #2
14. COLLECTOR	14. NO CONNECTION	14. BASE, #4	14. EMITTER, #2
15. EMITTER	15. ANODE	15. EMITTER, #4	15. BASE, #1
16. COLLECTOR	16. CATHODE	16. COLLECTOR, #4	16. EMITTER, #1

STYLE 5:	STYLE 6:	STYLE 7:
PIN 1. DRAIN, DYE #1	PIN 1. CATHODE	PIN 1. SOURCE N-CH
2. DRAIN, #1	2. CATHODE	2. COMMON DRAIN (OUTPUT)
3. DRAIN, #2	3. CATHODE	3. COMMON DRAIN (OUTPUT)
4. DRAIN, #2	4. CATHODE	4. GATE P-CH
5. DRAIN, #3	5. CATHODE	5. COMMON DRAIN (OUTPUT)
6. DRAIN, #3	6. CATHODE	6. COMMON DRAIN (OUTPUT)
7. DRAIN, #4	7. CATHODE	7. COMMON DRAIN (OUTPUT)
8. DRAIN, #4	8. CATHODE	8. SOURCE P-CH
9. GATE, #4	9. ANODE	9. SOURCE P-CH
10. SOURCE, #4	10. ANODE	10. COMMON DRAIN (OUTPUT)
11. GATE, #3	11. ANODE	11. COMMON DRAIN (OUTPUT)
12. SOURCE, #3	12. ANODE	12. COMMON DRAIN (OUTPUT)
13. GATE, #2	13. ANODE	13. GATE N-CH
14. SOURCE, #2	14. ANODE	14. COMMON DRAIN (OUTPUT)
15. GATE, #1	15. ANODE	15. COMMON DRAIN (OUTPUT)
16. SOURCE, #1	16. ANODE	16. SOURCE N-CH

#### SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

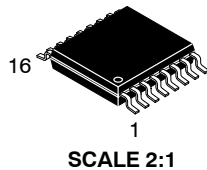
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DESCRIPTION:	SOIC-16	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

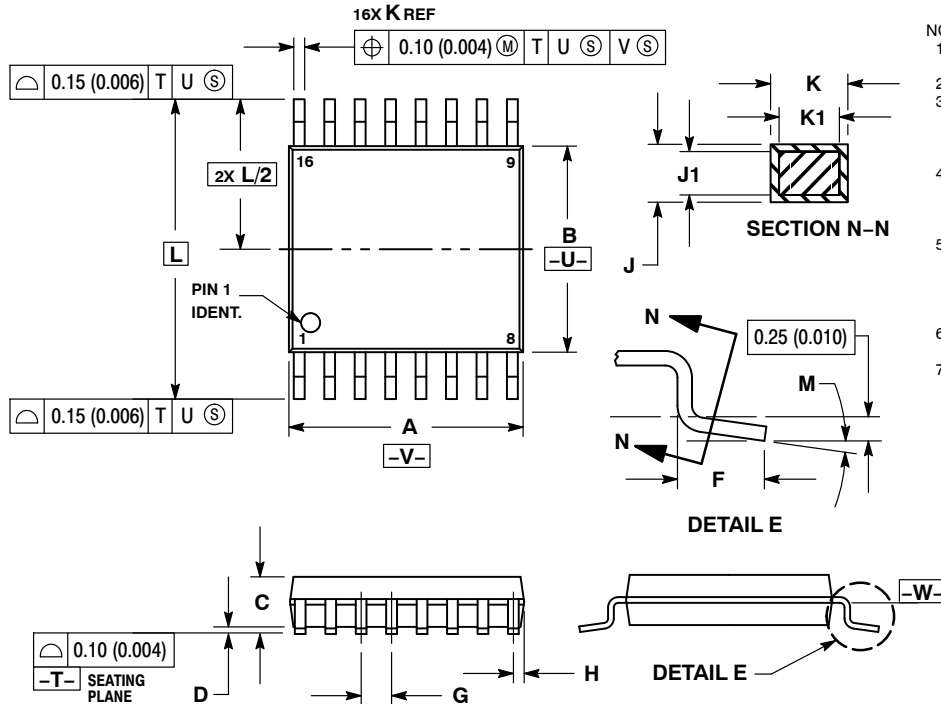
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**TSSOP-16**  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006

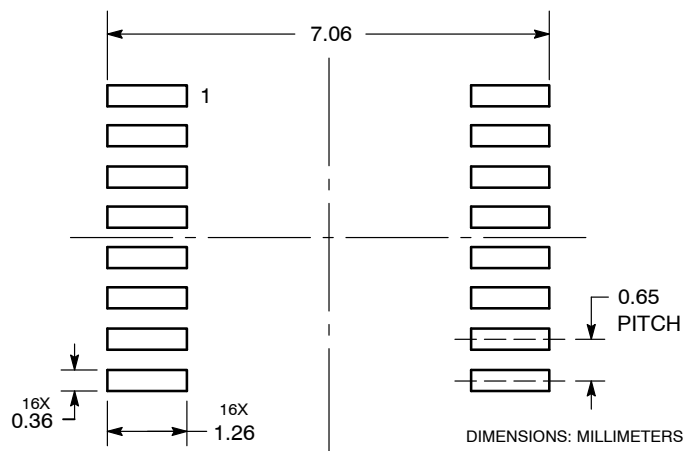


## NOTES:

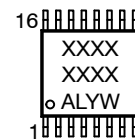
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

## SOLDERING FOOTPRINT



## GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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