

NDF04N60Z, NDD04N60Z

Power MOSFET, N-Channel, 600 V, 2.0 Ω

Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode-Protected Gate
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

| Parameter | Symbol | NDF | NDD | Unit |
|---|-----------------------------------|------------|-----|------|
| Drain-to-Source Voltage | V _{DSS} | 600 | | V |
| Continuous Drain Current R _{θJC} (Note 1) | I _D | 4.8 | 4.1 | A |
| Continuous Drain Current R _{θJC} , T _A = 100°C (Note 1) | I _D | 3.0 | 2.6 | A |
| Pulsed Drain Current, V _{GS} @ 10V | I _{DM} | 20 | 20 | A |
| Power Dissipation R _{θJC} | P _D | 30 | 83 | W |
| Gate-to-Source Voltage | V _{GS} | ±30 | | V |
| Single Pulse Avalanche Energy, I _D = 4.0 A | E _{AS} | 120 | | mJ |
| ESD (HBM) (JESD22-A114) | V _{esd} | 3000 | | V |
| RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T _A = 25°C) (Figure 15) | V _{ISO} | 4500 | - | V |
| Peak Diode Recovery (Note 2) | dV/dt | 4.5 | | V/ns |
| MOSFET dV/dt | dV/dt | 60 | | V/ns |
| Continuous Source Current (Body Diode) | I _S | 4.0 | | A |
| Maximum Temperature for Soldering Leads | T _L | 260 | | °C |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | -55 to 150 | | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

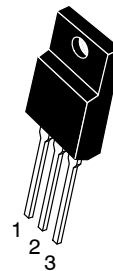
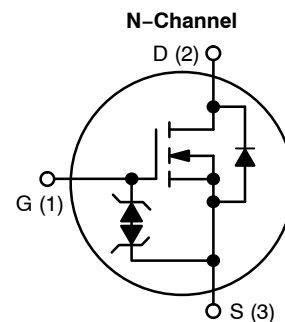
1. Limited by maximum junction temperature
2. I_{SD} = 4.0 A, di/dt ≤ 100 A/μs, V_{DD} ≤ BV_{DSS}, T_J = +150°C



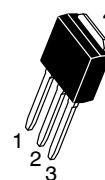
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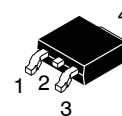
| V _{DSS} (@ T _{Jmax}) | R _{DS(on)} (MAX) @ 2 A |
|---|---------------------------------|
| 650 V | 2.0 Ω |



NDF04N60ZG,
NDD04N60ZH
TO-220FP
CASE 221AH



NDD04N60Z-1G
IPAK
CASE 369D



NDD04N60ZT4G
DPAK
CASE 369AA

ORDERING AND MARKING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

NDF04N60Z, NDD04N60Z

THERMAL RESISTANCE

| Parameter | Symbol | Value | Unit |
|----------------------------------|------------------|----------------------|------|
| Junction-to-Case (Drain) | R _{θJC} | NDF04N60Z | 4.2 |
| | | NDD04N60Z | 1.5 |
| Junction-to-Ambient Steady State | R _{θJA} | (Note 3) NDF04N60Z | 50 |
| | | (Note 4) NDD04N60Z | 38 |
| | | (Note 3) NDD04N60Z-1 | 80 |

3. Insertion mounted

4. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127 in sq [2 oz] including traces).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|----------------|-----------------|--------|-----|-----|-----|------|
|----------------|-----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|--|--|---|-------|-----|-----|------|
| Drain-to-Source Breakdown Voltage | V _{GS} = 0 V, I _D = 1 mA | BV _{DSS} | 600 | | | V |
| Breakdown Voltage Temperature Co-efficient | Reference to 25°C, I _D = 1 mA | ΔBV _{DSS} / ΔT _J | | 0.6 | | V/°C |
| Drain-to-Source Leakage Current | V _{DS} = 600 V, V _{GS} = 0 V | I _{DSS} | 25°C | | 1 | μA |
| | | | 150°C | | 50 | |
| Gate-to-Source Forward Leakage | V _{GS} = ±20 V | I _{GSS} | | | ±10 | μA |

ON CHARACTERISTICS (Note 5)

| | | | | | | |
|--------------------------------------|--|---------------------|-----|-----|-----|---|
| Static Drain-to-Source On-Resistance | V _{GS} = 10 V, I _D = 2.0 A | R _{DS(on)} | | 1.8 | 2.0 | Ω |
| Gate Threshold Voltage | V _{DS} = V _{GS} , I _D = 50 μA | V _{GS(th)} | 3.0 | 3.9 | 4.5 | V |
| Forward Transconductance | V _{DS} = 15 V, I _D = 2.0 A | g _{FS} | | 3.3 | | S |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|---------------------------------------|--|------------------|-----|-----|-----|----|
| Input Capacitance (Note 6) | V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz | C _{iss} | 427 | 535 | 640 | pF |
| Output Capacitance (Note 6) | | C _{oss} | 50 | 62 | 75 | |
| Reverse Transfer Capacitance (Note 6) | | C _{rss} | 8 | 14 | 20 | |
| Total Gate Charge (Note 6) | V _{DD} = 300 V, I _D = 4.0 A, V _{GS} = 10 V | Q _g | 10 | 19 | 29 | nC |
| Gate-to-Source Charge (Note 6) | | Q _{gs} | 2 | 3.9 | 6 | |
| Gate-to-Drain ("Miller") Charge | | Q _{gd} | 5 | 10 | 15 | nC |
| Plateau Voltage | | V _{GP} | | 6.5 | | V |
| Gate Resistance | | R _g | | 4.7 | | Ω |

RESISTIVE SWITCHING CHARACTERISTICS

| | | | | | | |
|---------------------|--|---------------------|--|-----|--|----|
| Turn-On Delay Time | V _{DD} = 300 V, I _D = 4.0 A, V _{GS} = 10 V, R _G = 5 Ω | t _{d(on)} | | 13 | | ns |
| Rise Time | | t _r | | 9.0 | | |
| Turn-Off Delay Time | | t _{d(off)} | | 24 | | |
| Fall Time | | t _f | | 15 | | |

SOURCE-DRAIN DIODE CHARACTERISTICS (T_C = 25°C unless otherwise noted)

| | | | | | | |
|-------------------------|---|-----------------|--|-----|-----|----|
| Diode Forward Voltage | I _S = 4.0 A, V _{GS} = 0 V | V _{SD} | | | 1.6 | V |
| Reverse Recovery Time | V _{GS} = 0 V, V _{DD} = 30 V I _S = 4.0 A, di/dt = 100 A/μs | t _{rr} | | 285 | | ns |
| Reverse Recovery Charge | | Q _{rr} | | 1.3 | | μC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

6. Guaranteed by design.

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TYPICAL CHARACTERISTICS

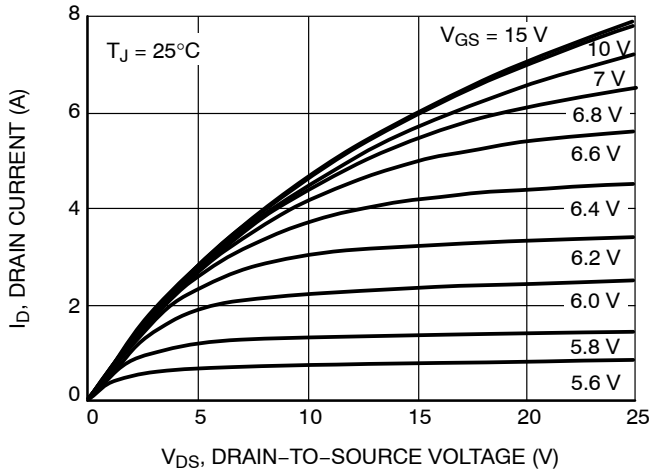


Figure 1. On-Region Characteristics

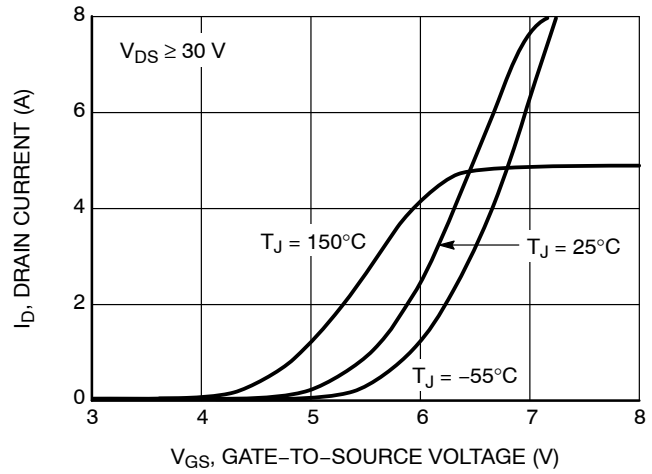


Figure 2. Transfer Characteristics

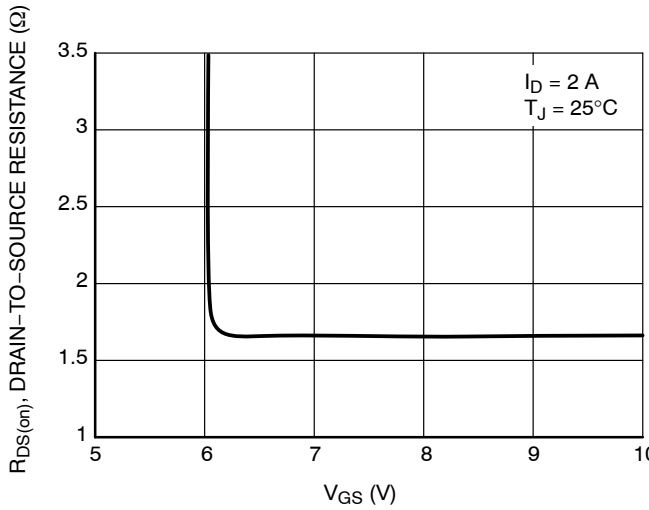


Figure 3. On-Resistance vs. Gate Voltage

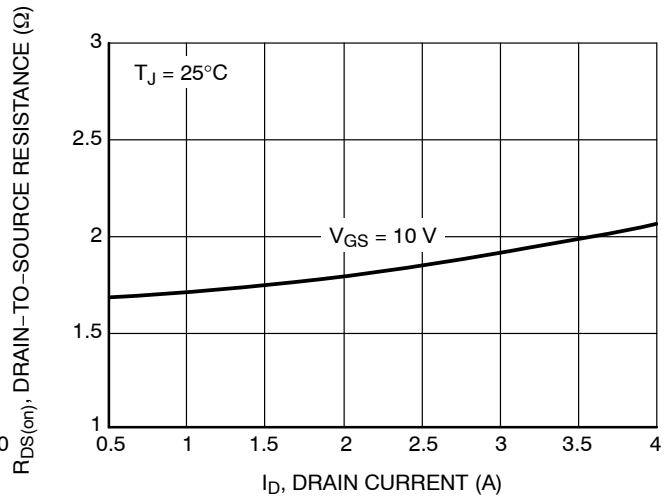


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

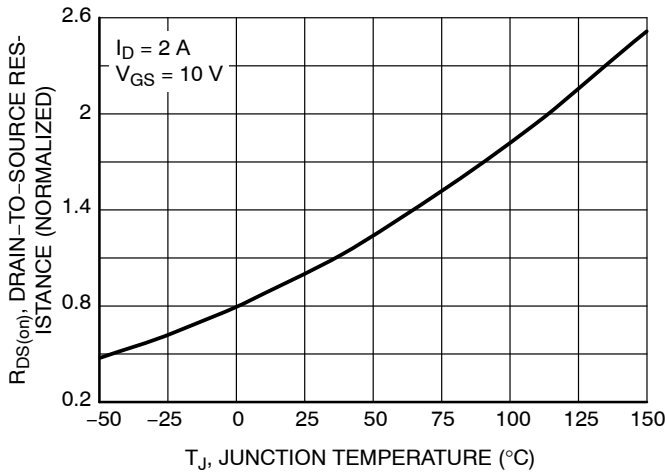


Figure 5. On-Resistance Variation with Temperature

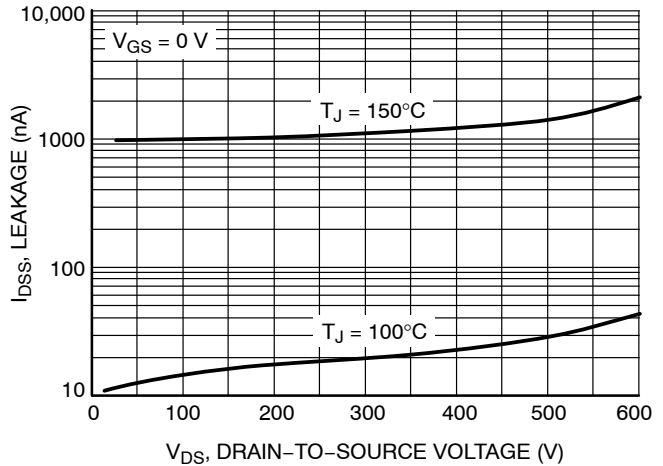


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NDF04N60Z, NDD04N60Z

TYPICAL CHARACTERISTICS

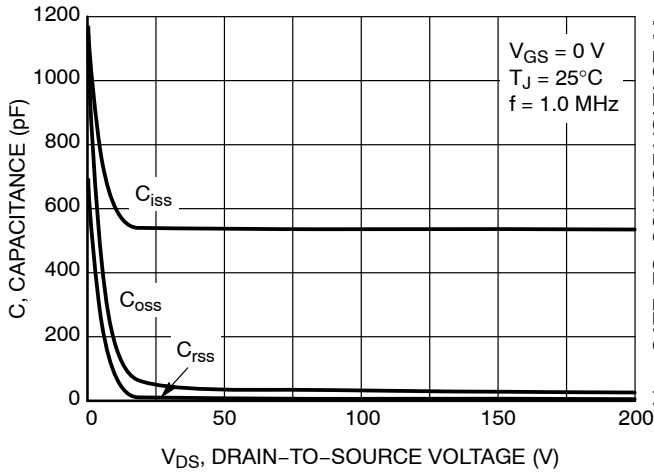


Figure 7. Capacitance Variation

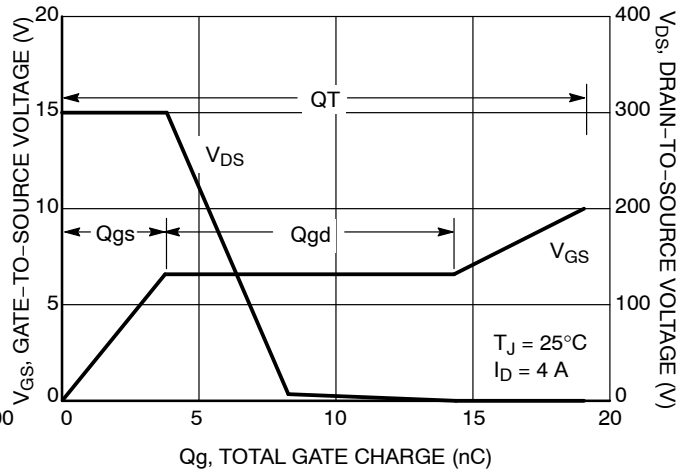


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

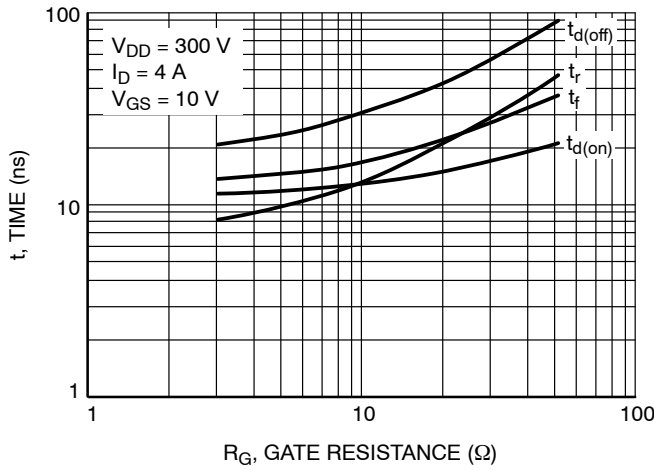


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

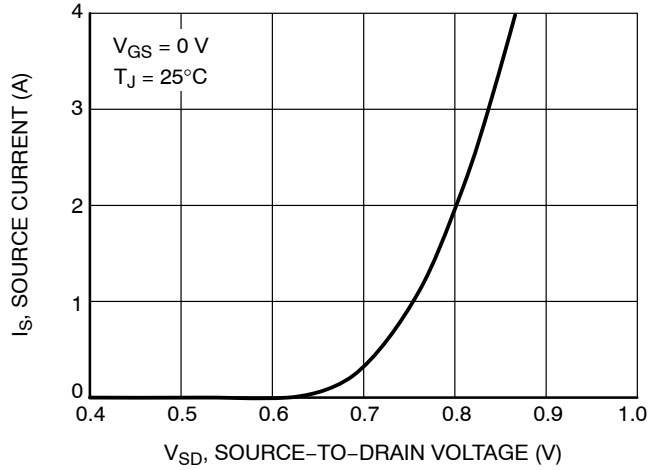


Figure 10. Diode Forward Voltage vs. Current

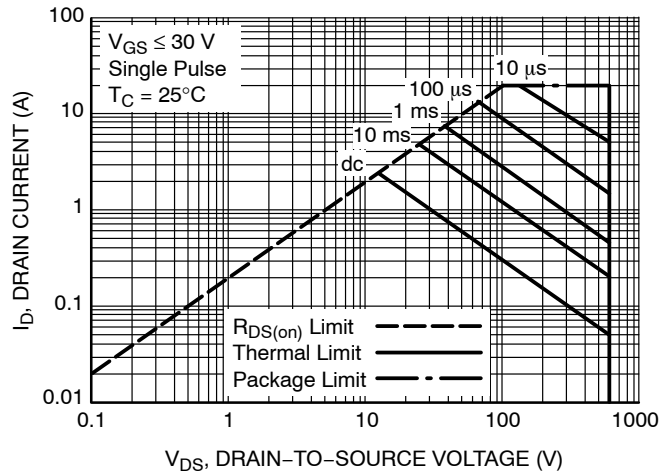


Figure 11. Maximum Rated Forward Biased Safe Operating Area for NDF04N60Z

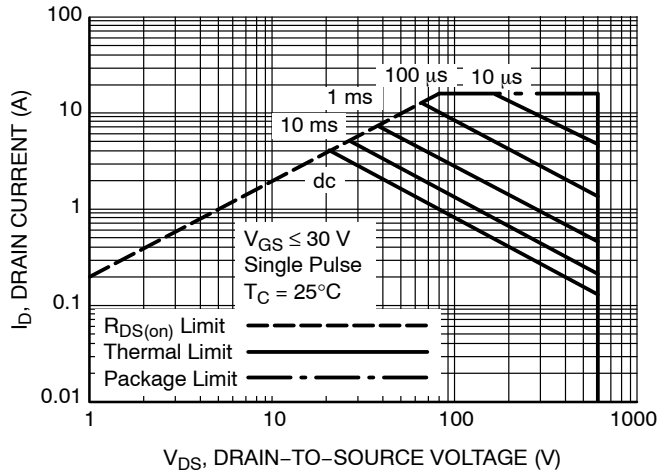


Figure 12. Maximum Rated Forward Biased Safe Operating Area for NDD04N60Z

NDF04N60Z, NDD04N60Z

TYPICAL CHARACTERISTICS

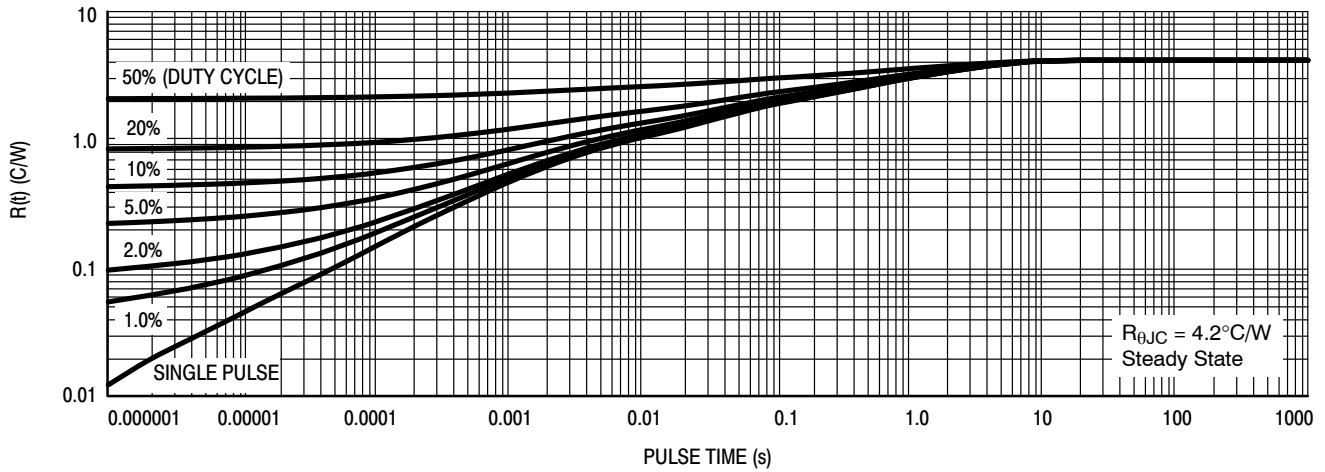


Figure 13. Thermal Impedance for NDF04N60Z

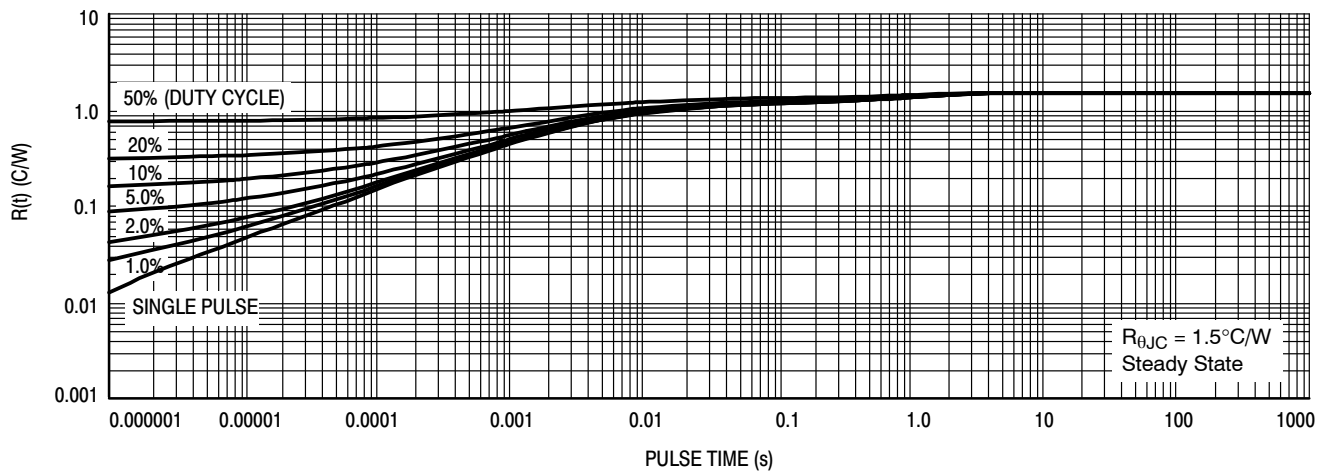


Figure 14. Thermal Impedance for NDD04N60Z

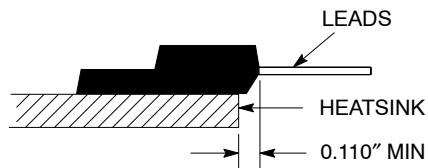


Figure 15. Mounting Position for Isolation Test

Measurement made between leads and heatsink with all leads shorted together.

*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

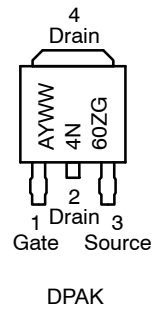
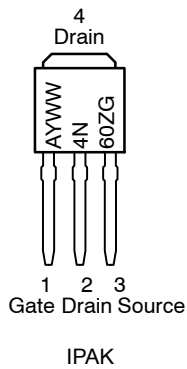
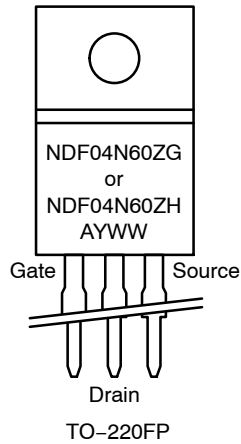
NDF04N60Z, NDD04N60Z

ORDERING INFORMATION

| Order Number | Package | Shipping† |
|--------------|-------------------------------------|----------------------|
| NDF04N60ZG | TO-220FP (Pb-Free, Halogen-Free) | 50 Units / Rail |
| NDF04N60ZH | TO-220FP (Pb-Free, Halogen-Free) | 50 Units / Rail |
| NDD04N60Z-1G | IPAK (Pb-Free, Halogen-Free) | 75 Units / Rail |
| NDD04N60ZT4G | DPAK (Pb-Free, Halogen-Free) | 2500 / Tape and Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS



A = Location Code*
 Y = Year
 WW = Work Week
 G, H = Pb-Free, Halogen-Free Package

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejecter pin), the front side assembly code may be blank.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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TO-220 FULLPACK, 3-LEAD CASE 221AH ISSUE F

DATE 30 SEP 2014



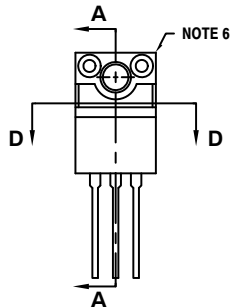
SCALE 1:1



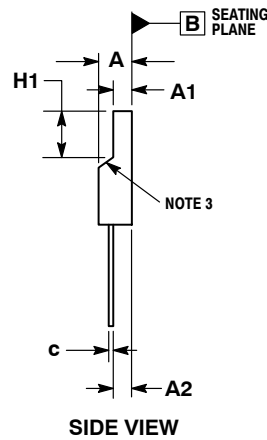
FRONT VIEW



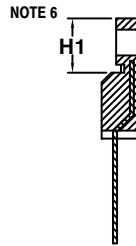
SECTION D-D



ALTERNATE CONSTRUCTION



SIDE VIEW



SECTION A-A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR UNCONTROLLED IN THIS AREA.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.
6. CONTOURS AND FEATURES OF THE MOLDED PACKAGE BODY MAY VARY WITHIN THE ENVELOPE DEFINED BY DIMENSIONS A1 AND H1 FOR MANUFACTURING PURPOSES.

| MILLIMETERS | | |
|-------------|----------|-------|
| DIM | MIN | MAX |
| A | 4.30 | 4.70 |
| A1 | 2.50 | 2.90 |
| A2 | 2.50 | 2.90 |
| b | 0.54 | 0.84 |
| b2 | 1.10 | 1.40 |
| c | 0.49 | 0.79 |
| D | 14.70 | 15.30 |
| E | 9.70 | 10.30 |
| e | 2.54 BSC | |
| H1 | 6.60 | 7.10 |
| L | 12.50 | 14.73 |
| L1 | --- | 2.80 |
| P | 3.00 | 3.40 |
| Q | 2.80 | 3.20 |

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:

1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE

STYLE 2:

1. CATHODE
2. ANODE
3. GATE

| | | |
|------------------|-------------------------|--|
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| DESCRIPTION: | TO-220 FULLPACK, 3-LEAD | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

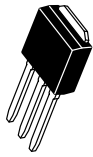
PACKAGE DIMENSIONS

ON Semiconductor®

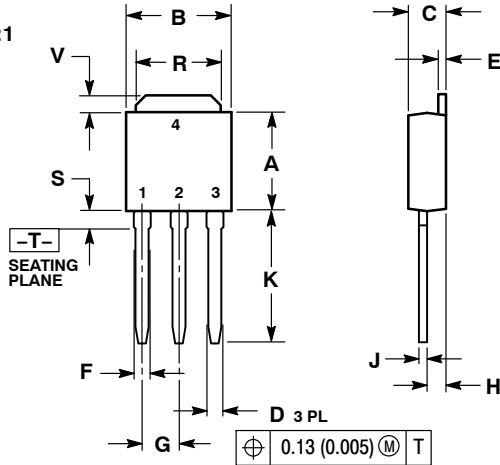


IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010



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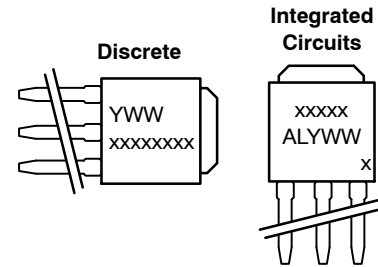


- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 | BSC | 2.29 | BSC |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

- | | | | |
|--|---|--|--|
| <p>STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR</p> | <p>STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN</p> | <p>STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE</p> | <p>STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE</p> |
| <p>STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE</p> | <p>STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2</p> | <p>STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR</p> | |

MARKING DIAGRAMS



- xxxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

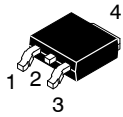
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| DOCUMENT NUMBER: | 98AON10528D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | IPAK (DPAK INSERTION MOUNT) | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



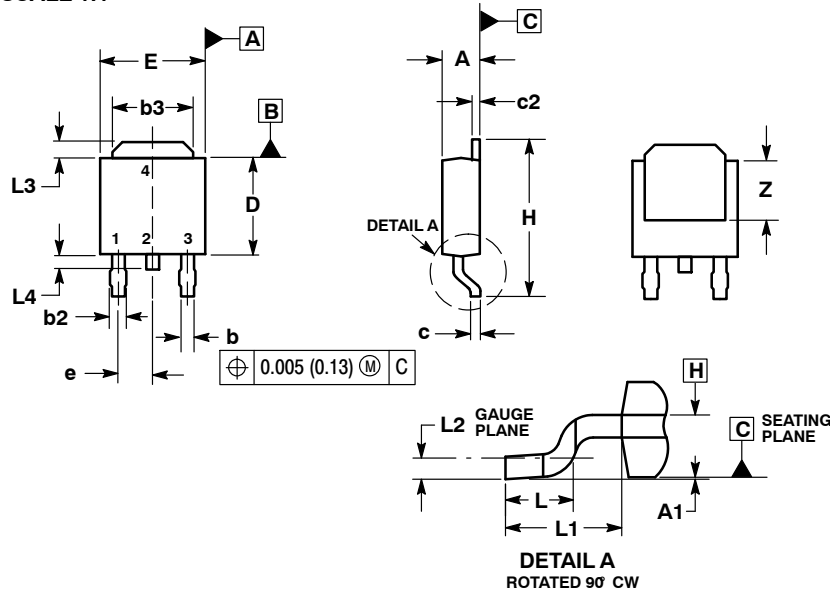
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DPAK (SINGLE GAUGE)

CASE 369AA-01

ISSUE B

DATE 03 JUN 2010



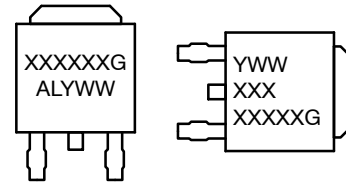
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

- | | | | |
|--|---|--|--|
| <p>STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR</p> | <p>STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN</p> | <p>STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE</p> | <p>STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE</p> |
| <p>STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE</p> | <p>STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2</p> | <p>STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR</p> | |

GENERIC MARKING DIAGRAM*

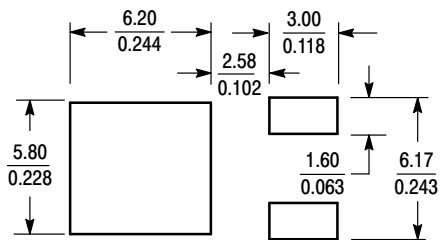


IC Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDETRM/D.

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| DESCRIPTION: | DPAK (SINGLE GAUGE) | PAGE 1 OF 1 |

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