NLAS5213

1 Ω R_{ON} DPST and Dual SPST Switches

The NLAS5213A and NLAS5213B are DPST and Dual SPST devices, respectively. They each consist of 2 single throw switches and are both designed for audio applications within portable devices. The NLAS5213A is controlled with a single enable pin while the NLAS5213B has two independent enables.

Both the NLAS5213A and NLAS5213B operate over a wide V_{CC} range, 1.65 V to 4.5 V, and maintain a very low R_{ON}: 1.3 Ω Max @ V_{CC} = 4.2 V. Each is available in a choice of two packages: US8 and UDFN8.

Features

- PST and Dual SPST Pinouts
- R_{ON}: 1.3 Ω Max @ V_{CC} = 4.2 V
- V_{CC} Range: 1.65 V to 4.5 V
- 8 kV Human Body Model ESD on I/O to GND
- UDFN8 or US8 Packages Available
- These are Pb−Free Devices

Typical Applications

- Mobile Phones
- Portable Devices

ON Semiconductor®

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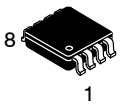
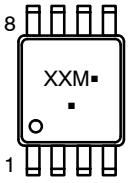
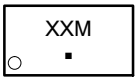
MARKING DIAGRAM



US8
US SUFFIX
CASE 493



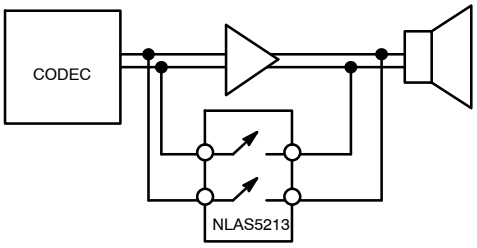
UDFN8
MU SUFFIX
CASE 517AJ



XX = Device Code
M = Date Code
▪ = Pb−Free Package

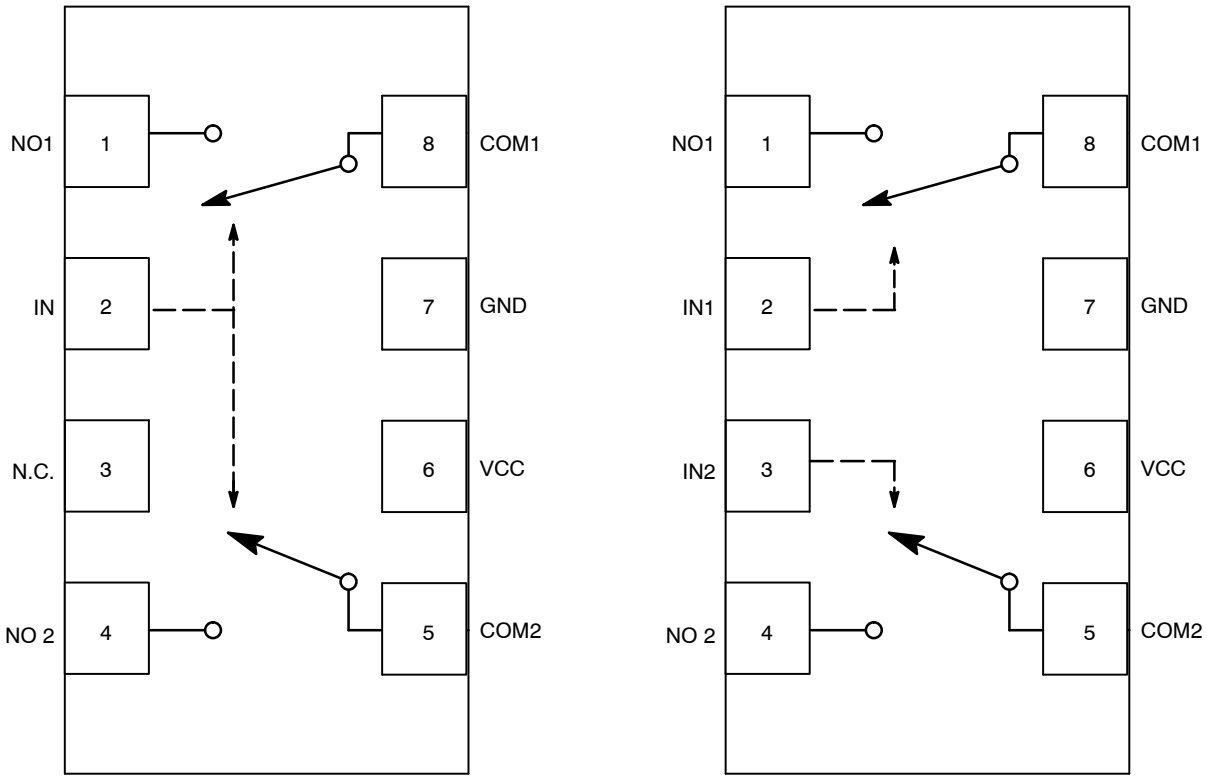
(Note: Microdot may be in either location)

APPLICATION DIAGRAM



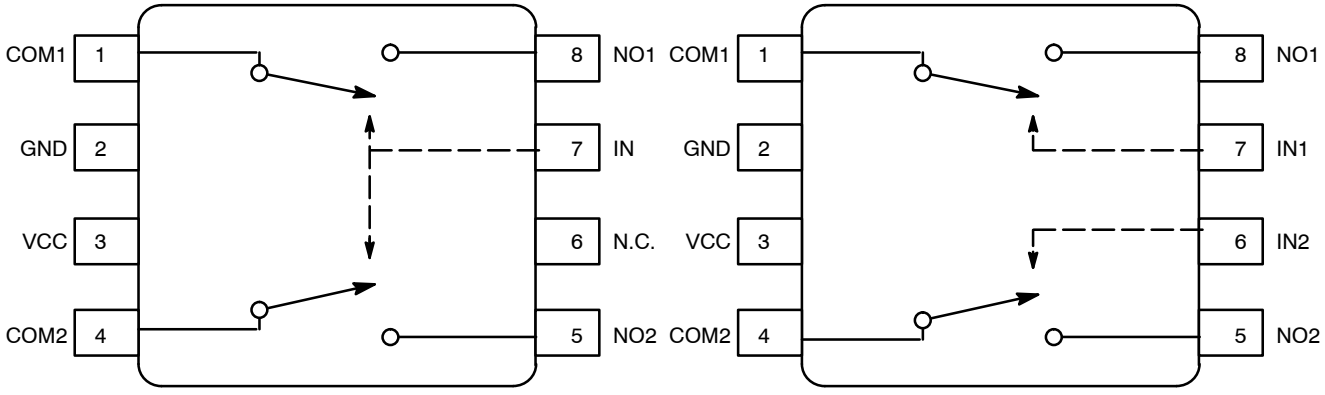
ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.



NLAS5213A **NLAS5213B**

Figure 1. Functional Block Diagram Pinouts (UDFN8)



NLAS5213A **NLAS5213B**

Figure 2. Functional Block Diagram Pinouts (US8)

NLAS5213A

Pin #		Name	Direction	Description
UDFN8	US8			
1	8	NO1	I/O	Normally Open Signal Line of Switch 1
2	7	IN	Input	Control Input
3	6	N.C.	N/A	No Connect
4	5	NO2	I/O	Normally Open Signal Line of Switch 2
5	4	COM2	I/O	Common Signal Line of Switch 2
6	3	V_{CC}	Input	Analog Supply Voltage
7	2	GND	Input	Ground
8	1	COM1	I/O	Common Signal Line of Switch 1

NLAS5213B

Pin #		Name	Direction	Description
UDFN8	US8			
1	8	NO1	I/O	Normally Open Signal Line of Switch 1
2	7	IN1	Input	Control Input of Switch 1
3	6	IN2	Input	Control Input of Switch 2
4	5	NO2	I/O	Normally Open Signal Line of Switch 2
5	4	COM2	I/O	Common Signal Line of Switch 2
6	3	V_{CC}	Input	Analog Supply Voltage
7	2	GND	Input	Ground
8	1	COM1	I/O	Common Signal Line of Switch 1

NLAS5213A FUNCTION TABLE

IN	NO1, NO2
0	OFF
1	ON

NLAS5213B FUNCTION TABLE

IN	NO1, NO2
0	OFF
1	ON

OPERATING CONDITIONS

MAXIMUM RATINGS

Symbol	Pins	Parameter	Value	Condition	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	−0.5 to 5.5		V
V_{IS}	NOx, NCx, COMx	Analog Signal Voltage	−0.5 to V_{CC} + 0.5		V
V_{IN}	IN1, IN2	Control Input Voltage	−0.5 to 5.5		V
I_{CC}	V_{CC}	Positive DC Supply Current	50		mA
I_{IS_CON}	NOx, NCx, COMx	Analog Signal Continues Current	±300	Closed Switch	mA
I_{IS_PK}	NOx, NCx, COMx	Analog Signal Peak Current	±500	10% Duty Cycle	mA
I_{IN}	IN	Control Input Current	±20		mA
T_{STG}		Storage Temperature Range	−65 to 150		ºC

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS*

Symbol	Pins	Parameter	Value	Condition	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	1.65 to 4.5		V
V_{IS}	NOx, NCx, COMx	Analog Signal Voltage	0 to V_{CC}		V
V_{IN}	IN1, IN2	Control Input Voltage	0 to V_{CC}		V
T_A		Operating Temperature Range	−40 to 85		ºC

Minimum and maximum values are guaranteed through test or design across the **Recommended Operating Conditions**, where applicable. Typical values are listed for guidance only and are based on the particularconditions listed for each section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

ESD PROTECTION

Symbol	Parameter	Value	Unit
ESD	Human Body Model I/O to GND All Pins	 8.0 4.0	kV

DC ELECTRICAL CHARACTERISTICS

CONTROL INPUT (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	−40°C to +85°C			Unit
					Min	Typ	Max	
V_{IH}	$\overline{OE}$	Control Input HIGH Voltage		2.7 3.3 4.2	1.4 1.7 2.3	–	–	V
V_{IL}	$\overline{OE}$	Control Input LOW Voltage		2.7 3.3 4.2	–	–	0.5 0.5 0.8	V
I_{IN}	$\overline{OE}$	Control Input Leakage Current	$0 \le V_{IS} \le V_{CC}$	1.65 – 4.5	–	–	±1.0	μA

SUPPLY CURRENT AND LEAKAGE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
I_{CC}	V_{CC}	Quiescent Supply Current	V_{IS} = V_{CC} or GND; I_D = 0 A	1.65 – 4.5	–	–	1.0	μA
I_{CCT}	V_{CC}	Increase in I_{CC} per Control Voltage	V_{IN} = 2.6 V	3.6	–	–	10.0	μA
I_{OZ}		OFF State Leakage	0 ≤ V_{IS} ≤ V_{CC}	1.65 – 4.5	–	–	±1.0	μA
I_{OFF}	D+, D–	Power OFF Leakage Current	0 ≤ V_{IS} ≤ V_{CC}	0	–	–	±1.0	μA

ON RESISTANCE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
R_{ON}		On–Resistance	I_{ON} = –100 mA V_{IS} = 0 to V_{CC}	2.7 3.3 4.2	–		2.0 1.4 1.3	Ω
R_{FLAT}		On–Resistance Flatness	I_{ON} = –100 mA V_{IS} = 0 to V_{CC}	2.7 3.3 4.2	–	0.32 0.35 0.37	–	Ω
ΔR_{ON}		On–Resistance Matching	I_{ON} = –100 mA V_{IS} = 0 to V_{CC}	2.7 3.3 4.2	–	0.16 0.16 0.15	–	Ω

AC ELECTRICAL CHARACTERISTICS

TIMING/FREQUENCY (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
t_{ON}	Closed to Open	Turn–ON Time		1.65 – 4.5	–	20	–	ns
t_{OFF}	Open to Closed	Turn–OFF Time		1.65 – 4.5	–	15	–	ns
BW		–3 dB Bandwidth	C_L = 5 pF	1.65 – 4.5	–	496	–	MHz

ISOLATION (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
O_{IRR}	Open	OFF–Isolation		1.65 – 4.5	–	–57	–	dB
X_{TALK}	HSD+, HSD–	Non–Adjacent Channel Crosstalk		1.65 – 4.5	–	–97	–	dB

CAPACITANCE (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	–40°C to +85°C			Unit
				Min	Typ	Max	
C_{IN}	$\overline{OE}$	Control Pin Input Capacitance	V_{CC} = 0 V	–	8.5	–	pF
C_{ON}	HSD+, to D+	ON Capacitance	V_{IN} = 0 V	–	32	–	pF
C_{OFF}	HSD+, HSD–	OFF Capacitance	V_{IS} = 3.3 V; V_{IN} = 3.3 V	–	19	–	pF

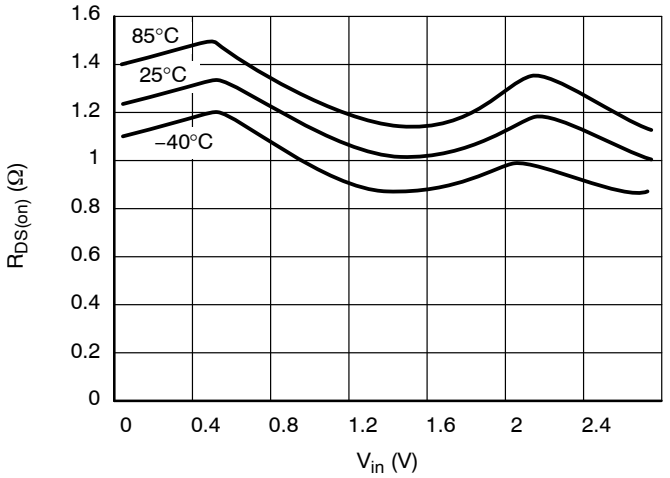


Figure 3. R_{ON} @ V_{CC} = 2.7 V

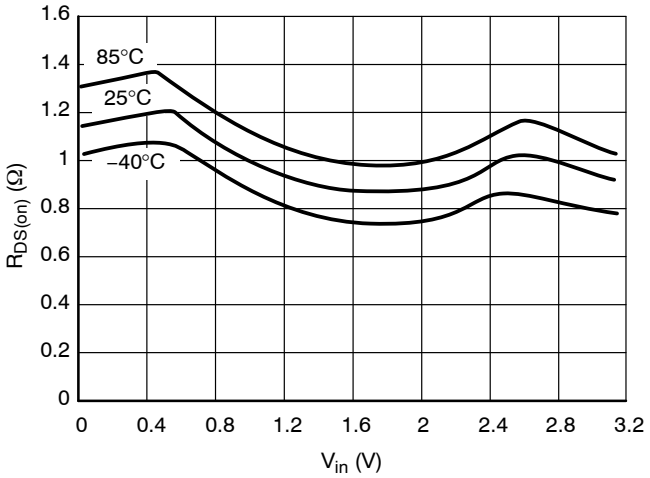


Figure 4. R_{ON} @ V_{CC} = 3.3 V

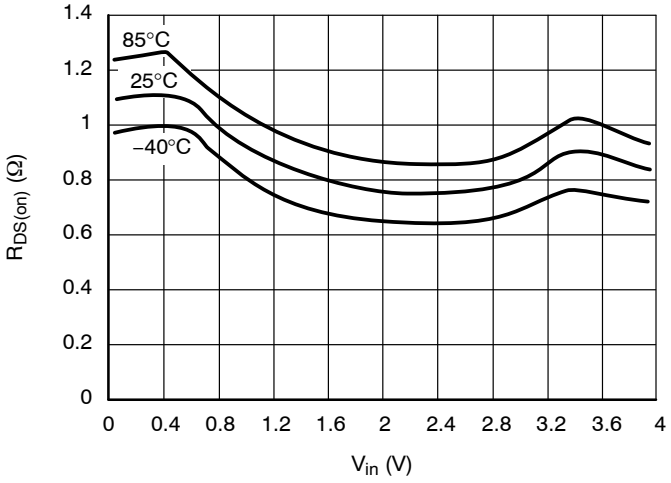


Figure 5. R_{ON} @ V_{CC} = 4.2 V

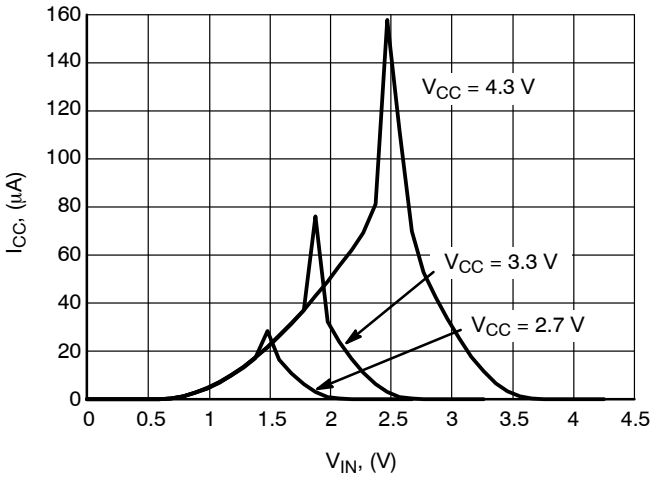


Figure 6. I_{CC} vs. V_{IN}

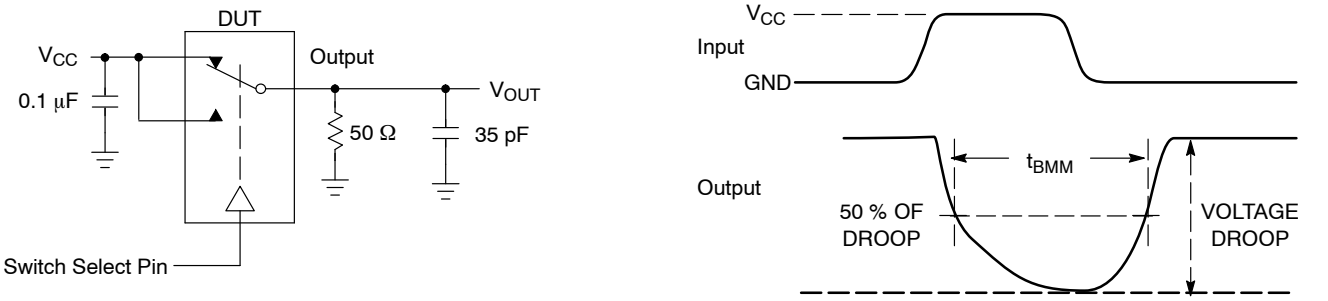


Figure 7. t_{BBM} (Time Break−Before−Make)

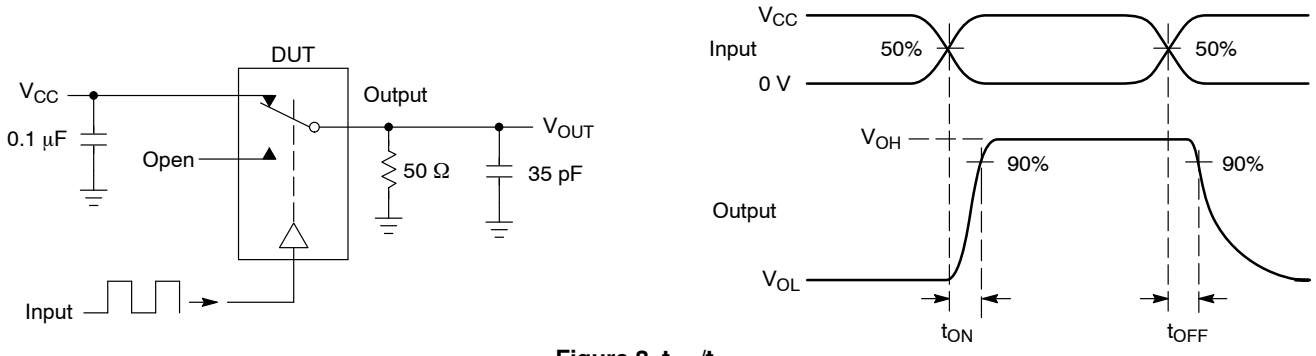


Figure 8. t_{ON}/t_{OFF}

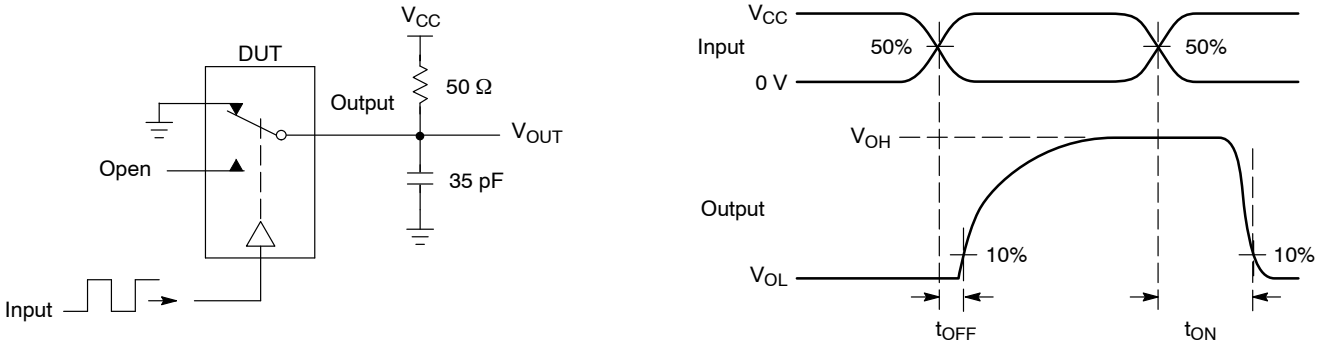
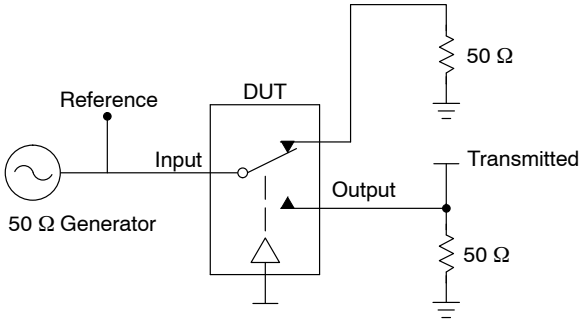


Figure 9. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 10. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

DEVICE ORDERING INFORMATION

Device	Marking	Package Type	Shipping†
NLAS5213AUSG	VD	US8 (Pb−Free)	3,000 / Tape & Reel
NLAS5213AMUTAG	VD	UDFN8 (Pb−Free)	3,000 / Tape & Reel
NLAS5213BUSG	VE	US8 (Pb−Free)	3,000 / Tape & Reel
NLAS5213BMUTAG	VE	UDFN8 (Pb−Free)	3,000 / Tape & Reel

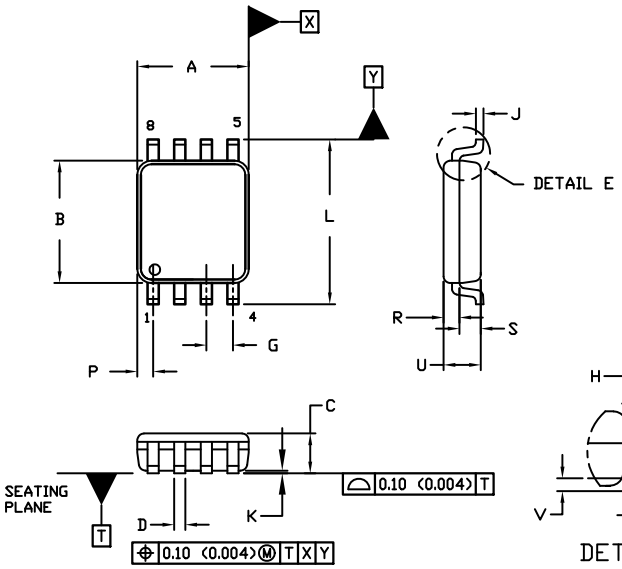
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

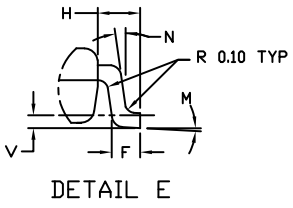
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 4 :1

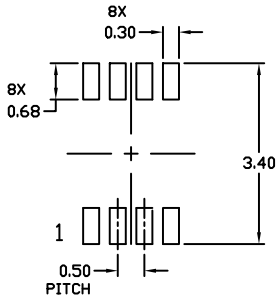
US8
CASE 493
ISSUE F

DATE 01 SEP 2021





DETAIL E



RECOMMENDED *
MOUNTING FOOTPRINT

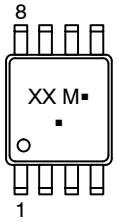
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR. MOLD FLASH, PROTRUSION, OR GATE BURR SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076–0.0203 MM (0.003–0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 MM (0.002").

	MILLIMETERS		INCHES	
DIM	MIN.	MAX.	MIN.	MAX.
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.25	0.118	0.128
M	0°	6°	0°	6°
N	0°	10°	0°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

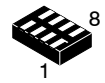
DOCUMENT NUMBER:	**98AON04475D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**US8**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

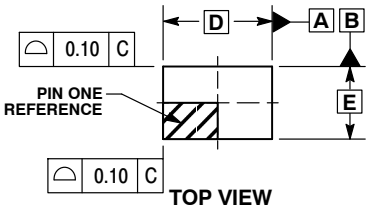
ON Semiconductor®

UDFN8 1.8x1.2, 0.4P
CASE 517AJ−01
ISSUE O

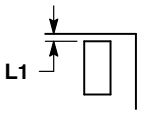
DATE 08 NOV 2006



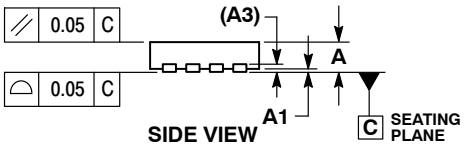
SCALE 4:1



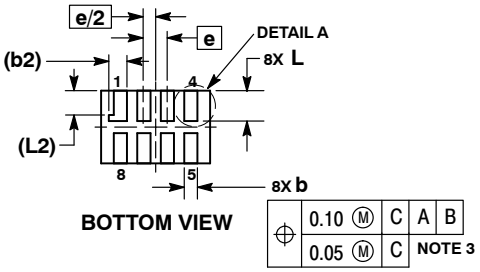
TOP VIEW



DETAIL A
NOTE 5



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

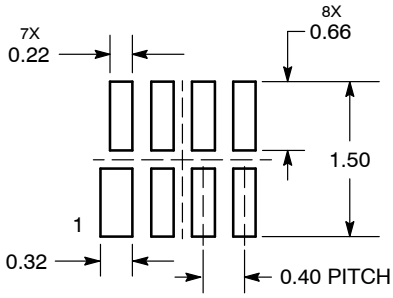
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
b2	0.30 REF	
D	1.80 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.45	0.55
L1	0.00	0.03
L2	0.40 REF	

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

MOUNTING FOOTPRINT SOLDERMASK DEFINED



DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	**98AON23417D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**UDFN8 1.8X1.2, 0.4P**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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