

FDS6675BZ

MOSFET – P-Channel, POWERTRENCH®

-30 V, -11 A, 13 mΩ

Description

This P-Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features

- Max $R_{DS(on)}$ = 13 mΩ at $V_{GS} = -10$ V, $I_D = -11$ A
- Max $R_{DS(on)}$ = 21.8 mΩ at $V_{GS} = -4.5$ V, $I_D = -9$ A
- Extended V_{GS} Range (-25 V) for Battery Applications
- HBM ESD Protection Level of 5.4 kV Typical (Note 3)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- This Device is Pb-Free and RoHS Compliant

Specifications

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	-30	V
V_{GS}	Gate to Source Voltage	±25	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	-11 -55	A
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	2.5 1.2 1.0	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

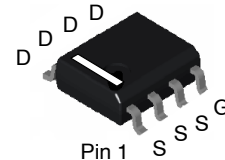
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	



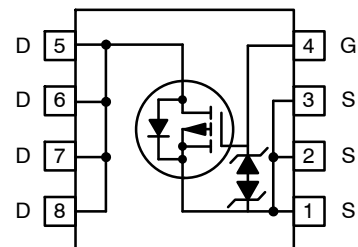
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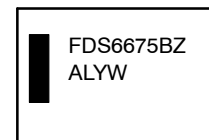


**SOIC8
CASE 751EB**

ELECTRICAL CONNECTION



MARKING DIAGRAM



FDS4435BZ = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

Device	Package	Shipping†
FDS6675BZ	SOIC8 (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDS6675BZ

Table 1. ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	-30			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, referenced to 25°C		-20		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V}$, $V_{GS} = 0 \text{ V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}$, $V_{DS} = 0 \text{ V}$			± 10	μA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250 \mu\text{A}$	-1	-2	-3	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, referenced to 25°C		15.7		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10 \text{ V}$, $I_D = -11 \text{ A}$		10.8	13.0	$\text{m}\Omega$
		$V_{GS} = -4.5 \text{ V}$, $I_D = -9 \text{ A}$		17.4	21.8	
		$V_{GS} = -10 \text{ V}$, $I_D = -11 \text{ A}$, $T_J = 125^\circ\text{C}$		15.0	18.8	
g_{FS}	Forward Transconductance	$V_{DS} = -5 \text{ V}$, $I_D = -11 \text{ A}$		34		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		1855	2470	pF
C_{oss}	Output Capacitance			335	450	pF
C_{rss}	Reverse Transfer Capacitance			330	500	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15 \text{ V}$, $I_D = -11 \text{ A}$, $V_{GS} = -10 \text{ V}$, $R_{GS} = 6 \Omega$		3.0	10	ns
t_r	Rise Time			7.8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			120	200	ns
t_f	Fall Time			60	100	ns
Q_g	Total Gate Charge	$V_{DS} = -15 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -11 \text{ A}$		44	62	nC
Q_g	Total Gate Charge	$V_{DS} = -15 \text{ V}$, $V_{GS} = -5 \text{ V}$, $I_D = -11 \text{ A}$		25	35	nC
Q_{gs}	Gate to Source Charge			7.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			11.4		nC

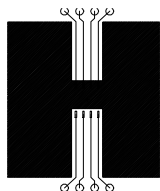
DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = -2.1 \text{ A}$		-0.7	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -11 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$			42	ns
Q_{rr}	Reverse Recovery Charge	$I_F = -11 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$			30	nC

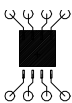
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

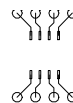
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $105^\circ\text{C}/\text{W}$ when mounted on a 0.04 in^2 pad of 2 oz copper.



c. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad

- Pulse Test: Pulse Width $< 300 \mu\text{s}$, Duty cycle $< 2.0\%$.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

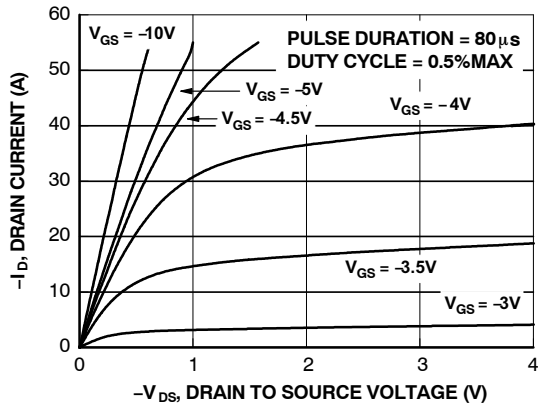


Figure 1. On-Region Characteristics

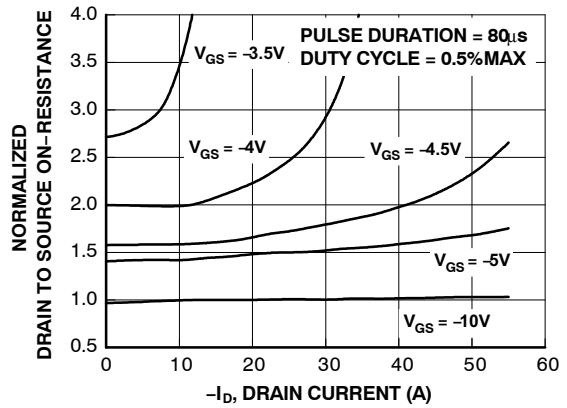


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

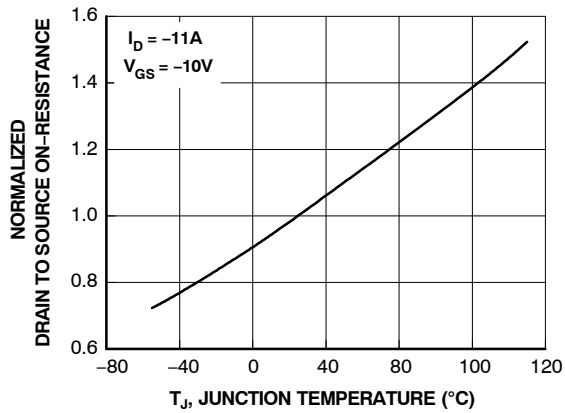


Figure 3. Normalized On-Resistance vs Junction Temperature

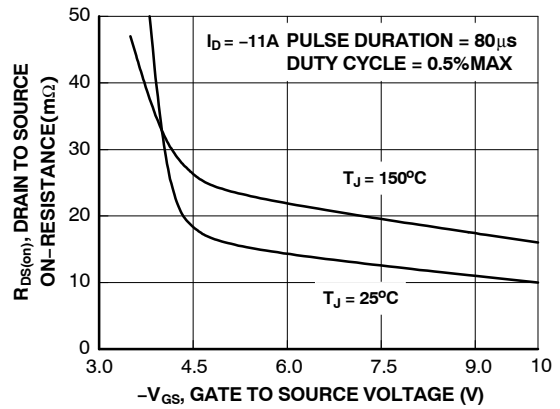


Figure 4. On-Resistance vs Gate to Source Voltage

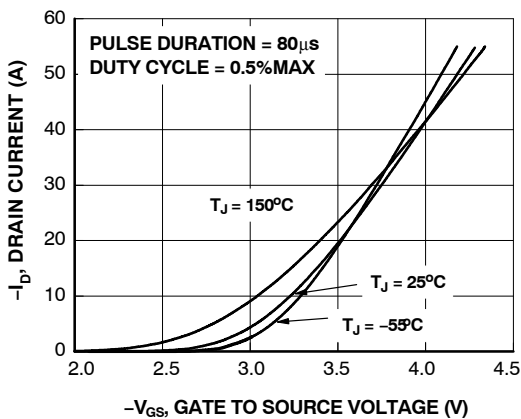


Figure 5. Transfer Characteristics

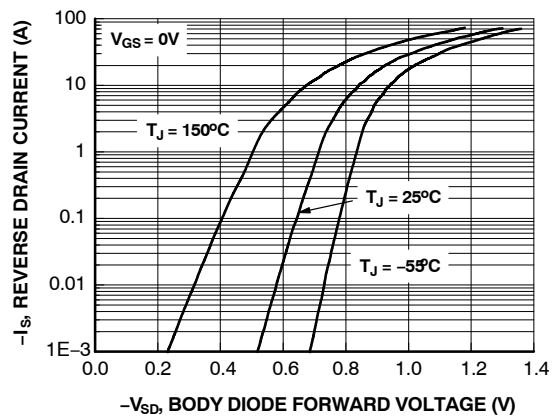


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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TYPICAL CHARACTERISTICS (Continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

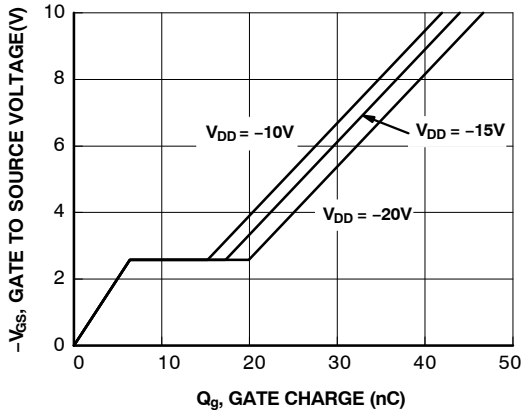


Figure 7. Gate Charge Characteristics

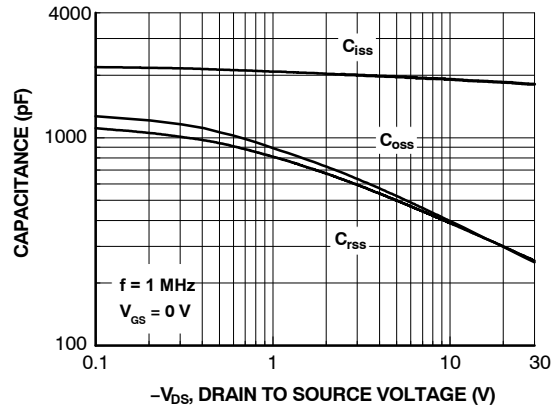


Figure 8. Capacitance vs Drain to Source Voltage

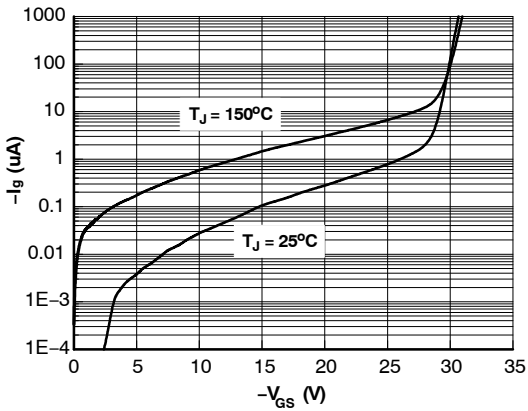


Figure 9. I_g vs V_{GS}

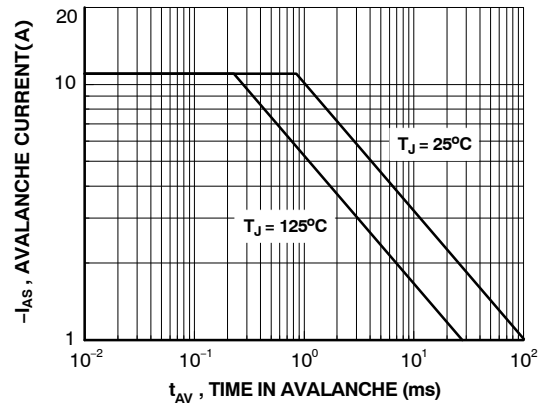


Figure 10. Unclamped Inductive Switching Capability

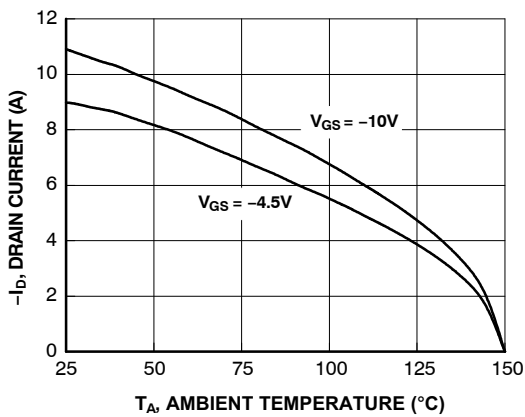


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

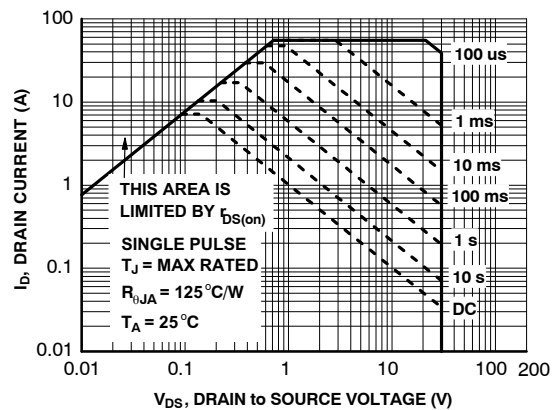


Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS (Continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

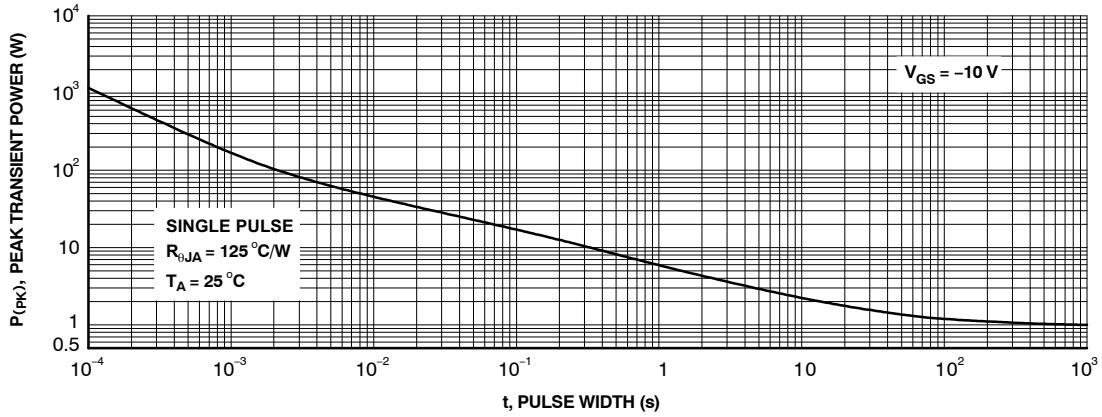


Figure 13. Single Pulse Maximum Power Dissipation

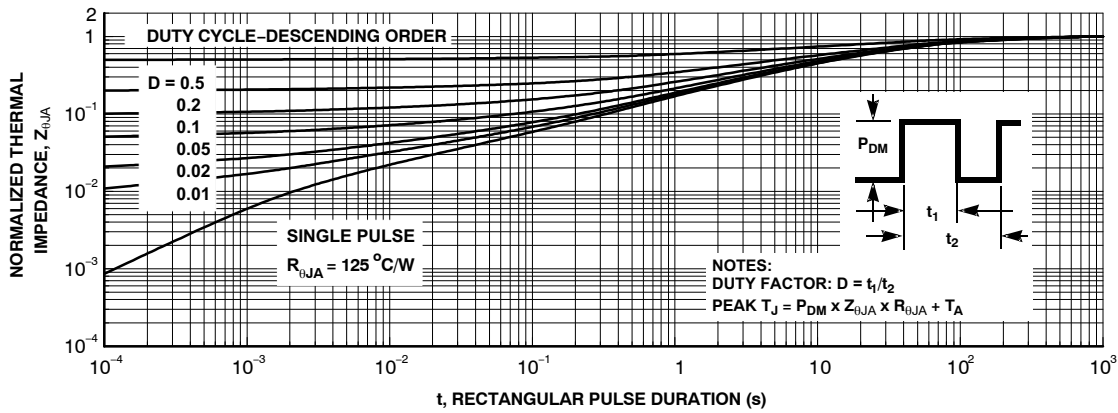


Figure 14. Junction To Ambient Transient Thermal Response Curve

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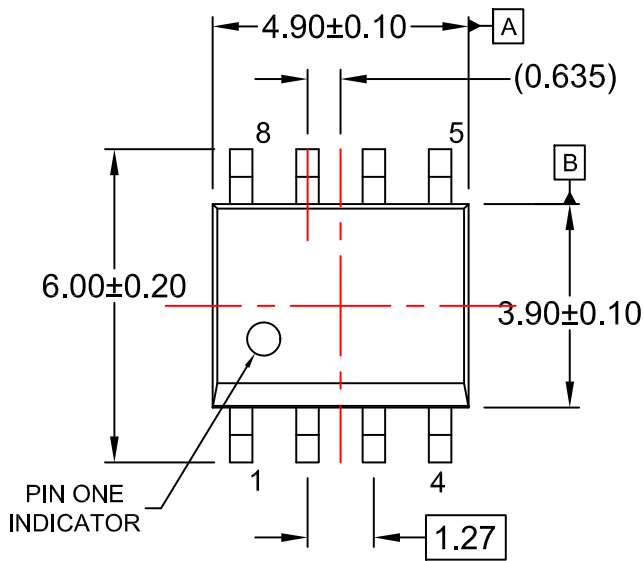
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

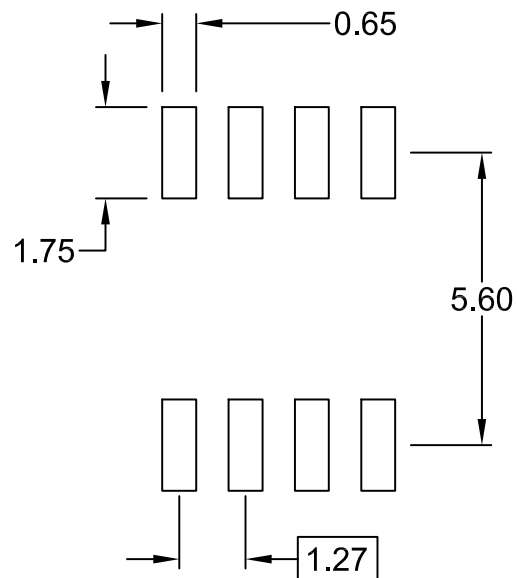


SOIC8
CASE 751EB
ISSUE A

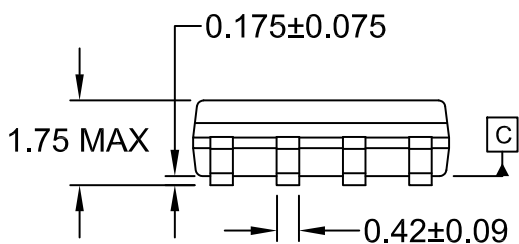
DATE 24 AUG 2017



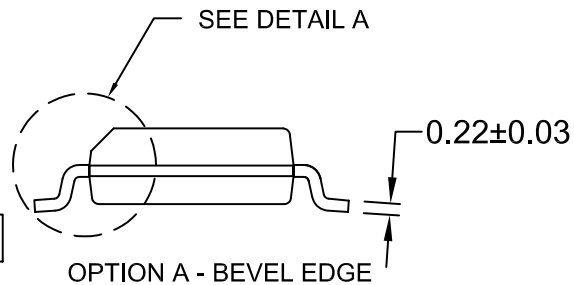
\varnothing 0.25 (M) C B A



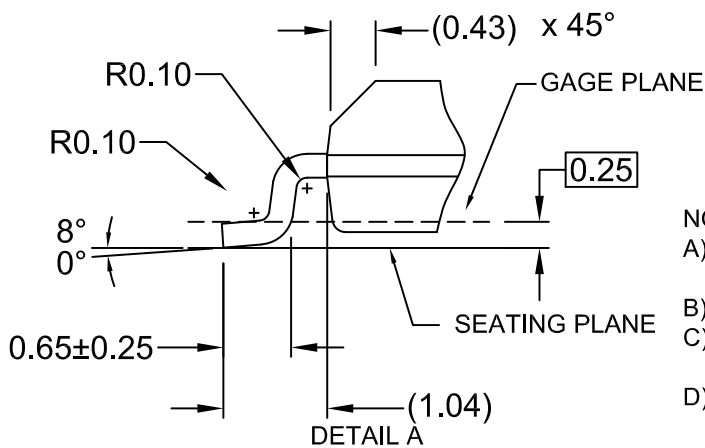
LAND PATTERN RECOMMENDATION



$\frac{1}{2}$ 0.10



OPTION B - NO BEVEL EDGE



DETAIL A
 SCALE: 2:1

NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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