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NCP1337

PWM Current-Mode Controller for Free Running Quasi-Resonant Operation

The NCP1337 combines a true current mode modulator and a demagnetization detector which ensures full Borderline/Critical Conduction Mode in any load/line conditions together with minimum drain voltage switching (Quasi−Resonant operation). The transformer core reset detection is done internally, without using any external signal, due to the Soxyless concept. The frequency is internally limited to 130 kHz, preventing the controller to operate above the 150 kHz CISPR−22 EMI starting limit.

By monitoring the feedback pin activity, the controller enters skip mode as soon as the power demand falls below a predetermined level. As each restart is softened by an internal Soft−Skip™, and as the frequency cannot go below 25 kHz, no audible noise can be heard.

The NCP1337 also features an efficient protective circuitry which, in presence of an overcurrent condition, disables the output pulses and enters a safe burst mode, trying to restart. Once the default has gone, the device auto−recovers. Also included is a bulk voltage monitoring function (known as brown−out protection), an adjustable overpower compensation, and a V_{CC} OVP. The controller immediately restarts after any of these conditions, unless the fault timer has timed out. Finally, an internal 4.0 ms soft−start eliminates the traditional startup stress.

Features

- Free−Running Borderline/Critical Mode Quasi−Resonant Operation
- Current−Mode
- Soft−Skip Mode with Minimum Switching Frequency for Standby
- Auto−Recovery Short−Circuit Protection Independent of Auxiliary Voltage
- Overvoltage Protection
- Brown−Out Protection
- Two Externally Triggerable Fault Comparators (one for a disable function, and the other for a permanent latch)
- Internal 4.0 ms Soft−Start
- 500 mA Peak Current Drive Sink Capability
- 130 kHz Max Frequency
- Internal Leading Edge Blanking
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- Dynamic Self−Supply with Levels of 12 V (On) and 10 V (Off)
- SPICE Models Available for TRANsient and AC Analysis
- These are Pb−Free Devices

Typical Applications

- AC−DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Consumer Electronics (DVD Players, Set−Top Boxes, TVs, etc.)
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

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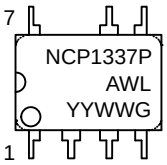
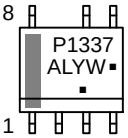
MARKING DIAGRAM

PDIP−7
P SUFFIX
CASE 626B



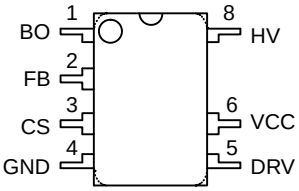
SOIC−7
D SUFFIX
CASE 751U



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G, ▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1337PG	PDIP−7 (Pb−Free)	50 Units/Rail
NCP1337DR2G	SOIC−7 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Function	Description
1	BO	Brown−out and external triggering	• By connecting this pin to the input voltage through a resistor divider, the controller ensures operation at a safe mains level, thanks to a 500 mV brown−out comparator. • If an external event brings this pin above 3.0 V, the controller's output is disabled. • If an external event brings this pin above 5.0 V, the controller is permanently latched−off.
2	FB	Sets the peak current setpoint	• By connecting an optocoupler or an auxiliary winding to this pin, the peak current setpoint is adjusted accordingly to the output power demand. • When the requested peak current setpoint is below the internal standby level, the device enters Soft−Skip mode.
3	CS	Current sense input and overpower compensation adjustment	• This pin senses the primary current and routes it to the internal comparator via an L.E.B. • Inserting a resistor in series with the pin allows to control the overpower compensation level.
4	GND	IC ground	
5	DRV	Output driver	• To be connected to an external MOSFET.
6	VCC	IC supply	• Connected to a tank capacitor (and possibly an auxiliary winding). • When V_{CC} reaches 18.6 V, an internal OVP stops the output pulses.
8	HV	High−voltage pin	• Connected to the high−voltage rail, this pin injects a constant current into the V_{CC} bulk capacitor and ensures a clean lossless startup sequence.

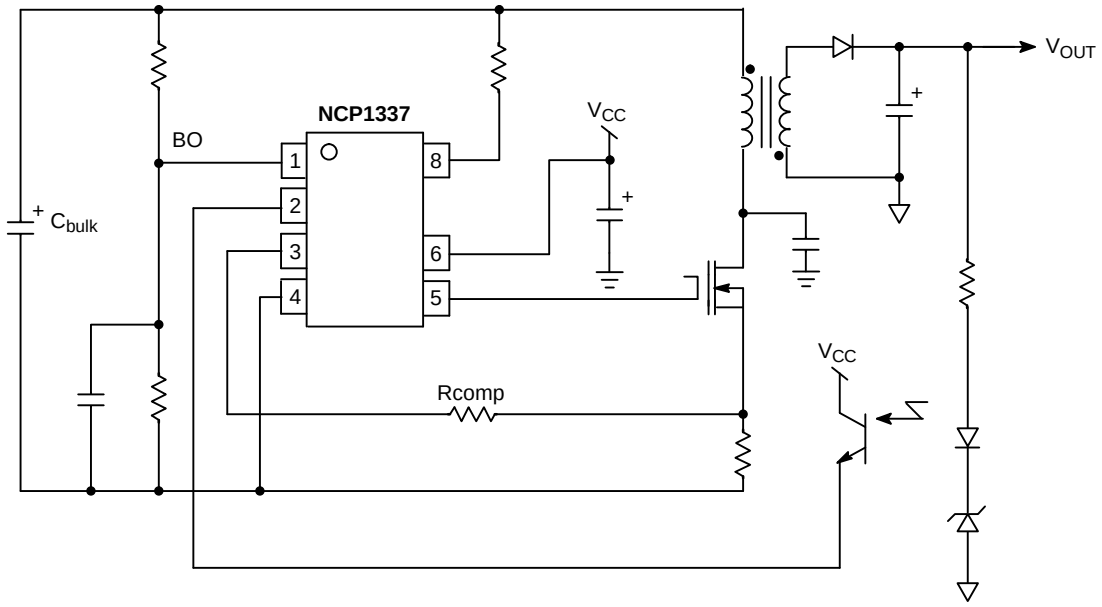


Figure 1. Typical Application Schematic

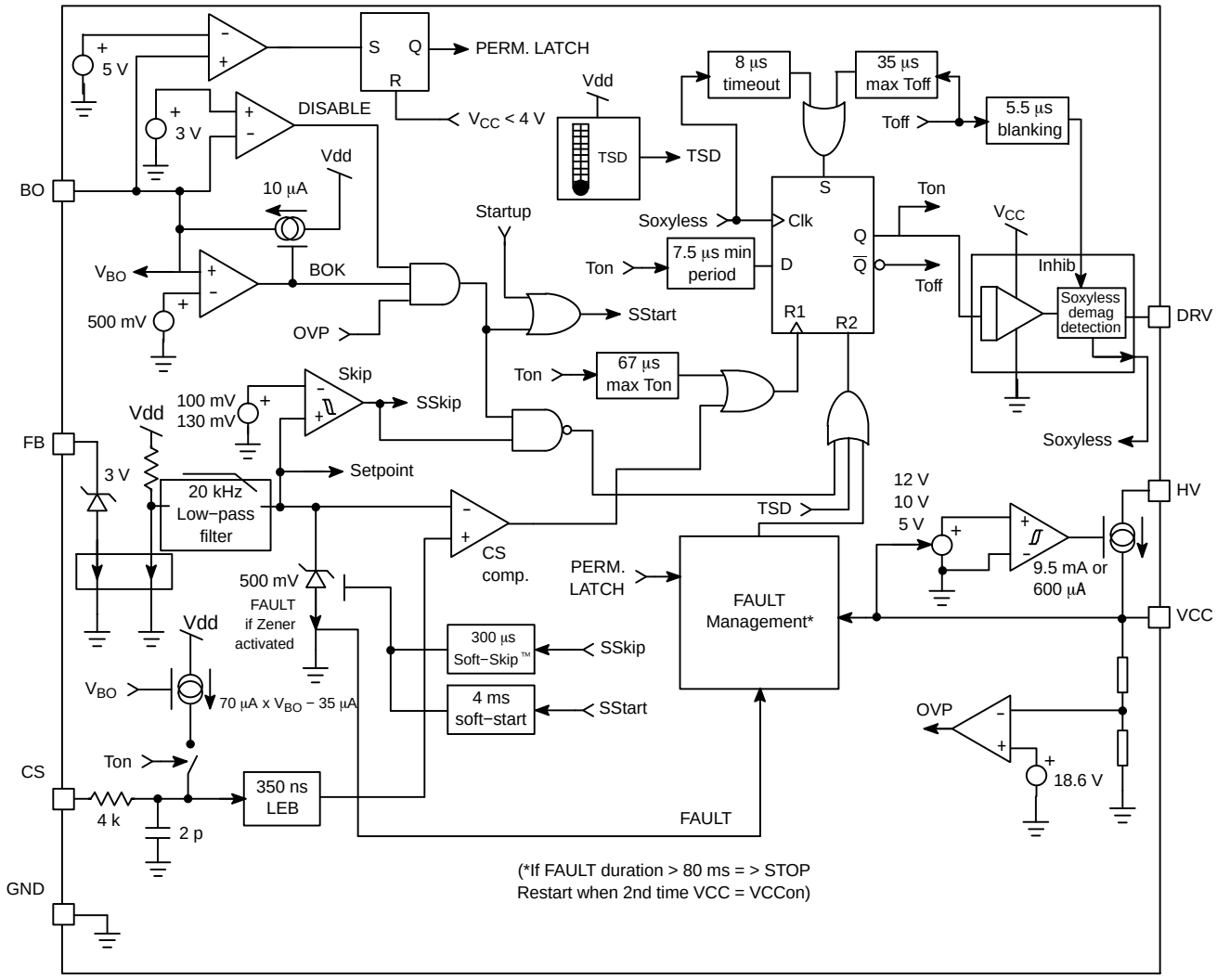


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage on Pin 8 (HV) when Pin 6 (V_{CC}) is Decoupled to Ground with 10 μF	V_{HV}	−0.3 to 500	V
Maximum Current in Pin 8 (HV)	−	20	mA
Power Supply Voltage, Pin 6 (V_{CC}) and Pin 5 (DRV)	V_{CCmax}	−0.3 to 20	V
Maximum Current in Pin 6 (V_{CC})	−	±30	mA
Maximum V_{CC} Slew Rate (dV/dt)	dV_{CC}/dt	9.0	V/ms
Maximum Voltage on all Pins except Pin 8 (HV), Pin 6 (V_{CC}) and Pin 5 (DRV)	−	−0.3 to 10	V
Maximum Current into all Pins except Pin 8 (HV), Pin 6 (V_{CC}) and Pin 5 (DRV)	−	±10	mA
Maximum Current into Pin 6 (DRV) during ON Time and T_{BLANK}	−	±1.0	A
Maximum Current into Pin 6 (DRV) after T_{BLANK} during OFF Time	−	±15	mA
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	57	°C/W
Thermal Resistance, Junction−to−Air, SOIC Version	$R_{\theta JA}$	178	°C/W
Thermal Resistance, Junction−to−Air, DIP Version	$R_{\theta JA}$	100	°C/W
Maximum Junction Temperature	TJ_{MAX}	150	°C
Operating Temperature Range	−	−40 to +125	°C
Storage Temperature Range	−	−60 to +150	°C
ESD Capability, HBM Model per JESD22, Method A114E (All Pins except HV)	−	2.0	kV
ESD Capability, Machine Model per JESD22, Method A115A	−	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latchup protection and exceeds 100 mA per JEDEC standard JESD78.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, Max T_J = 150°C, V_{CC} = 11 V, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION						
V_{CC} Increasing Level at which the Controller Starts	6	VCC_{ON}	11	12	13	V
V_{CC} Decreasing Level at which the Controller Stops	6	VCC_{MIN}	9.0	10	11	V
Protection Mode is Activated if V_{CC} reaches this Level whereas the HV Current Source is ON	6	VCC_{OFF}	−	9.0	−	V
V_{CC} Decreasing Level at which the Latch−Off Phase Ends	6	VCC_{LATCH}	3.6	5.0	6.0	V
Margin between V_{CC} Level at which Latch Fault is Released and VCC_{LATCH}	−	V_{MARGIN}	0.3	−	−	V
V_{CC} Increasing Level at which the Controller Enters Protection Mode	6	VCC_{OVP}	17.6	18.6	19.6	V
V_{CC} Level below which HV Current Source is Reduced	6	VCC_{INHIB}	−	1.5	−	V
Internal IC Consumption, No Output Load on Pin 5, F_{SW} = 60 kHz	6	ICC1	−	1.2	−	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 60 kHz	6	ICC2	−	2.0	−	mA
Internal IC Consumption, Latch−Off Phase, V_{CC} = 8.0 V	6	ICC3	−	600	−	μA
Internal IC Consumption in Skip	6	ICC_{LOW}	−	600	−	μA
INTERNAL STARTUP CURRENT SOURCE						
Minimum Guaranteed Startup Voltage on HV Pin	8	V_{HVmin}	−	−	55	V
High−Voltage Current Source when V_{CC} > VCC_{INHIB} (V_{CC} = 10.5 V, V_{HV} = 60 V)	8	IC1	5.5	9.5	15	mA
High−Voltage Current Source when V_{CC} < VCC_{INHIB} (V_{CC} = 0 V, V_{HV} = 60 V)	8	IC2	0.3	0.6	1.1	mA
Leakage Current Flowing when the HV Current Source is OFF (V_{CC} = 17 V, V_{HV} = 500 V)	8	I_{HVLeak}	−	−	90	μA
DRIVE OUTPUT						
Output Voltage Rise−Time @ CL = 1.0 nF, 10−90% of Output Signal	5	T_R	−	50	−	ns
Output Voltage Fall−Time @ CL = 1.0 nF, 10−90% of Output Signal	5	T_F	−	20	−	ns
Source Resistance	5	R_{OH}	−	20	−	Ω
Sink Resistance	5	R_{OL}	−	8.0	−	Ω
TEMPERATURE SHUTDOWN						
Temperature Shutdown	−	TSD	130	−	−	°C
Hysteresis on Temperature Shutdown	−	−	−	30	−	°C
CURRENT COMPARATOR						
Maximum Internal Current Setpoint (@ I_{FB} = $I_{FB100\%}$)	3	$V_{CSLimit}$	475	500	525	mV
Minimum Internal Current Setpoint (@ I_{FB} = $I_{FBrippleIN}$)	3	$V_{CSrippleIN}$	−	100	−	mV
Internal Current Setpoint for I_{FB} = $I_{FBrippleOUT}$	3	$V_{CSrippleOUT}$	−	130	−	mV
Propagation Delay from Current Detection to Gate OFF State	3	T_{DEL}	−	120	150	ns
Leading Edge Blanking Duration	3	T_{LEB}	−	350	−	ns
Internal Current Offset Injected on the CS Pin during ON Time (Over Power Compensation) @ 1.0 V on Pin 1 and Vpin3 = 0.5 V @ 2.0 V on Pin 1 and Vpin3 = 0.5 V	3	I_{OPC}	 − −	 35 105	 − −	μA
Maximum ON Time	5	$MaxT_{ON}$	52	67	82	μs

ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, Max T_J = 150°C, V_{CC} = 11 V, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
FEEDBACK SECTION						
FB Current under which FAULT is Detected	2	I_{FBopen}	−	40	−	μA
FB Current for which Internal Setpoint is 100%	2	$I_{FB100\%}$	−	50	−	μA
FB Current above which DRV Pulses are Stopped	2	$I_{FBrippleIN}$	−	220	−	μA
FB Current under which DRV Pulses are Reauthorized after having reached $I_{FBrippleIN}$	2	$I_{FBrippleOUT}$	−	205	−	μA
FB Current above which FB Pin Voltage is not Regulated anymore	2	$I_{FBregMax}$	−	500	−	μA
FB Pin Voltage when $I_{FBopen} < I_{FB} < I_{FBregMax}$	2	V_{FB}	2.8	3.0	3.2	V
Duration before Entering Protection Mode after FAULT Detection	−	T_{FAULT}	−	80	−	ms
Internal Soft−Start Duration (Up to $V_{CSLimit}$)	−	T_{SS}	−	4.0	−	ms
Internal Soft−Skip Duration (Up to $V_{CSLimit}$)	−	T_{SSkip}	−	300	−	μs
BROWN−OUT AND LATCH SECTION						
Brown−Out Detection Level	1	V_{BO}	460	500	540	mV
Current Flowing out of Pin 1 when Brown−Out Comparator has Toggled	1	I_{BO}	−	10	−	μA
Vpin1 Threshold that Disables the Output	1	$V_{DISABLE}$	2.8	3.0	3.3	V
Vpin1 Threshold that Activates the Permanent Latch	1	V_{LATCH}	4.75	5.0	5.25	V
DEMAGNETIZATION DETECTION BLOCK						
Current Threshold for Demagnetization Detection	5	I_{SOXYth}	−	210	−	μA
Max Voltage on DRV Pin During OFF Time after T_{BLANK} (when Sinking 15 mA)	5	$V_{DRVlowMAX}$	−	−	1.5	V
Min Voltage on DRV Pin During OFF Time after T_{BLANK} (when Sourcing 15 mA)	5	$V_{DRVlowMIN}$	−0.6	−	−	V
Propagation Delay from Demag Detection to Gate ON State (I_{GATE} Slope of 500 A/s)	5	T_{DMG}	−	180	220	ns
Blanking Window after Gate OFF State before Detecting Demagnetization	5	T_{BLANK}	−	5.5	−	μs
Timeout on Demag Signal	5	T_{OUT}	−	8.0	−	μs
Maximum OFF Time	5	$MaxT_{OFF}$	−	35	42	μs
Minimum Switching Period	5	MinPeriod	6.8	7.7	8.5	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

APPLICATION INFORMATION

INTRODUCTION

The NCP1337 implements a standard current mode architecture where the switch−off time is dictated by the peak current setpoint, whereas the core−reset detection triggers the turn−on event. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost AC−DC adapters, consumer electronics, auxiliary supplies, etc. Due to its high−performance, high−voltage technology, the NCP1337 incorporates all the necessary features needed to build a rugged and reliable Switch−Mode Power Supply (SMPS):

- **Quasi−Resonant Operation:** Valley−switching operation is ensured whatever the operating conditions are, due to the internal soxyless circuitry. As a result, there are virtually no primary switch turn−on losses, and no secondary diode recovery losses, and EMI and video noise perturbations are reduced. The converter also stays a first−order system and accordingly eases the feedback loop design.
- **Dynamic Self−Supply (DSS):** Due to its Very High Voltage Integrated Circuit (VHVIC) technology, ON Semiconductor's NCP1337 allows for a direct pin connection to the high−voltage DC rail. A dynamic current source charges up a capacitor and thus provides a fully independent V_{CC} level. As a result, low power applications will not require any auxiliary winding to supply the controller. In applications where this winding is anyway required (see "Power Dissipation" section in the application note), the DSS will simplify the V_{CC} capacitor selection.
- **Overcurrent Protection (OCP):** When the feedback current is below minimum value, a fault is detected. If this fault is present for more than 80 ms, NCP1337 enters an auto−recovery soft burst mode. All pulses are stopped and the V_{CC} capacitor discharges down to 5.0 V. Then, by monitoring the V_{CC} level, the startup current source is activated ON and OFF to create a burst mode. After the current source being activated twice, the controller tries to restart, with a 4.0 ms soft−start. If the fault has gone, the SMPS resumes operation. If the fault is still there, the burst sequence starts again. The soft−start, together with a minimum frequency clamp, allow to reduce the noise generated in the transformer in short−circuit conditions.
- **Overvoltage Protection (OVP):** By continuously monitoring the V_{CC} voltage level, the NCP1337 stops switching whenever an overvoltage condition is detected.
- **Brown−Out Detection (BO):** By monitoring the level on Pin 1 during normal operation, the controller protects the SMPS against low mains condition. When Pin 1 level falls below 500 mV, the controller stops switching until this level goes back and resumes operation, unless the fault timer has timed out. By adjusting the resistor divider connected between the high input voltage and this pin, start and stop levels are programmable.
- **Over Power Compensation (OPC):** An internal current source injects out of Pin 3 (CS pin) a current proportional to the voltage applied on Pin 1. As this voltage is an image of the input voltage, by inserting a resistor in series with Pin 3, it is possible to create an offset on the current sense signal that will compensate the effect of the input voltage variation.
- **External Latch Trip Point:** By externally forcing a level on Pin 1 (e.g., with a signal coming from a temperature sensor) greater than 3.0 V (but below 5.0 V), it is possible to disable the output of the controller. If the voltage is forced over 5.0 V, the controller is permanently latched−off: to resume normal operation, the V_{CC} voltage should go below 4.0 V, which implies to unplug the SMPS from the mains.
- **Standby Ability:** Under low load conditions, NCP1337 enters a Soft−Skip mode: when the CS setpoint becomes lower than 20% of the maximum peak current, output pulses are stopped, then switching is starting again when FB loop forces a setpoint higher than 25%. As this occurs at low peak current, with Soft−Skip activated, and as the T_{OFF} is clamped, noise−free operation is guaranteed, even with a cheap transformer.

Timing Diagrams

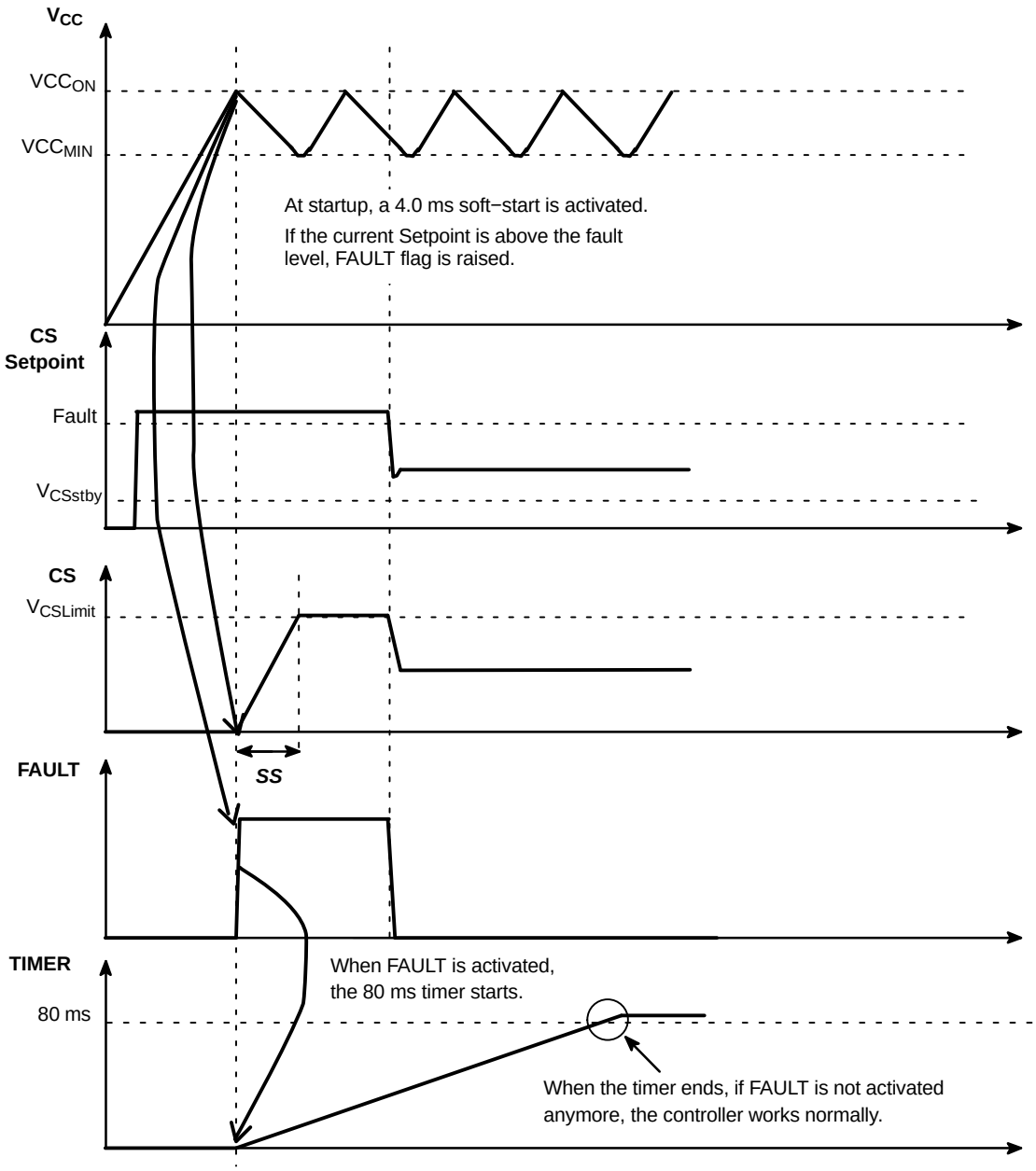


Figure 3. Startup Sequence

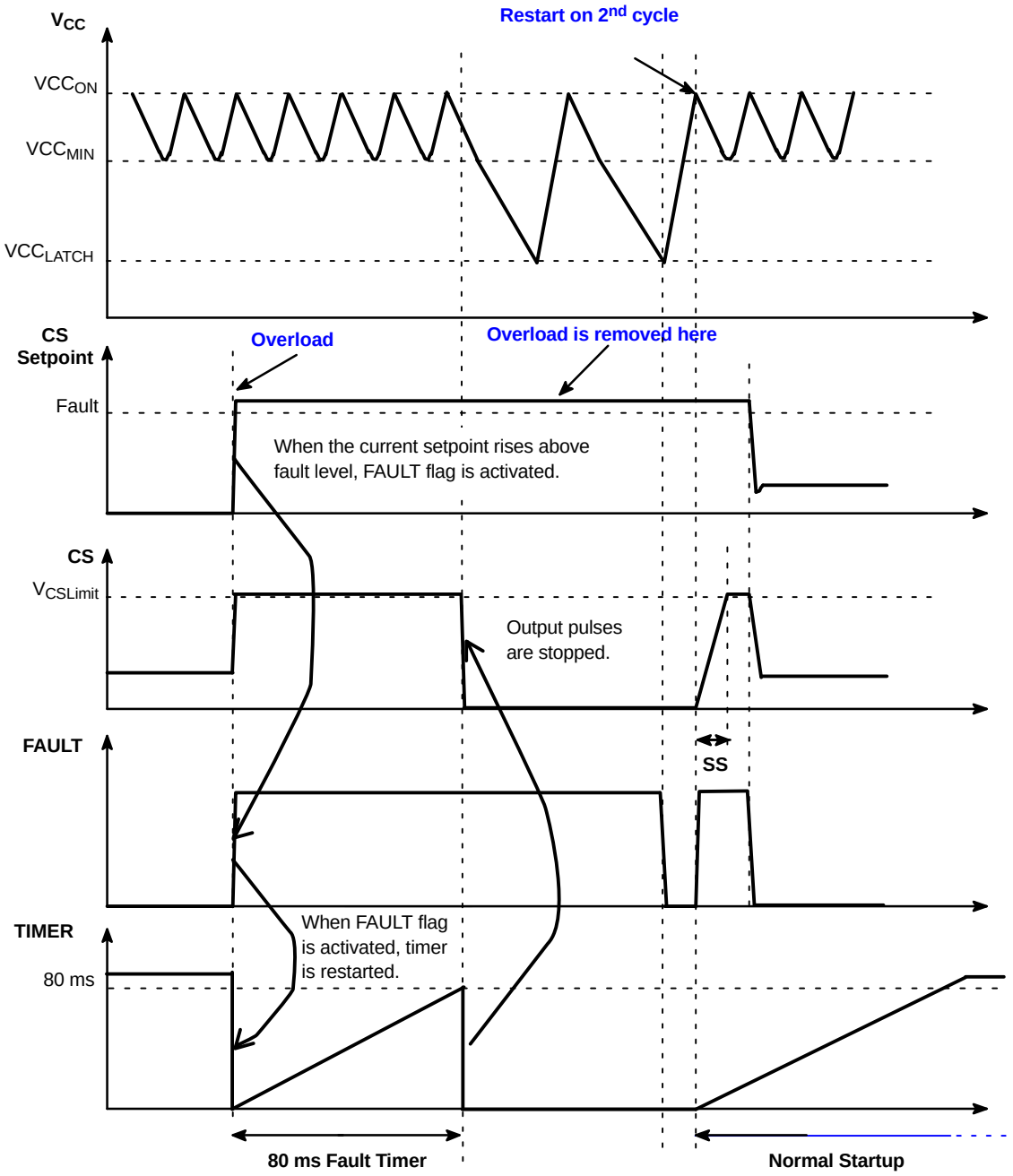


Figure 4. Overload

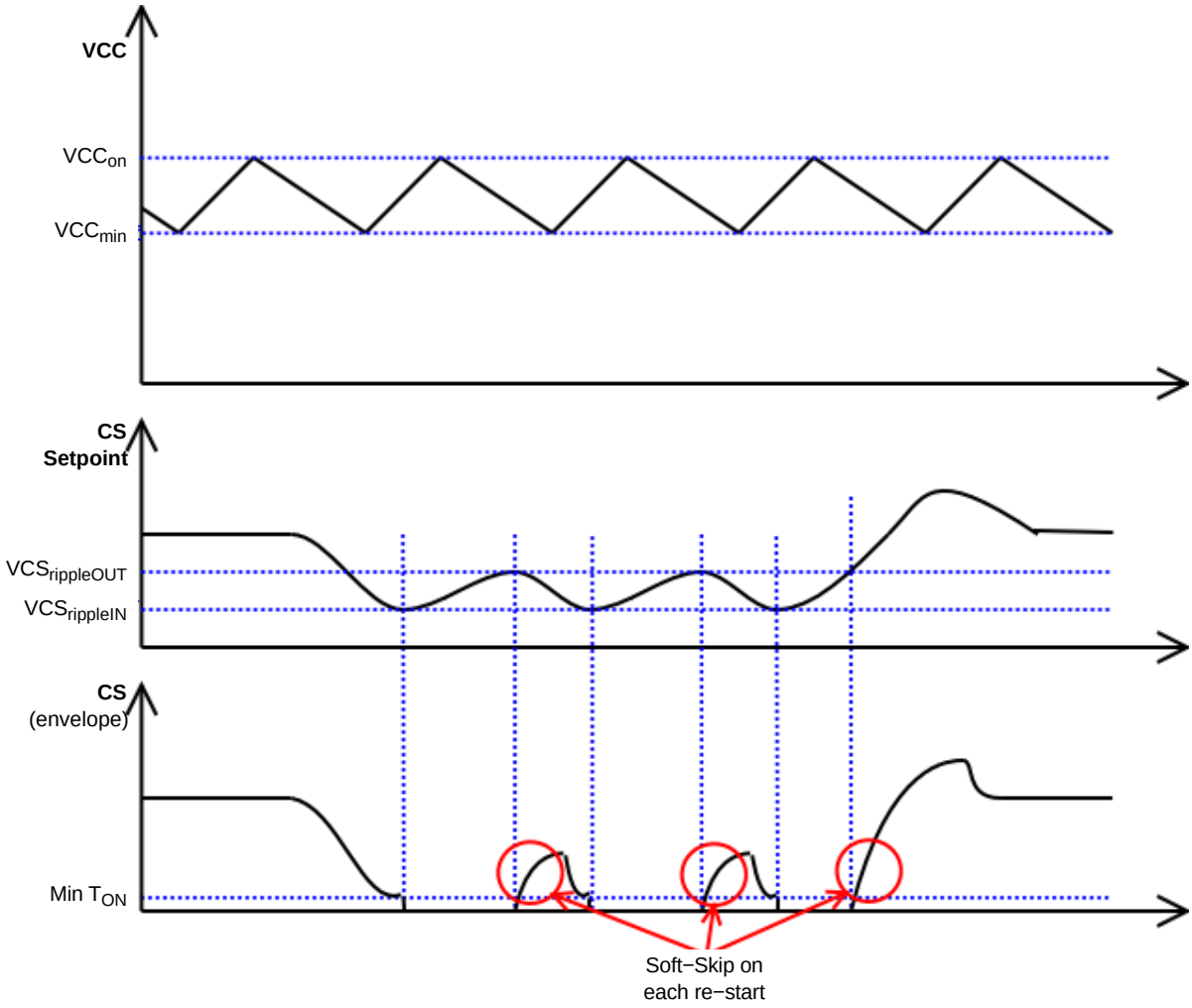


Figure 5. Soft−Skip Mode in Standby

Soxyless

The “Valley point detection” is based on the observation of the Power MOSFET Drain voltage variations. When the transformer is fully demagnetized, the Drain voltage evolution from the plateau level down to the V_{IN} asymptote is governed by the resonating energy transfer between the L_P transformer inductor and the global capacitance present on the Drain. These voltage oscillations create current oscillation in the parasitic capacitor across the switching MOSFET (modelized by the Crss capacitance between Gate and Drain): a negative current (flowing out of DRV pin) takes place during the decreasing part of the Drain oscillation, and a positive current (entering into the DRV pin) during the increasing part.

The Drain valley corresponds to the inversion of the current (i.e., the zero crossing): by detecting this point, we always ensure a true valley turn−on.

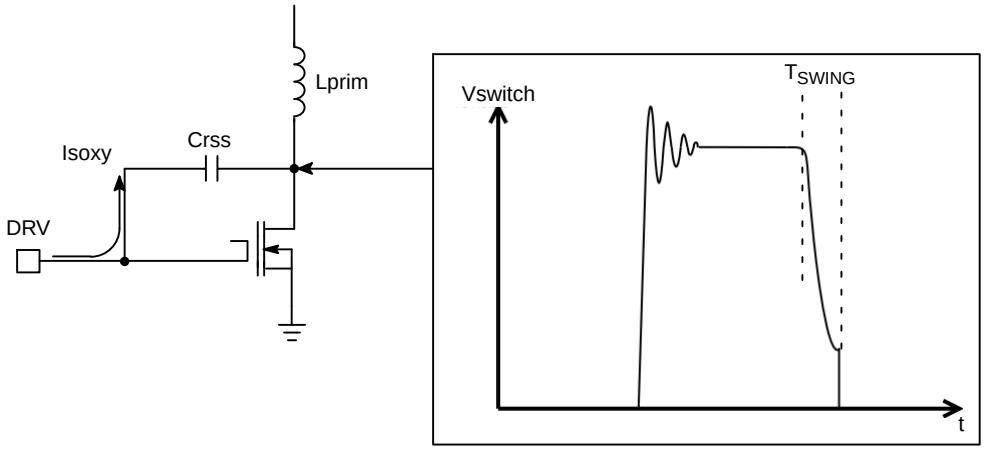


Figure 6. Soxyless Concept

The current in the Power MOSFET gate is:

Igate = Vringing/Zc (with Zc the capacitance impedance) so

Igate = Vringing • (2 • π • Fres • Crss)

The magnitude of this gate current depends on the MOSFET, the resonating frequency and the voltage swing present on the Drain at the end of the plateau voltage.

The dead time T_{SWING} is given by the equation:

$$Tswing = 0.5/Fres = \pi * \sqrt{Lp * Cdrain} \quad \text{(eq. 1)}$$

(where L_P is the primary transformer inductance and C_{DRAIN} the total capacitance present on the MOSFET Drain. This capacitance includes the snubber capacitor if any, the transformer windings stray capacitance plus the parasitic MOSFET capacitances C_{OSS} and C_{RSS}).

Internal Feedback Circuitry

To simplify the implementation of a primary regulation, it is necessary to inject a current into the FB pin (instead of sourcing it out). But to have a precise primary regulation, the voltage present on FB pin must be regulated. Figure 8 gives the FB pin internal implementation: the circuitry combines the functions of a current to voltage converter and a voltage regulator.

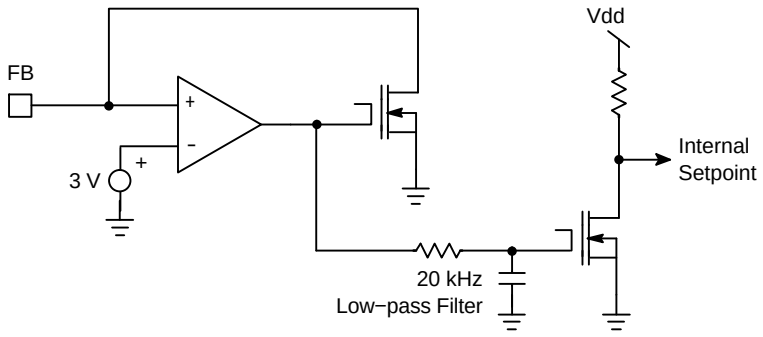


Figure 7. Internal Implementation of FB Pin

The input information is the current injected in FB pin by the feedback loop. The range of current is from 40 μA for overload detection to 220 μA corresponding to $V_{CSrippleIN}$. In transients, currents from 0 to more than 400 μA may also appear: the circuitry is able to sustain them.

To regulate the FB pin voltage, the operational amplifier needs to have a high gain and a wide bandwidth. But the feedback information used internally needs to be filtered, because we don't want the controller to be sensitive to the switching noise. For this purpose, a 20 kHz filter is added after the shunt regulator, and any reading of the feedback signal (for ripple mode, fault detection, or setpoint elaboration) is done after.

Soft Burst Mode (Protection Mode)

The NCP1337 features a fault timer to detect an overload completely independently of the V_{CC} voltage. As soon as the feedback loop asks for the maximum power, a fault is detected, and an internal timer is started. When the fault disappears the timer is reset, but if the timer reaches 80 ms, the protection mode is activated.

Once this protection is toggled, output pulses are stopped and DSS is deactivated (HV current source turn−on threshold changes from VCC_{MIN} to VCC_{LATCH}). V_{CC} slowly decreases (the current consumption is ICC3), and the HV current source is switched ON when V_{CC} reaches VCC_{LATCH}. As a result V_{CC} increases until VCC_{ON}, but the controller does not start as the output is still forced low. V_{CC} decreases again down to VCC_{LATCH}, and a new start−up cycle occurs. On the second attempt, the output is released, and NCP1337 effectively starts, with the soft−start activated. Figure 4 illustrates this behavior.

Safety Features

The NCP1337 includes several safety features to help the power supply designer to build a rugged design:

- OVP (Overvoltage on V_{CC}): Activated when voltage on pin V_{CC} is higher than 18.6 V
- Brown−Out (Undervoltage lockout on bulk voltage): Activated when voltage on pin BO is below 500 mV
- Disable (Comparator activated by an external signal): Activated when the voltage on BO pin is higher than 3.0 V but below 5.0 V
- TSD (Temperature shutdown): Typically activated when the die temperature is above 150°C, released at 120°C

All these events have the same consequence for the controller: the DRV pulses are stopped. When the condition disappears, the controller restarts with the soft−start activated. However, as the fault timer is still active, it can time out while the switching is stopped. As a result the controller will go into protection mode, and won't restart instantaneously.

- Permanent Latch (Comparator activated by an external signal): Activated when the voltage on BO pin is above 5.0 V

When this comparator is activated, the DRV pulses are stopped, and the DSS is deactivated (only the start−up current source is turned on each time V_{CC} reaches VCC_{LATCH}, maintaining V_{CC} between 5.0 V and 12 V): the controller stays in this position until the V_{CC} voltage is decreased below 4.0 V, i.e., when the power supply is unplugged from the mains (in normal operation, as soon as a voltage is present on the HV pin, V_{CC} is always kept above 5.0 V).

Soft−Skip Mode

The soft ripple mode is a skip mode with a large hysteresis on the skip comparator in order to ensure a noise−free and high−efficiency operation in low−load conditions (standby). When internal setpoint is reaching $V_{CSrippleIN}$ = 100 mV (corresponding to 20% of the maximum setpoint), the output pulses are stopped. Then FB loop asks for more power and internal setpoint is increasing: when it reaches $V_{CSrippleOUT}$ = 130 mV (corresponding to 25% of the maximum setpoint), the output starts switching again. Soft−Skip is activated in each activity following a stop period. See Figure 5 for detailed timing diagram.

HV Current Source

NCP1337 features a DSS, to allow operation without any auxiliary voltage. But to protect the die in case of short−circuit on V_{CC} pin, the current delivered by the HV current source is lowered when V_{CC} voltage is below 1.5 V.

In the case the current consumed on the DRV pin is higher than the DSS capability (high Qg MOSFET or failure), the HV current source is switched ON when V_{CC} reaches VCC_{MIN}, but the voltage on V_{CC} pin keep on decreasing. If there is no UVLO threshold to stop the DRV pulses, the gate voltage will become too low and the risk is high to destroy the MOSFET. NCP1337 features an additional comparator, which threshold is 9.0 V: when V_{CC} reaches this level whereas the HV current source is ON, DRV pulses are stopped and the protection mode is activated.

The maximum dV/dt that can be applied to the V_{CC} pin is 9.0 V/ms. The supply capacitor is selected to ensure the maximum dV/dt is not exceeded.

Brown−Out

The brown−out protection comparator has a fixed reference of 500 mV. When the comparator is activated (i.e., when the input voltage V_{IN} is above the starting level), a 10 μA internal current source is activated and creates an offset across the bottom resistor of the external resistor divider. It gives the minimum hysteresis of the brown−out protection. By adding a series resistor between the divider and the BO pin, it is possible to adjust (increase) the hysteresis.

The BO pin also features two additional comparators: the first one (that toggles at 3.0 V) stops the DRV pulses, whereas the second one (that toggles at 5.0 V) permanently latches off the controller (the V_{CC} should be forced below 4.0 V to release the latch).

Figure 8 gives the internal implementation of the BO pin.

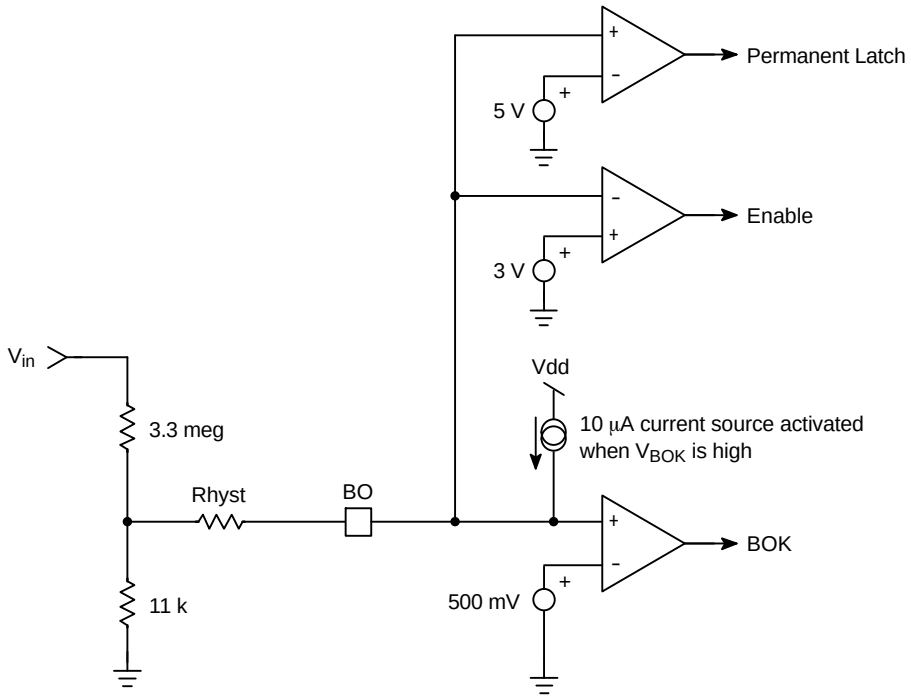


Figure 8. Internal Implementation of BO Pin

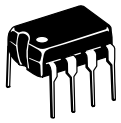
Soft−Skip is a trademark of Semiconductor Components Industries, LLC (SCILLC).

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

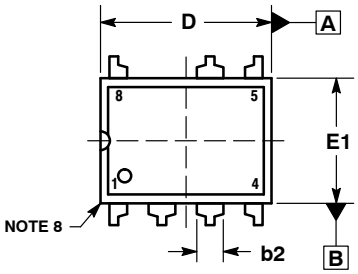
ON Semiconductor®

PDIP−7 (PDIP−8 LESS PIN 7)
CASE 626B
ISSUE D

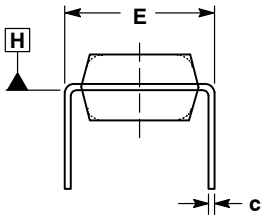
DATE 22 APR 2015



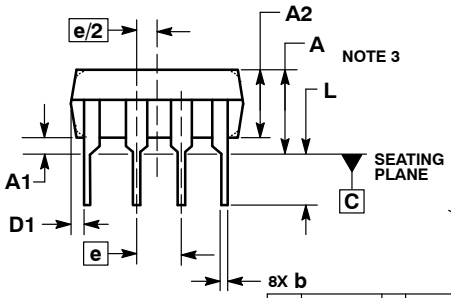
SCALE 1:1



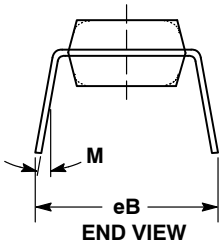
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



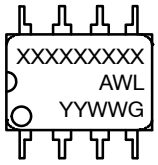
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. NOT USED
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

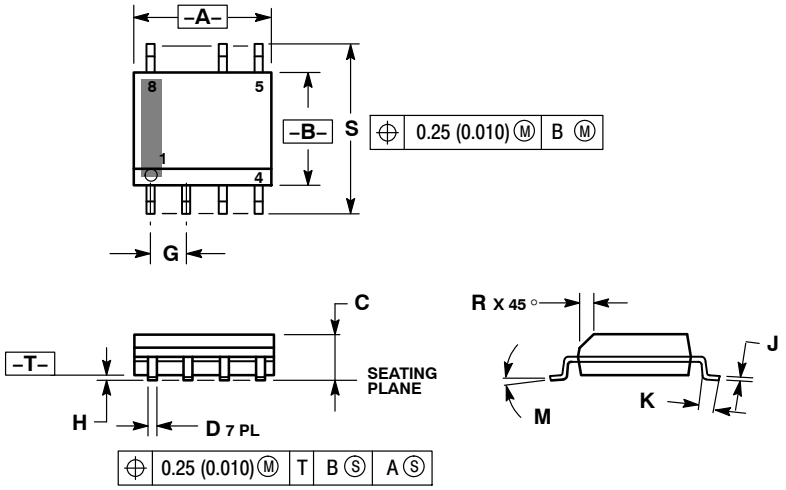
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98AON12198D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PDIP−7 (PDIP−8 LESS PIN 7)	PAGE 1 OF 1

SOIC–7
CASE 751U–01
ISSUE E

DATE 20 OCT 2009

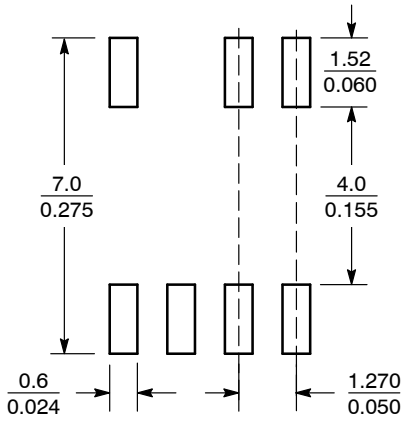
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

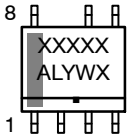
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

SOIC−7
CASE 751U−01
ISSUE E

DATE 20 OCT 2009

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

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