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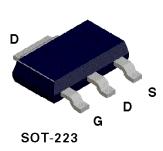
NDT451AN N-Channel Enhancement Mode Field Effect Transistor

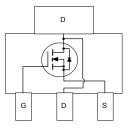
General Description

Features

Power SOT N-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

- 7.2A, 30V. $R_{DS(ON)} = 0.035\Omega @ V_{GS} = 10V$ $R_{DS(ON)} = 0.05\Omega @ V_{GS} = 4.5V.$
- High density cell design for extremely low R_{DS(ON)}.
- High power and current handling capability in a widely used surface mount package.

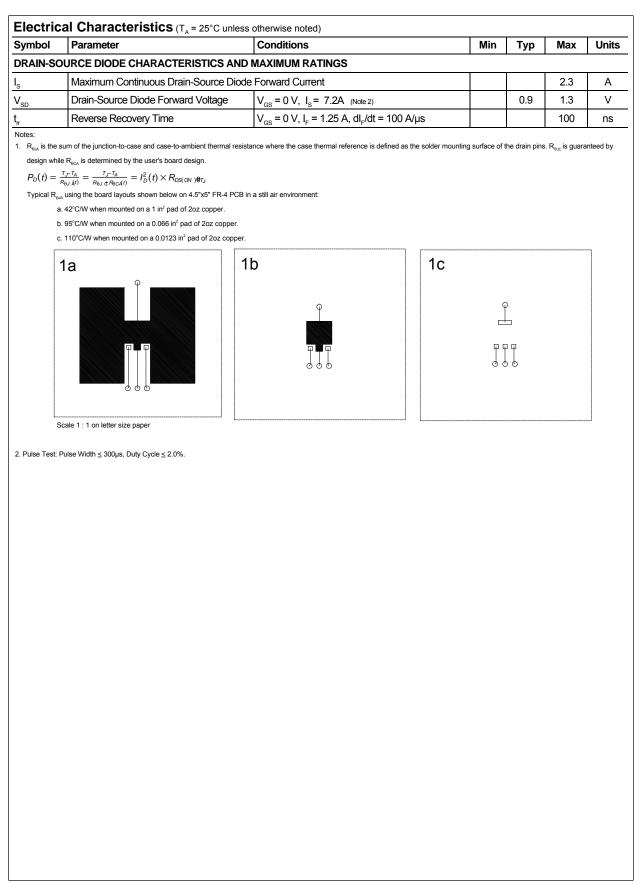


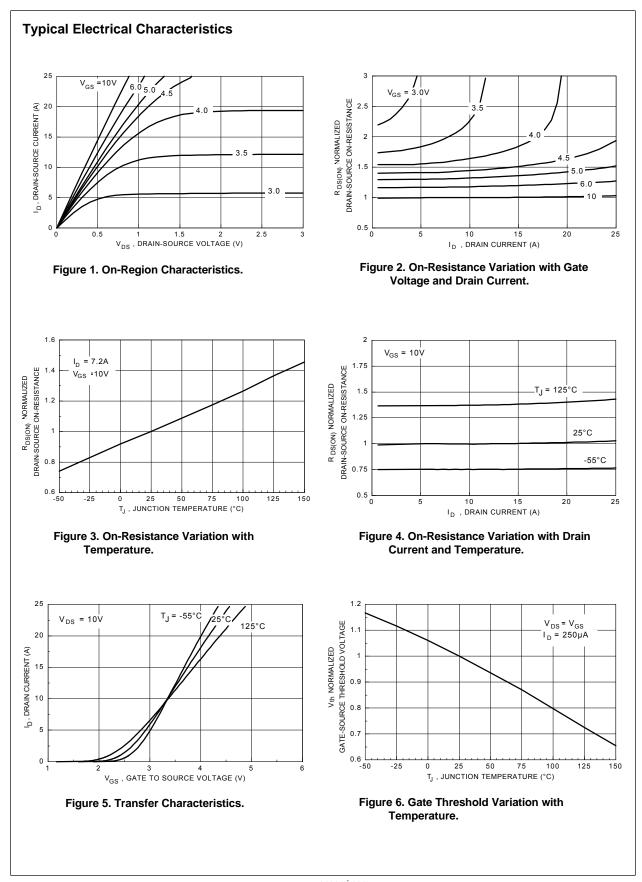


Absolute Maximum Ratings T_A= 25°C unless otherwise noted

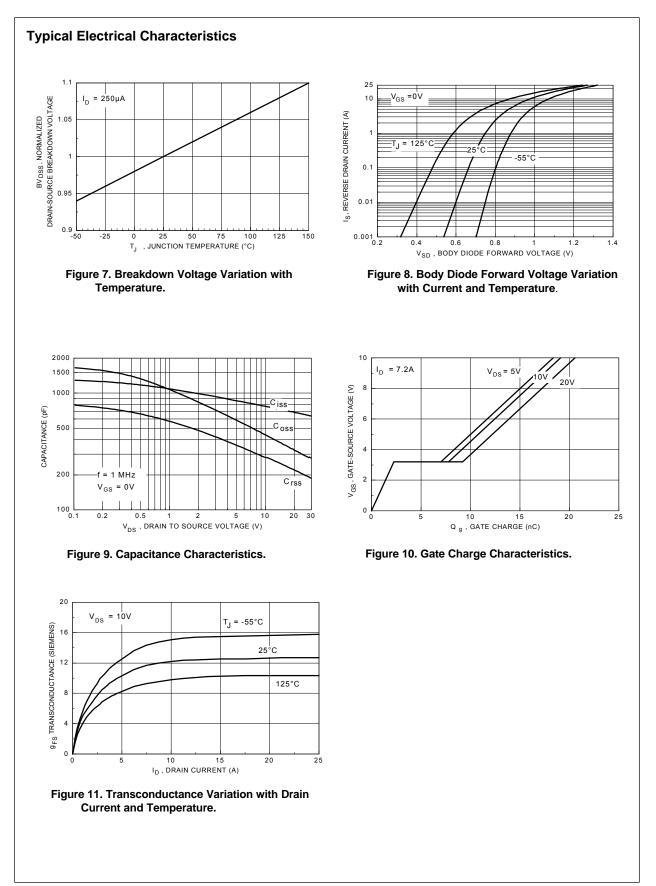
| Symbol | Parameter | | NDT451AN | Units |
|----------------------------------|---|-----------|------------|-------|
| V _{DSS} | Drain-Source Voltage | | 30 | V |
| V _{GSS} | Gate-Source Voltage | | ± 20 | V |
| I _D | Drain Current - Continuous | (Note 1a) | ±7.2 | А |
| | - Pulsed | | ± 25 | |
| P _D | Maximum Power Dissipation | (Note 1a) | 3 | W |
| | | (Note 1b) | 1.3 | |
| | | (Note 1c) | 1.1 | |
| Г _J ,Т _{stg} | Operating and Storage Temperature Range | | -65 to 150 | °C |
| THERMA | L CHARACTERISTICS | | | |
| R _{øja} | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 42 | °C/W |
| ۲ _{өлс} | Thermal Resistance, Junction-to-Case | (Note 1) | 12 | °C/W |

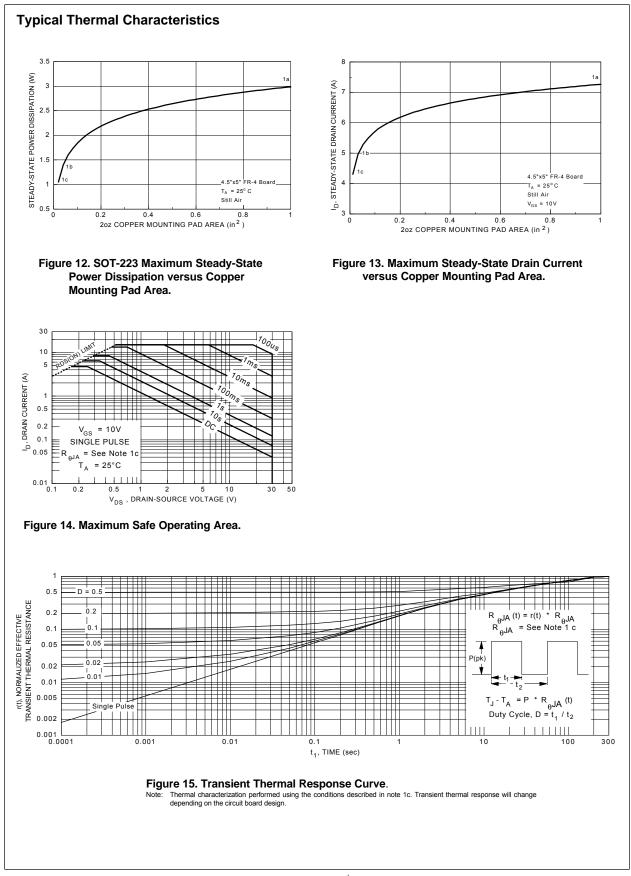
| Symbol | Parameter | Conditions | | Min | Тур | Max | Units |
|---------------------|-----------------------------------|--|------------------------|-----|-------|-------|-------|
| OFF CHA | RACTERISTICS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} = 0 V, I _D = 250 μA | | 30 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 24 V, V _{GS} = 0 V | | | | 1 | μA |
| | | | T_= 55°C | | | 10 | μA |
| | Gate - Body Leakage, Forward | V _{GS} = 20 V, V _{DS} = 0 V | · | | | 100 | nA |
| I _{GSSR} | Gate - Body Leakage, Reverse | V _{GS} = -20 V, V _{DS} = 0 V | | | | -100 | nA |
| ON CHAR | ACTERISTICS (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$ | | 1 | 1.6 | 3 | V |
| | | | T _J = 125°C | 0.7 | 1.2 | 2.2 | |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} = 10 V, I _D = 7.2 A | · | | 0.03 | 0.035 | Ω |
| | | | T _J = 125°C | | 0.042 | 0.063 | |
| | | $V_{GS} = 4.5 \text{ V}, I_{D} = 6.0 \text{ A}$ | · | | 0.042 | 0.05 | |
| | | | T _J = 125°C | | 0.058 | 0.09 | |
| I _{D(on)} | On-State Drain Current | $V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$ | | 25 | | | Α |
| | | $V_{GS} = 4.5 V, V_{DS} = 5 V$ | | 15 | | | |
| 9 _{FS} | Forward Transconductance | $V_{DS} = 10 \text{ V}, \text{ I}_{D} = 7.2 \text{ A}$ | | | 11 | | S |
| DYNAMIC | CHARACTERISTICS | | | | | | |
| C _{iss} | Input Capacitance | $V_{DS} = 15 V, V_{GS} = 0 V,$ f = 1.0 MHz | | | 720 | | pF |
| C _{oss} | Output Capacitance | | | | 370 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | | 250 | | pF |
| SWITCHI | IG CHARACTERISTICS (Note 2) | | | | | | |
| t D(on) | Turn - On Delay Time | $V_{DD} = 10 \text{ V}, \text{ I}_{D} = 1 \text{ A},$ $V_{GEN} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ | | | 12 | 20 | ns |
| ţ | Turn - On Rise Time | | | | 13 | 30 | ns |
| L _{D(off)} | Turn - Off Delay Time | | | | 29 | 50 | ns |
| ł | Turn - Off Fall Time | | | | 10 | 20 | ns |
| Q | Total Gate Charge | $V_{DS} = 10 \text{ V},$ $I_{D} = 7.2 \text{ A}, \text{ V}_{GS} = 10 \text{ V}$ | | | 19 | 30 | nC |
| Q_{gs} | Gate-Source Charge | | | | 2.3 | | nC |
| Q _{gd} | Gate-Drain Charge | | | | 5.5 | | nC |





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