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# CM2021-02TR

# HDMI Receiver Port Protection and Interface Device

## Product Description

The CM2021-02TR HDMI Receiver Port Protection and Interface Device is specifically designed for next generation HDMI Host interface protection.

An integrated package provides all ESD, level shift and backdrive protection for an HDMI port in a single 38−Pin TSSOP package.

The CM2021−02TR part is specifically designed to complement the CM2020 protection part in HDMI transmitters (DVD, STB/OPVR, etc.).

## Features

- HDMI 1.3 Compliant
- 0.05 pF Matching Capacitance between the TMDS Intra−Pair
- Level Shifting/Isolation Circuitry
- Provides ESD Protection to IEC61000−4−2 Level 4:
  - ±8 kV Contact Discharge
  - ±15 kV Air Discharge
- Matched 0.5 mm Trace Spacing (TSSOP)
- Simplified Layout for HDMI Connectors
- Backdrive Protection
- These Devices are Pb−Free and are RoHS Compliant

## Applications

- PC
- Consumer Electronics
- Displays and Digital Television

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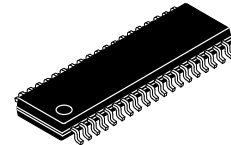


**TSSOP 38**
**TR SUFFIX**
**CASE 948AG**

### MARKING DIAGRAM

CM2021−02TR

CM2021−02TR = Specific Device Code

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| CM2021−02TR | TSSOP−38 (Pb−Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# CM2021−02TR

## ELECTRICAL SCHEMATIC



## PACKAGE / PINOUT DIAGRAM

Top View

| | Pin | | Pin | |
|---|---|---|---|---|
| 5V_SUPPLY | 1 | | 38 | NC |
| LV_SUPPLY | 2 | | 37 | ESD_BYP |
| GND | 3 | | 36 | GND |
| TMDS_D2+ | 4 | | 35 | TMDS_D2+ |
| TMDS_GND | 5 | | 34 | TMDS_GND |
| TMDS_D2− | 6 | | 33 | TMDS_D2− |
| TMDS_D1+ | 7 | | 32 | TMDS_D1+ |
| TMDS_GND | 8 | | 31 | TMDS_GND |
| TMDS_D1− | 9 | | 30 | TMDS_D1− |
| TMDS_D0+ | 10 | | 29 | TMDS_D0+ |
| TMDS_GND | 11 | | 28 | TMDS_GND |
| TMDS_D0− | 12 | | 27 | TMDS_D0− |
| TMDS_CK+ | 13 | | 26 | TMDS_CK+ |
| TMDS_GND | 14 | | 25 | TMDS_GND |
| TMDS_CK− | 15 | | 24 | TMDS_CK− |
| CE_REMOTE_IN | 16 | | 23 | CE_REMOTE_OUT |
| DDC_CLK_IN | 17 | | 22 | DDC_CLK_OUT |
| DDC_DAT_IN | 18 | | 21 | DDC_DAT_OUT |
| HOTPLUG_DET_IN | 19 | | 20 | HOTPLUG_DET_OUT |

38−Pin TSSOP Package

# CM2021−02TR

**Table 1. PIN DESCRIPTIONS**

| Pins | Name | ESD Level | Description |
|---|---|---|---|
| 4, 35 | TMDS_D2+ | 8 kV (Note 2) | TMDS 0.9 pF ESD Protection (Note 1) |
| 6, 33 | TMDS_D2− | 8 kV (Note 2) | TMDS 0.9 pF ESD Protection (Note 1) |
| 7, 32 | TMDS_D1+ | 8 kV (Note 2) | TMDS 0.9 pF ESD Protection (Note 1) |
| 9, 30 | TMDS_D1− | 8 kV (Note 2) | TMDS 0.9 pF ESD Protection (Note 1) |
| 10, 29 | TMDS_D0+ | 8 kV (Note 2) | TMDS 0.9 pF ESD Protection (Note 1) |
| 12, 27 | TMDS_D0− | 8 kV (Note 2) | TMDS 0.9 pF ESD Protection (Note 1) |
| 13, 26 | TMDS_CK+ | 8 kV (Note 2) | TMDS 0.9 pF ESD Protection (Note 1) |
| 15, 24 | TMDS_CK− | 8 kV (Note 2) | TMDS 0.9 pF ESD Protection (Note 1) |
| 16 | CE_REMOTE_IN | 2 kV (Note 3) | LV_SUPPLY Referenced Logic Level into ASIC |
| 23 | CE_REMOTE_OUT | 8 kV(Note 2) | 5V_SUPPLY Referenced Logic Level Out plus 3.5 pF ESD to Connector |
| 17 | DDC_CLK_IN | 2 kV (Note 3) | LV_SUPPLY Referenced Logic Level into ASIC |
| 22 | DDC_CLK_OUT | 8 kV (Note 2) | 5V_SUPPLY Referenced Logic Level Out plus 3.5 pF ESD to Connector |
| 18 | DDC_DAT_IN | 2 kV (Note 3) | LV_SUPPLY Referenced Logic Level into ASIC |
| 21 | DDC_DAT_OUT | 8 kV (Note 2) | 5V_SUPPLY Referenced Logic Level Out plus 3.5 pF ESD to Connector |
| 19 | HOTPLUG_DET_IN | 2 kV (Note 3) | LV_SUPPLY Referenced Logic Level into ASIC |
| 20 | HOTPLUG_DET_OUT | 8 kV (Note 2) | 5V_SUPPLY Referenced Logic Level Out plus 3.5 pF ESD to Connector |
| 2 | LV_SUPPLY | 2 kV (Note 3) | Bias for CE / DDC / HOTPLUG Level Shifters |
| 1 | 5V_SUPPLY | 2 kV (Note 3) | Current Source for 5V_OUT |
| 37 | ESD_BYP | 2 kV (Note 3) | This Pin may be Connected to a 0.1 μF Ceramic Capacitor, but it is not necessary. |
| 5, 34, 8, 31, 11, 28, 14, 25 | TMDS_GND | N/A | TMDS ESD and Parasitic GND Return (Note 4) |
| 3, 36 | GND | N/A | Supply GND Reference |
| 38 | NC | N/A | No Connect |

1. These 2 pins need to be connected together in−line on the PCB.
2. Standard IEC 61000−4−2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, each bypassed with a 0.1 μF ceramic capacitor connected to GND.
3. Human Body Model per MIL−STD−883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, and each bypassed with a 0.1 μF ceramic capacitor connected to GND.
4. These pins should be routed directly to the associated GND pins on the HDMI connector with single point ground vias at the connector.

## BACKDRIVE PROTECTION

Two scenarios below describe what can happen when a powered device is connected to an unpowered device via an HDMI interface, substantiating the need for backdrive protection for this type of interface.

In a classic scenario, a DVD player is connected to a TV via an HDMI interface. If the DVD player is switched off and the TV is left on, there is a possibility of reverse current flow back into the main power supply rail of the DVD player. Typically, the DVD's power supply has some form of bulk supply capacitance associated with it. Because all CMOS logic exhibits a very high impedance on the power rail node when "off," if there is very little parasitic shunt resistance and as little as a few milliamps of "backdrive" current flowing back into the power rail, it is possible over time to charge that bulk supply capacitance to some intermediate level. If this level rises above the power-on-reset (POR) voltage level of some of the integrated circuits in the DVD player, these devices may not reset properly when the DVD player is turned back on.

In a more serious scenario, if any SOC devices are incorporated in the design which have built-in level shifter and DRC diodes for ESD protection, there is even a higher risk for damage. In this case, if there is a pullup resistor (such as with DDC) on the other end of the cable, that resistance will pull the SOC chips "output" up to a high level. This will forward bias the upper ESD diode in the DRC and charge the bulk capacitance in a similar fashion like above. If the current flow is high enough, even as little as a few milliamps, it could destroy one of the SOC chip's internal DRC diodes, as they are not designed for passing DC.

To avoid either of these situations, the CM2021-02TR is designed to block backdrive current, guaranteeing no more than 5 μA on any I/O pin when the I/O pin voltage is greater than the CM2021-02TR supply voltage.
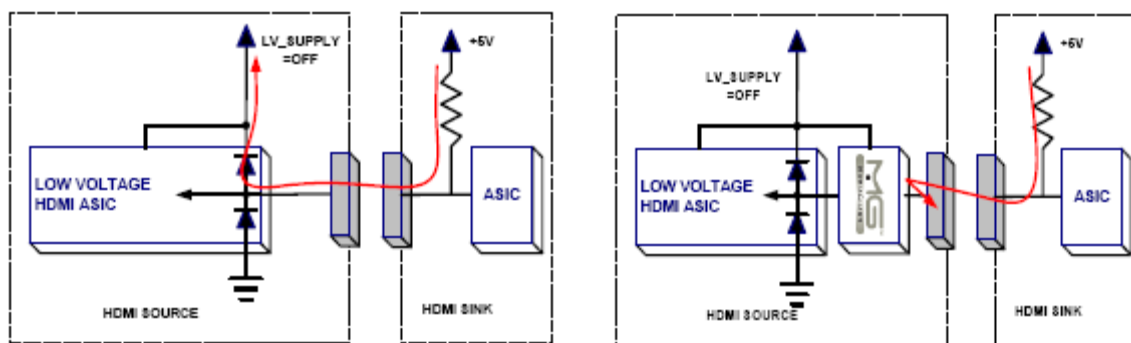


Figure 1. Backdrive Protection Diagram.

## SPECIFICATIONS

### Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Units |
|---|---|---|
| $V_{CC5V}$, $V_{CCLV}$ | 6.0 | V |
| DC Voltage at any Channel Input | 6.0 | V |
| Storage Temperature Range | −65 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### Table 3. STANDARD (RECOMMENDED) OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| 5V_SUPPLY | Operating Supply Voltage | GND | 5 | 5.5 | V |
| LV_SUPPLY | Bias Supply Voltage | 1 | 3.3 | 5.5 | V |
| − | Operating Temperature Range | −40 | − | 85 | °C |

## SPECIFICATIONS (Cont'd)

### Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC5V}$ | Operating Supply Current | 5V_SUPPLY = 5.0 V | | 110 | 130 | μA |
| $I_{CCLV}$ | Bias Supply Current | LV_SUPPLY = 3.3 V | | 1 | 5 | μA |
| $I_{OFF}$ | OFF State Leakage Current, Level Shifting NFET | LV_SUPPLY = 0 V | | 0.1 | 5.0 | μA |
| $I_{BACKDRIVE}$ | Current Conducted from Output Pins to V_SUPPLY Rails when Powered Down | 5V_SUPPLY < $V_{CH\_OUT}$ Signal Pins: TMDS_D[2:0]+/−, TMDS_CK+/−, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT Only | | 0.1 | 5.0 | μA |
| $I_{BACKDRIVE, CEC}$ | Current through CE−REMOTE_OUT when Powered Down | CE−REMOTE_IN = CE_SUPPLY < CE_REMOTE_OUT | | 0.1 | 1.0 | μA |
| $V_{ON}$ | VOLTAGE Drop Across Level Shifting NFET when ON | LV_SUPPLY = 2.5 V, $V_S$ = GND, $I_{DS}$ = 3 mA | 75 | 95 | 140 | mV |
| $V_F$ | Diode Forward Voltage<br>Top Diode<br>Bottom Diode | $I_F$ = 8 mA, $T_A$ = 25°C<br>(Note 2) | 0.60<br>0.60 | 0.85<br>0.85 | 0.95<br>0.95 | V |
| $V_{ESD}$ | ESD Withstand Voltage (IEC) | Pins 4, 7, 10, 13, 20, 21, 22, 23, 24, 27, 30, 33 (Notes 2 and 3) | 8 | | | kV |
| $V_{CL}$ | Channel Clamp Voltage<br>Positive Transients<br>Negative Transients | $T_A$ = 25°C, $I_{PP}$ = 1 A, $t_P$ = 8/20 μs<br>(Notes 2 and 4) | | 11.0<br>−2.0 | | V |
| $R_{DYN}$ | Dynamic Resistance<br>Positive Transients<br>Negative Transients | $T_A$ = 25°C, $I_{PP}$ = 1 A, $t_P$ = 8/20 μs<br>(Notes 2 and 4) | | 1.2<br>0.9 | | Ω |
| $I_{LEAK}$ | TMDS Channel Leakage Current | $T_A$ = 25°C (Note 2) | | 0.01 | 1 | μA |
| $C_{IN, TMDS}$ | TMDS Channel Input Capacitance | 5V_SUPPLY = 5.0 V, Measured at 1 MHz, $V_{BIAS}$ = 2.5 V (Note 2) | | 0.9 | 1.2 | pF |
| $\Delta C_{IN, TMDS}$ | TMDS Channel Input Capacitance Matching | 5V_SUPPLY = 5.0 V, Measured at 1 MHz, $V_{BIAS}$ = 2.5 V (Note 2 and 5) | | 0.05 | | pF |
| $C_{IN, DDC}$ | Level Shifting Input Capacitance, Capacitance to GND | 5V_SUPPLY = 5 V, Measured at 100 kHz, $V_{BIAS}$ = 2.5 V (Note 2) | | 3.5 | 4 | pF |
| $C_{IN, CEC}$ | Level Shifting Input Capacitance, Capacitance to GND | 5V_SUPPLY = 5 V, Measured at 100 kHz, $V_{BIAS}$ = 2.5 V (Note 2) | | 3.5 | 4 | pF |
| $C_{IN, HP}$ | Level Shifting Input Capacitance, Capacitance to GND | 5V_SUPPLY = 5 V, Measured at 100 kHz, $V_{BIAS}$ = 2.5 V (Note 2) | | 3.5 | 4 | pF |

1. Operating Characteristics are over Standard Operating Conditions unless otherwise specified.
2. This parameter is guaranteed by design and verified by device characterization.
3. Standard IEC 61000−4−2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, each bypassed with a 0.1 μF ceramic capacitor connected to GND.
4. These measurements performed with no external capacitor on ESD_BYP.
5. Intra−pair matching, each TMDS pair (i.e. D+, D−).

## PERFORMANCE INFORMATION

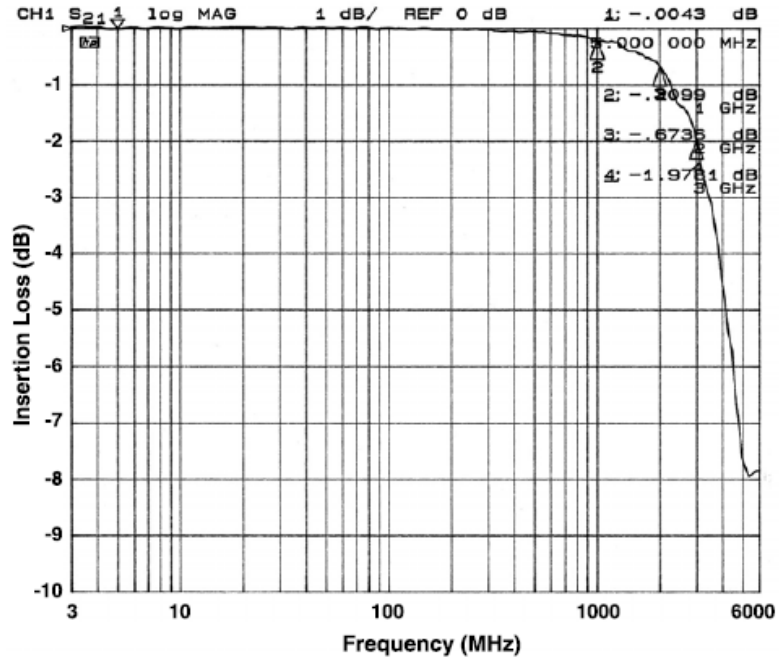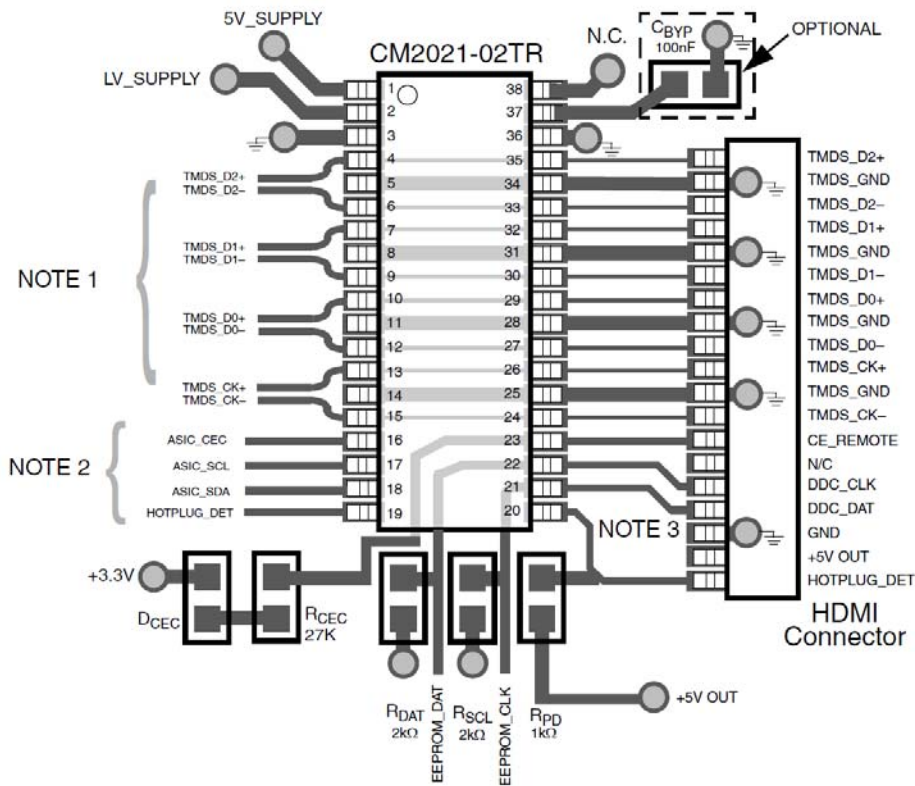**Typical Filter Performance (T$_A$ = 25°C, DC Bias = 0 V, 50 Ω Environment)**



**Figure 2. Insertion Loss vs. Frequency (TMDS_D1− to GND)**

## APPLICATION INFORMATION



**Figure 3. Typical Application for CM2021−02TR**

LAYOUT NOTES

NOTE 1) Differential TMDS Pairs should be designed as normal 100 Ω HDMI microstrip. Single Ended TMDS traces underneath CM2021 and between CM2021 and Connector should be tuned to match chip/connector parasitics. (See MediaGuard™ Application Notes.)

NOTE 2) Level Shifter signals should be biased with a weak pullup to the desired local LV_SUPPLY. If the local ASIC includes sufficient pullups to register a logic high when the CM2021 NFET is "off", then external pullups are not needed.

NOTE 3) Place CM2021 as close to conector as possible, and as with any controlled impedance line avoid ANY silkscreening over TMDS lines.

## APPLICATION INFORMATION (Cont'd)

### Design Considerations

#### DUT On vs. DUT Off

Many HDMI CTS tests require a power off condition on the System Under Test. Many Dual Rail Clamp (DRC) ESD diode configurations will be forward biased when their VDD rail is lower than the I/O pin bias, thereby exhibiting extremely high apparent capacitance measurements, for example. The *MediaGuard*™ backdrive isolation circuitry limits this current to less than 10 μA, and will help ensure compliance.

#### EEPROM Configurations

The EDID EEPROM may be connected to either the ASIC LV domain or Connector 5 V domain of the CM2021. See the MediaGuard EEPROM Application Note for further circuit connection and layout examples.
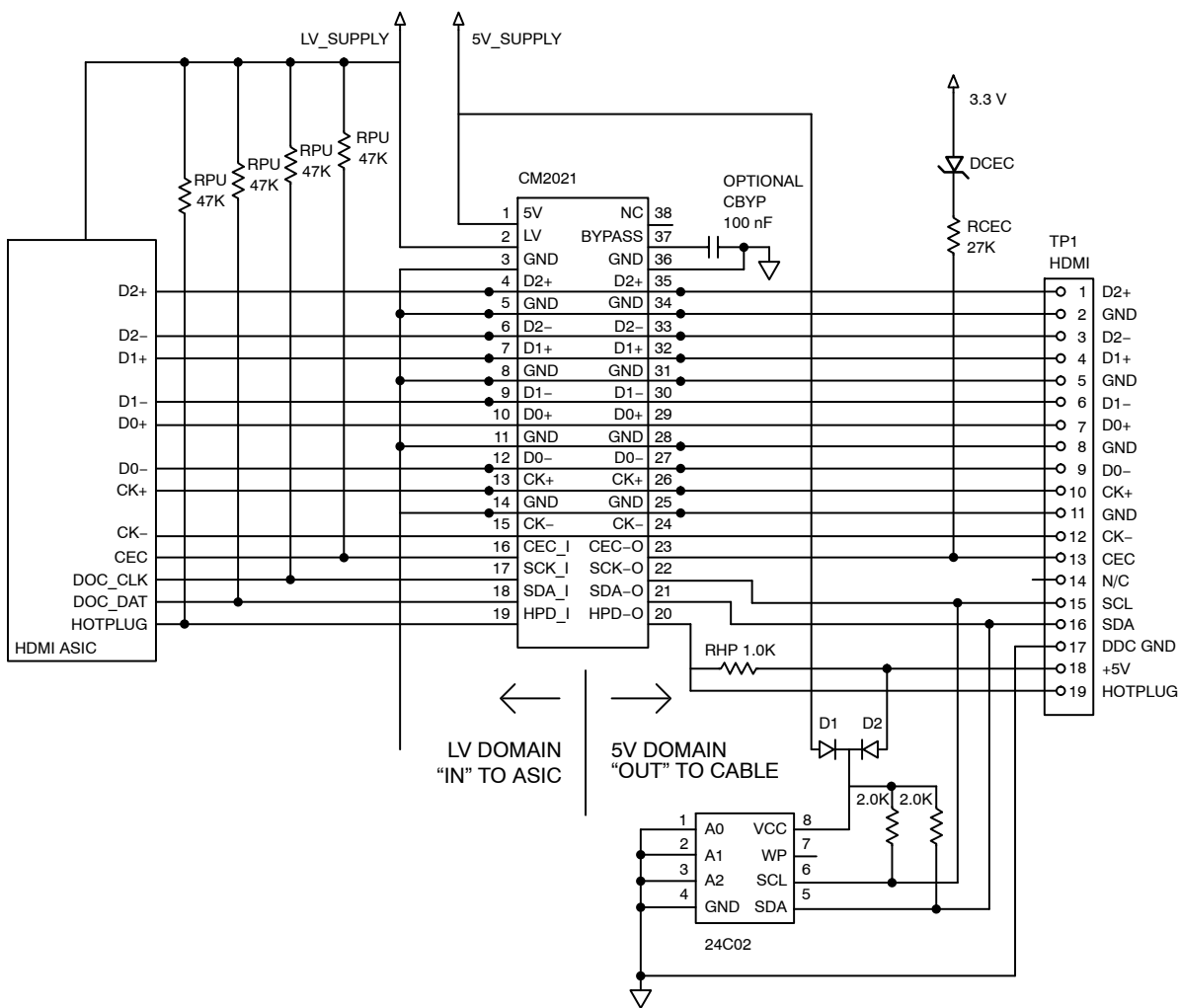
**Figure 4. Design Example**

# CM2021−02TR

## PACKAGE DIMENSIONS

**TSSOP 38**
CASE 948AG−01
ISSUE O



9.70 [.382] ±0.10 [.004]

1.00 [.040] TYP

38    20

6.40 [.252] ±0.200 [.008 ]

4.40 [.173] ±0.10 [.004]

1.00 [.040] TYP

1    19

PIN#1 Ident
ø0.75 [.0295]TYP

0.50 [.0197] BSC

1.20 [.047] MAX

12° TYP

DETAIL A

0.90 [.0354] +0.15 [.006] −0.10 [.004]

0.15 [.006] MAX
0.05 [.002] MIN

0.20[.008] 0.09[.0035]

0.27[.011]
0.17[.0067]

Base Mat'l

0.23[.009]
0.17[.0067]

0.16[.006] 0.09[.0035]

0.08 [.003]
0.00 [.000]

0.025 [.001] MAX

DETAIL A

R0.15 [.006] TYP

R0.102 [.004] MIN

R0.204 [.008] MIN

GAGE PLANE

0.15 [.006] MIN

0.25 [.010]

0°−8°

0.60[.024]±0.15[.006]

1.00 [.040] REF

**Notes :**
1. Datums −A− and −B− to be determined at Datum Plane −H− .
2. Package dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
3. Controlling dimension in mm.
4. Refer to JEDEC MO−153 rev. E for dimensions not shown.

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