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BUL42D

High Speed, High Gain Bipolar NPN Transistor Integrating an Antisaturation Network and a Transient Voltage Suppression Capability

The BUL42D is a state−of−the−art bipolar transistor. Tight dynamic characteristics and lot to lot minimum spread make it ideally suitable for light ballast applications.

Main Features:

- Free Wheeling Diode Built In
- Flat DC Current Gain
- Fast Switching Times and Tight Distribution
- "Six Sigma" Process Providing Tight and Reproducible Parameter Spreads

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter−Base Voltage	V_{EBO}	9	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	4.0 8.0	Adc
Base Current − Continuous − Peak (Note 1)	I_B I_{BM}	1.0 2.0	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to +150	°C

TYPICAL GAIN

Typical Gain @ I_C = 1 A, V_{CE} = 2 V	h_{FE}	13	−
Typical Gain @ I_C = 0.3 A, V_{CE} = 1 V	h_{FE}	16	−

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance − Junction−to−Case	$R_{\theta JC}$	1.66	°C/W
Thermal Resistance − Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 seconds	T_L	260	°C

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%

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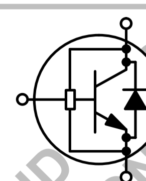
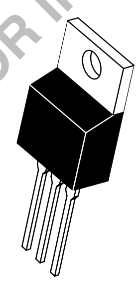
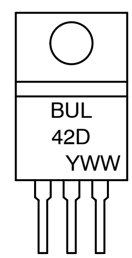
4 AMPERES
700 VOLTS, 75 WATTS
POWER TRANSISTOR





TO−220
CASE 221A
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
BUL42D	TO−220	50 Units/Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	430	–	Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	780	–	Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	9.0	12	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CEO}	– –	– –	100 200	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}	– –	– –	10 200	μAdc
Emitter−Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS						
Base−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{BE(sat)}$	–	0.85	1.2	Vdc
Collector−Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	–	0.2	1.0	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 2 Vdc) (I_C = 2 Adc, V_{CE} = 5 Vdc)		h_{FE}	 8.0 10	 13 12	 – –	–
DIODE CHARACTERISTICS						
Forward Diode Voltage (I_{EC} = 1.0 Adc)		V_{EC}	–	0.9	1.5	V
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)						
Turn−Off Time (I_C = 1.2 Adc, I_{B1} = 0.4 A, I_{B2} = 0.1 A, V_{CC} = 300 V)		T_{off}	4.6	–	6.55	μs
Fall Time (I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 A, V_{CC} = 150 V, V_{BE} = −2 V)		T_f	–	–	0.8	μs

DYNAMIC SATURATION VOLTAGE

Characteristic	Conditions	Time	Temperature	Symbol	Min	Typ	Max	Unit
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 400 mA, I_{B1} = 40 mA, V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$	– –	2.8 3.2	– –	V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		– –	0.75 1.3	– –	
	I_C = 1 A, I_{B1} = 200 mA, V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C		– –	2.1 4.7	– –	
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		– –	0.35 0.6	– –	

TYPICAL STATIC CHARACTERISTICS

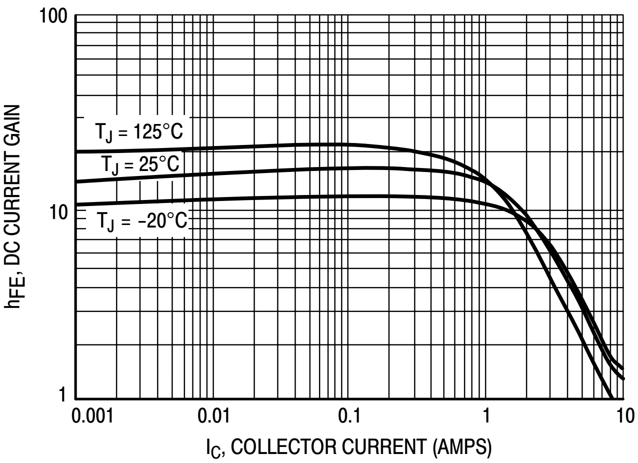


Figure 1. DC Current Gain @ V_{CE} = 1 V

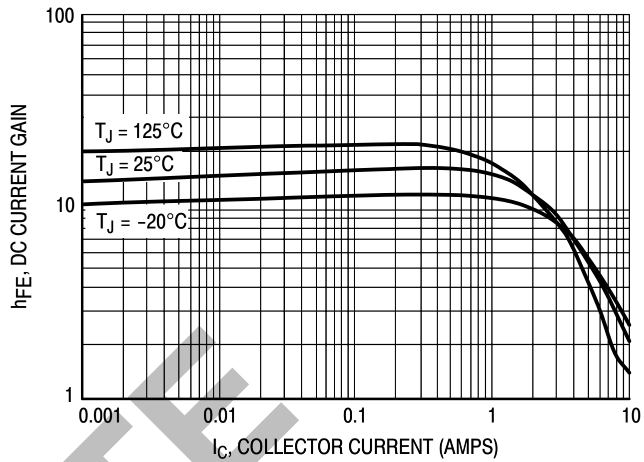


Figure 2. DC Current Gain @ V_{CE} = 5 V

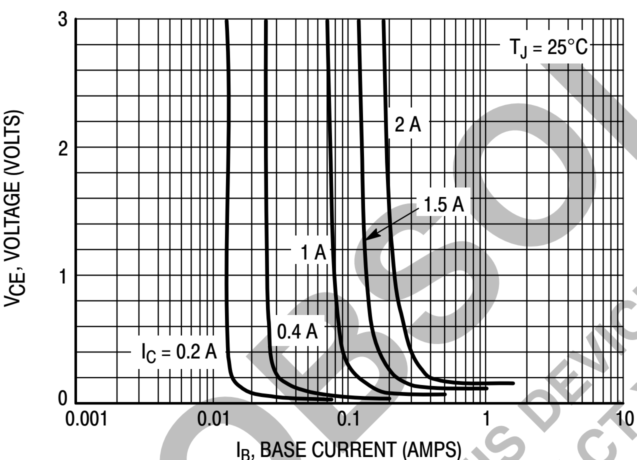


Figure 3. Collector Saturation Region

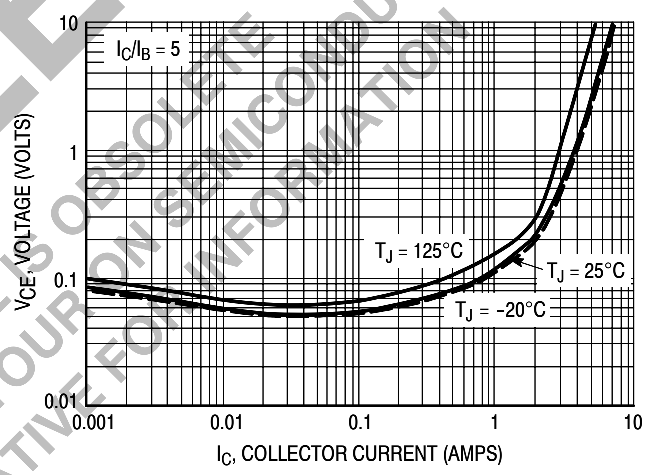


Figure 4. Collector−Emitter Saturation Voltage

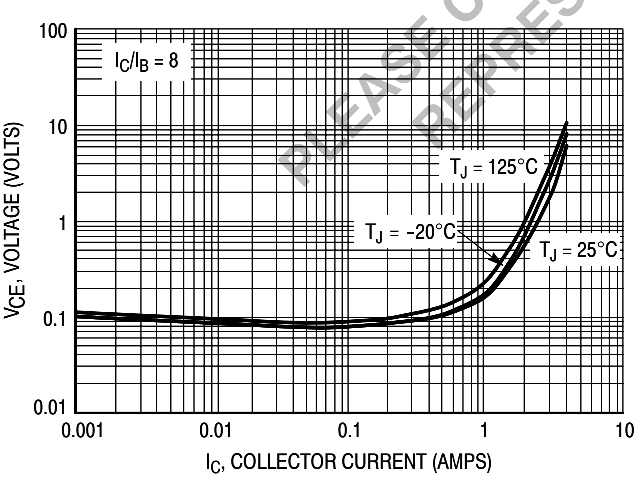


Figure 5. Collector−Emitter Saturation Voltage

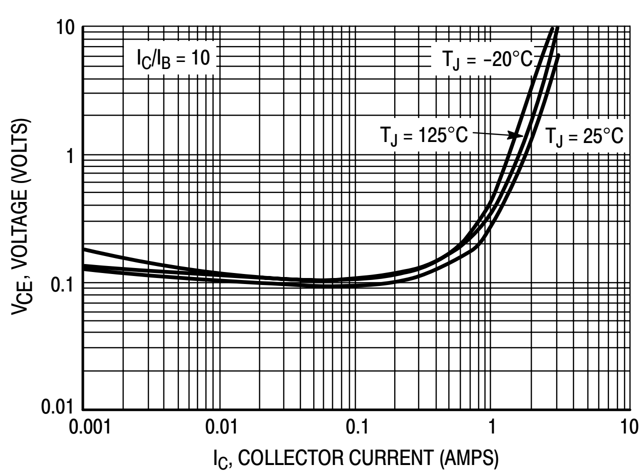


Figure 6. Collector−Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

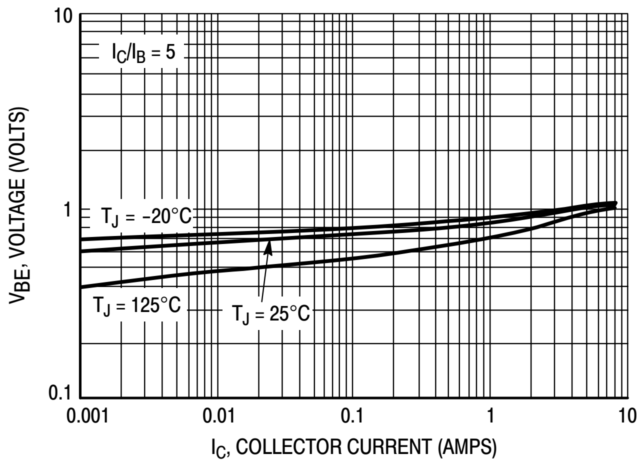


Figure 7. Base−Emitter Saturation Region

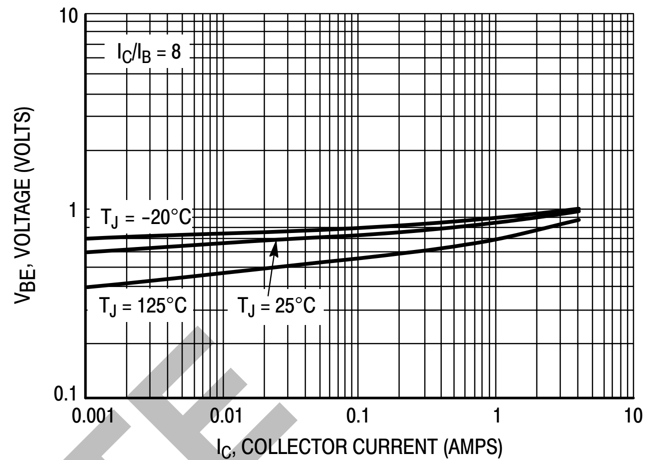


Figure 8. Base−Emitter Saturation Region

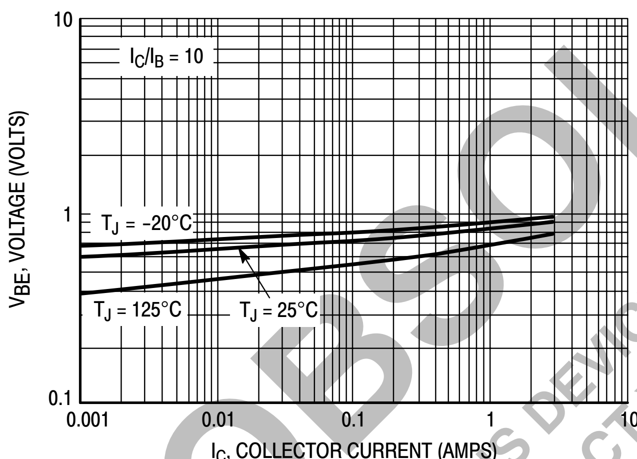


Figure 9. Base−Emitter Saturation Region

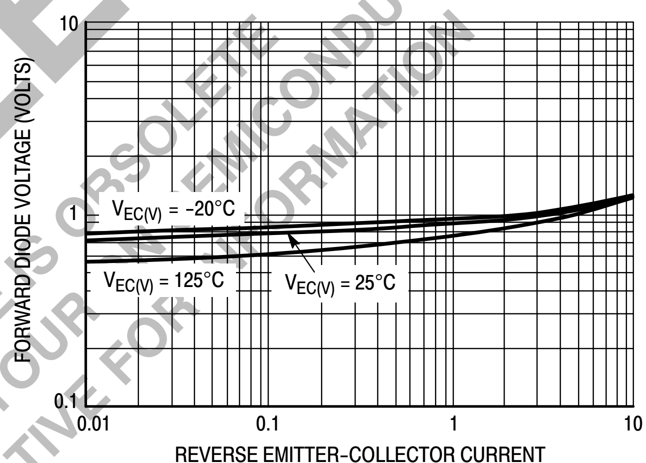


Figure 10. Forward Diode Voltage

TYPICAL SWITCHING CHARACTERISTICS

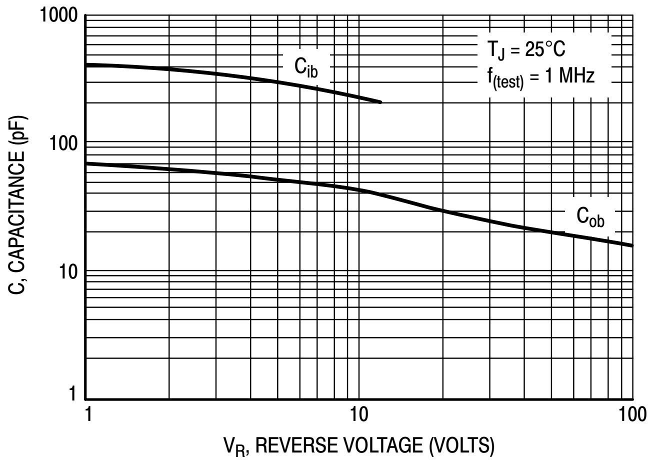


Figure 11. Capacitance

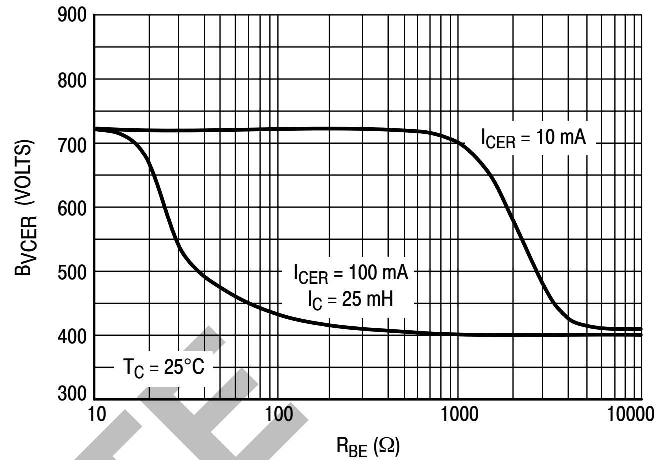


Figure 12. B_{VCER} = f(R_{BE})

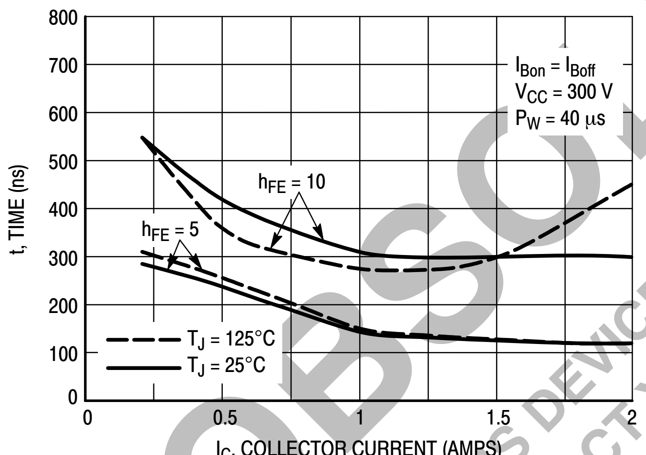


Figure 13. Resistive Switching, t_{on}

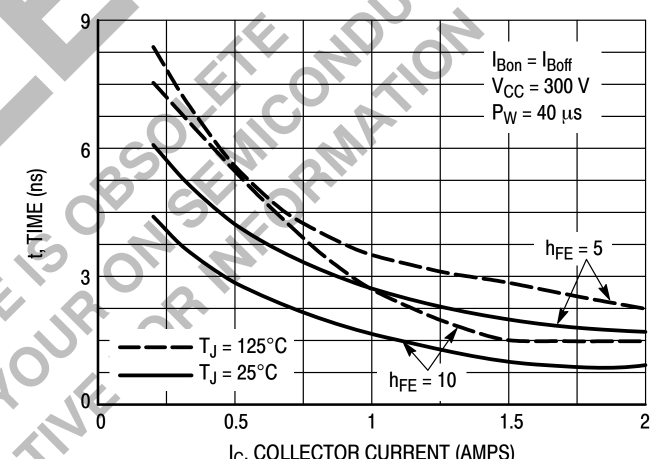


Figure 14. Resistive Switching, t_{off}

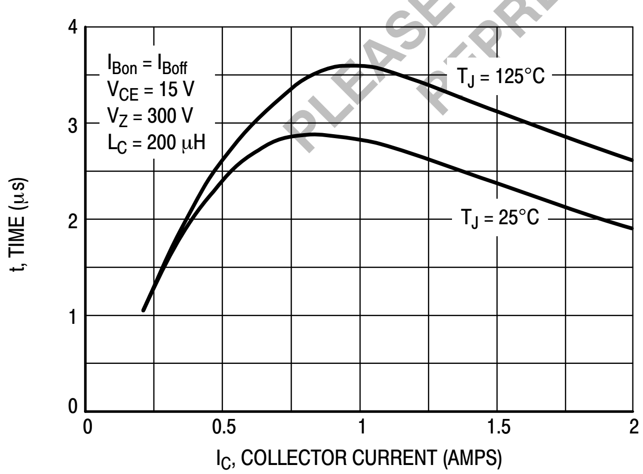


Figure 15. Inductive Storage Time, t_{si} @ h_{FE} = 5

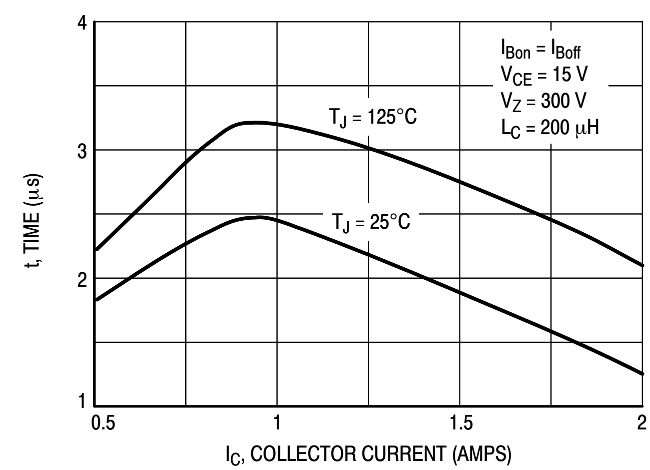


Figure 16. Inductive Storage Time, t_{si} @ h_{FE} = 10

TYPICAL SWITCHING CHARACTERISTICS

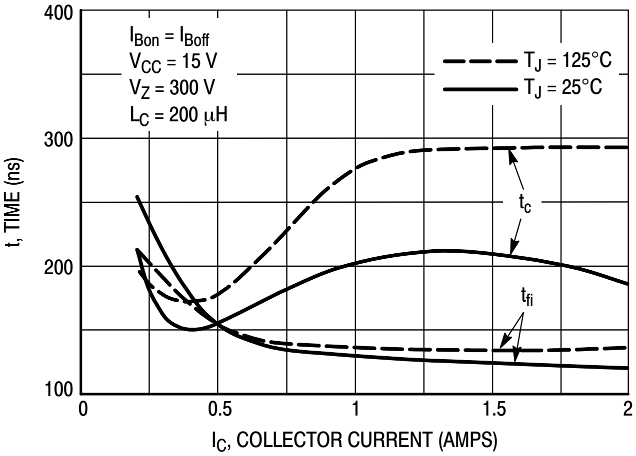


Figure 17. Inductive Fall and Cross Over Time, t_{fi} and t_c @ h_{FE} = 5

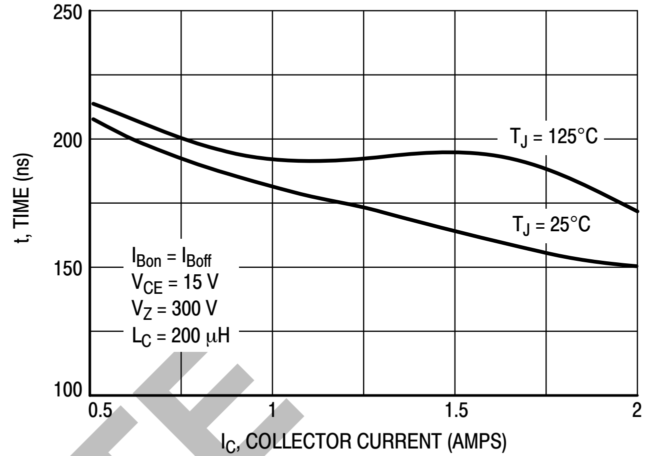


Figure 18. Inductive Fall Time, t_{fi} @ h_{FE} = 10

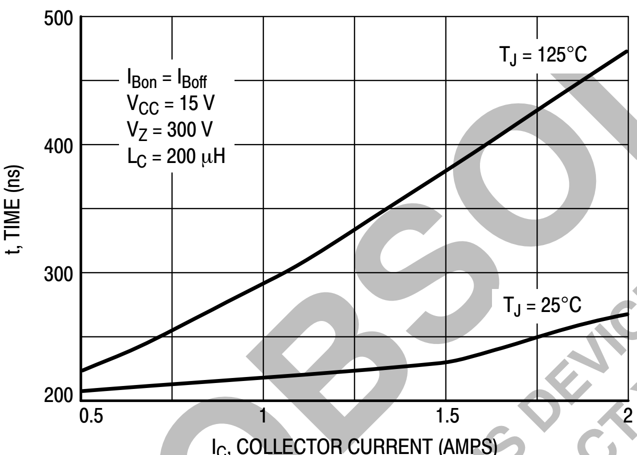


Figure 19. Inductive Cross Over Time, t_c @ h_{FE} = 10

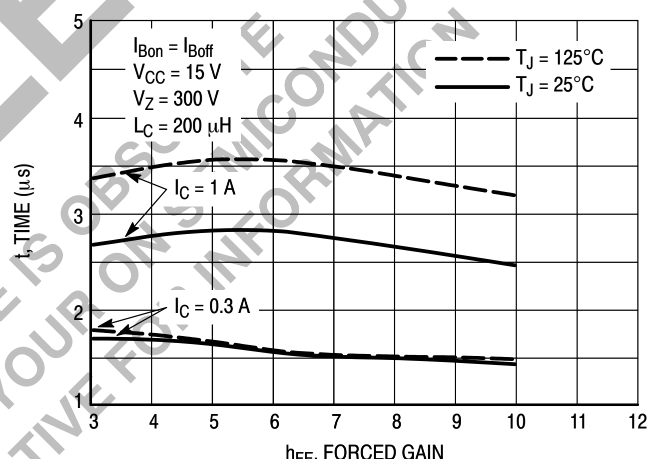


Figure 20. Inductive Storage Time, t_{si}

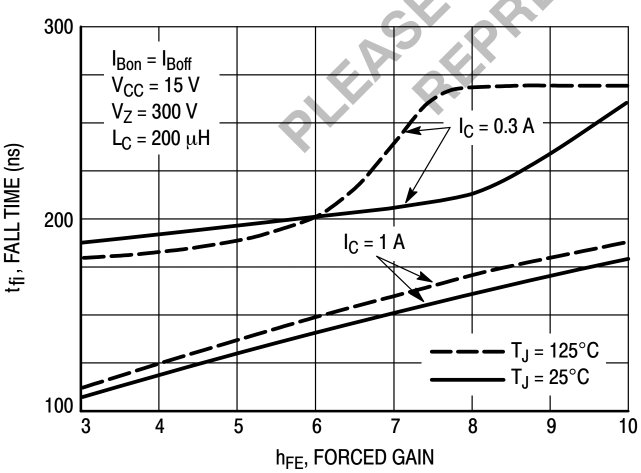


Figure 21. Inductive Fall Time, t_f

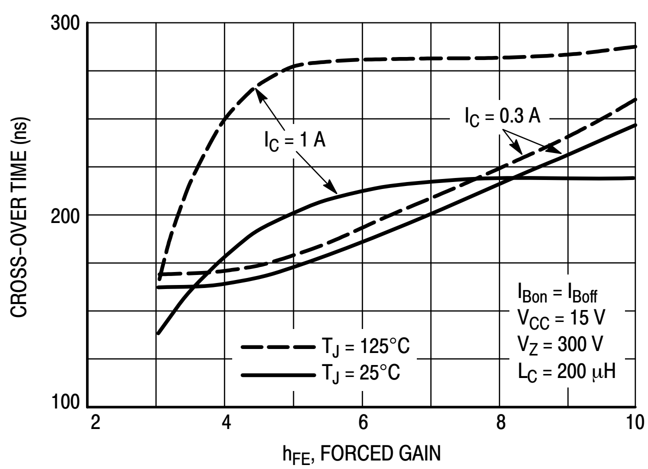


Figure 22. Inductive Cross Over Time, t_c

TYPICAL SWITCHING CHARACTERISTICS

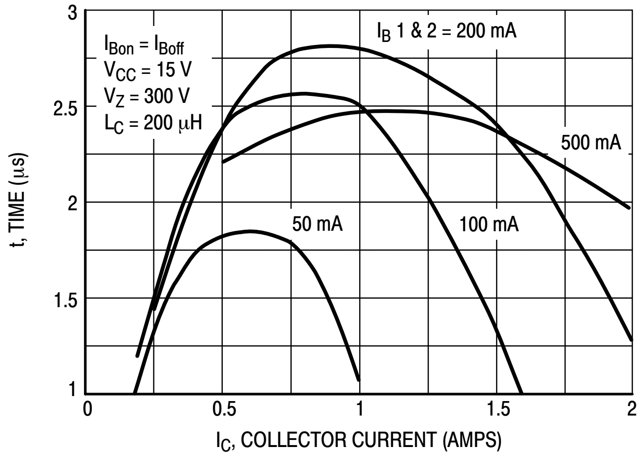


Figure 23. Inductive Storage Time, t_{si}

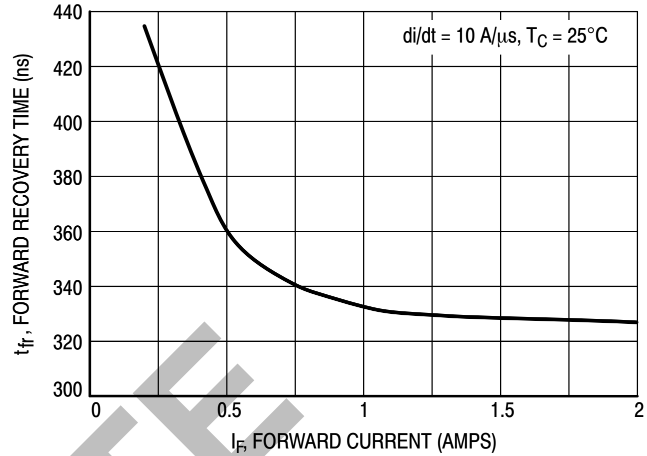


Figure 24. Forward Recovery Time, t_{fr}

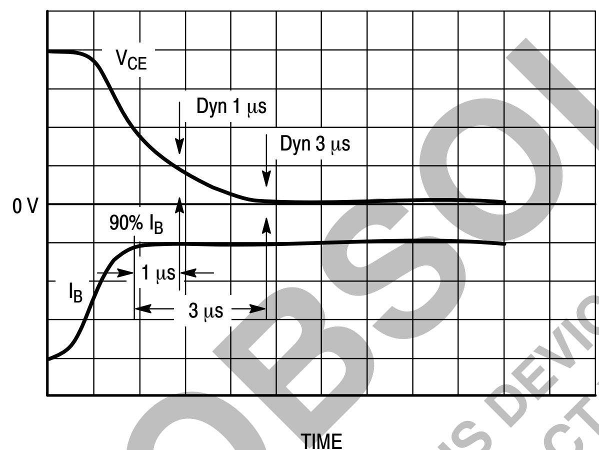


Figure 25. Dynamic Saturation Voltage Measurements

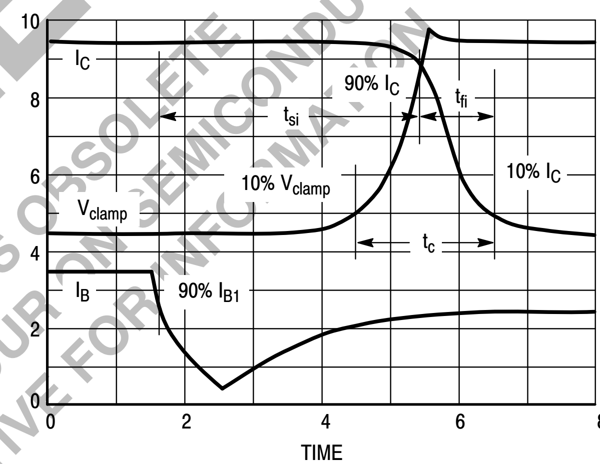
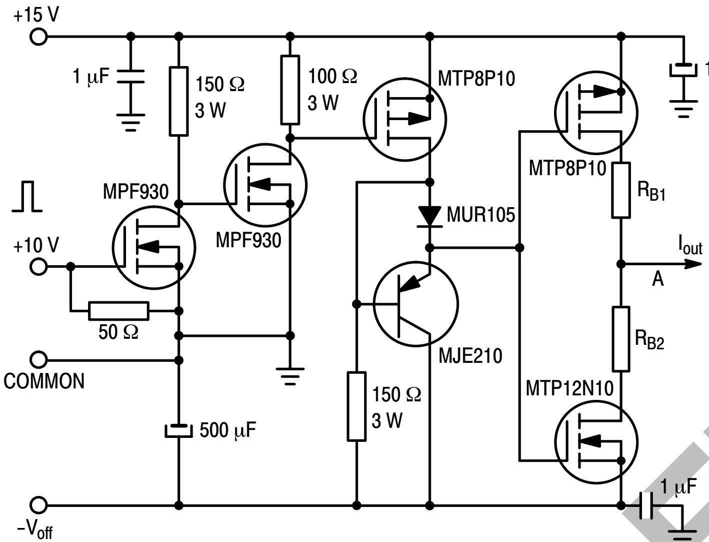
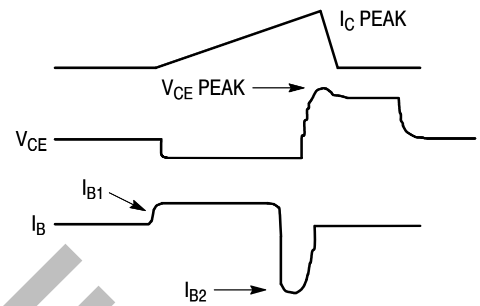


Figure 26. Inductive Switching Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
$R_{B2} = \infty$	$R_{B2} = 0$	$R_{B2} = 0$
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

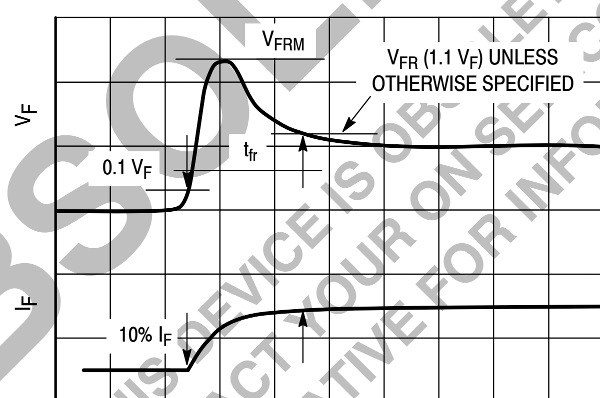


Figure 27. t_{fr} Measurement

MAXIMUM RATINGS

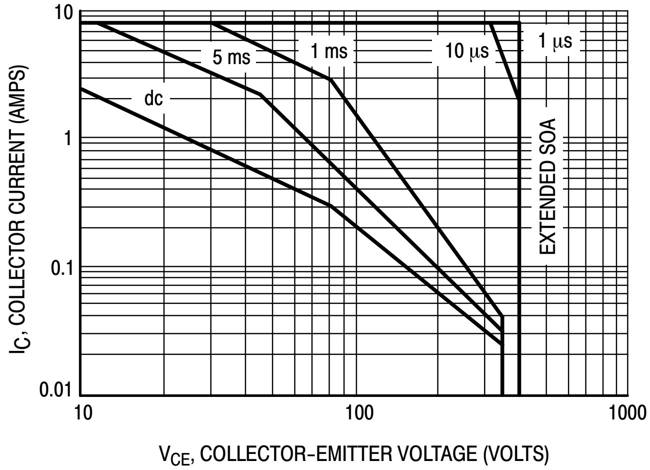


Figure 28. Forward Bias Safe Operating Area

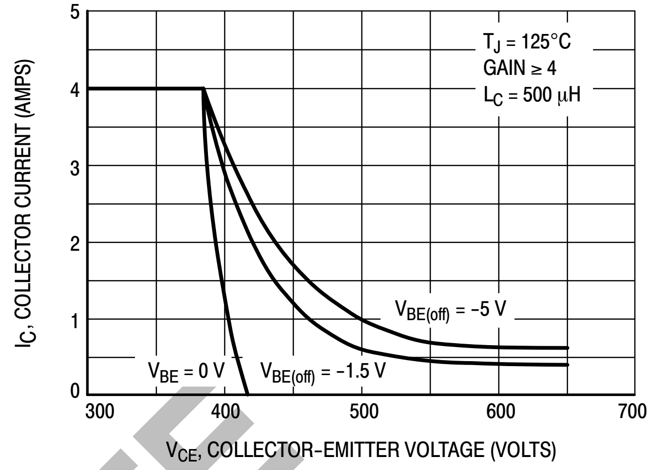


Figure 29. Reverse Bias Safe Operating Area

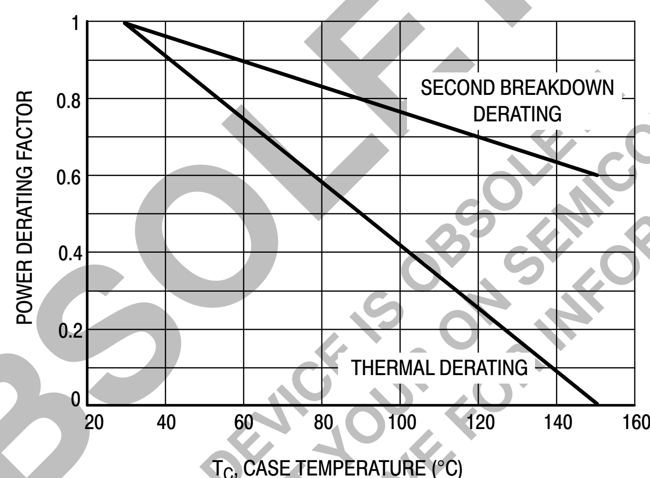


Figure 30. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on T_C = 25°C; $T_{j(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second Breakdown limitations do not derate like thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

$T_{j(pk)}$ may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as reverse biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

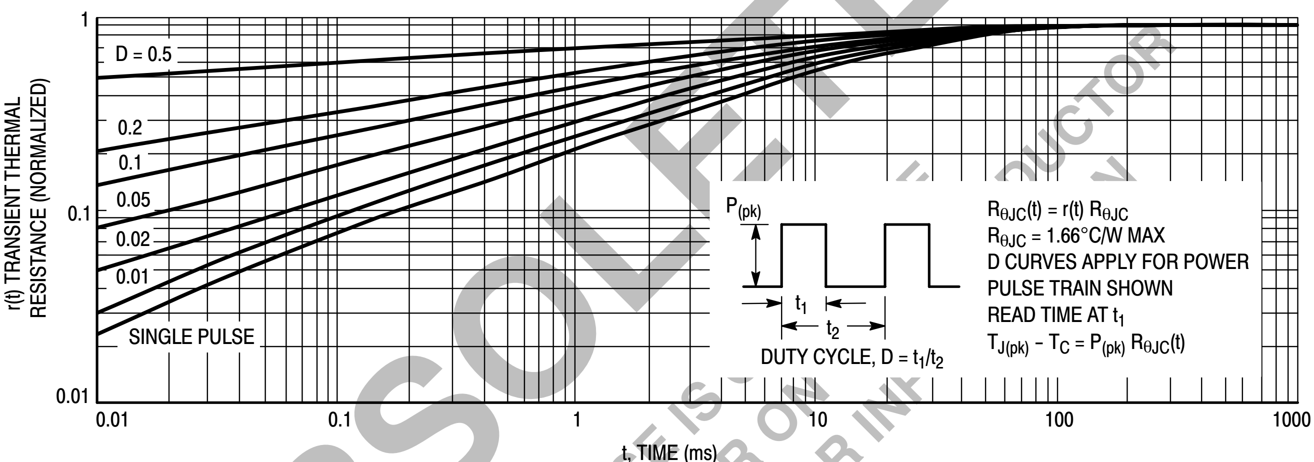
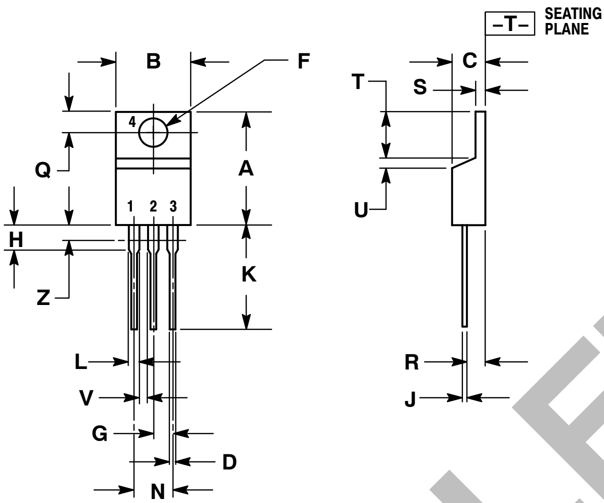


Figure 31. Thermal Response

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

PUBLICATION ORDERING INFORMATION

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