NLHV18T3244

18-Channel Level Shifter

The NLHV18T3244 is an 18−channel level translator designed for high voltage level shifting applications such as displays. The 18 channels are divided into twelve and two three channel groups, with each group controlled by the inverting inputs SEL1, SEL2 and, SEL3; respectively. The EN input is used to select the ‘ON’ or power saving shutdown modes.

Each channel consists of a high voltage output buffer. The output buffers use N−channel low side and P−channel high side transistors. The output signal on pins OUT1 to OUT18 is pulled by the transistors to the positive high or negative low voltage on the V_{Hx} and V_{Lx} power supply pins, respectively, depending on the voltage of the inverting pins.

Features

- 18 Non−Inverting / Inverting Channels
- V_{H1}, V_{H2} Supply Range: 5 V to 25 V
- V_{L1}, V_{L2} Supply Range: −13 V to 0 V
- $V_{Hx} - V_{Lx}$ Difference Range: 5 V to 25 V
- V_{L1} and V_{L2} can be tied together or connected to independent supply voltages as long as $V_{L1} \leq V_{L2}$
- V_D Supply Range: 2 V to 5.5 V
- Outputs Specified with 1000 pF Capacitive Loads
- Disable Function
- Low Standby Current
- No Glitch on Power−Up
- Available in: 5 mm x 10 mm, 0.5 mm pitch, QFN50 Package

Typical Applications

- OLED Drivers
- High Voltage Level Shifters
- Piezoelectric Motor Drivers

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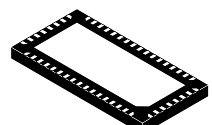


QFN50
CASE 485BW

MARKING DIAGRAM

NLHV
18T3244
AWLYYWWG

A	=	Assembly Location
WL	=	Wafer Lot
YY	=	Year
WW	=	Work Week
G	=	Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

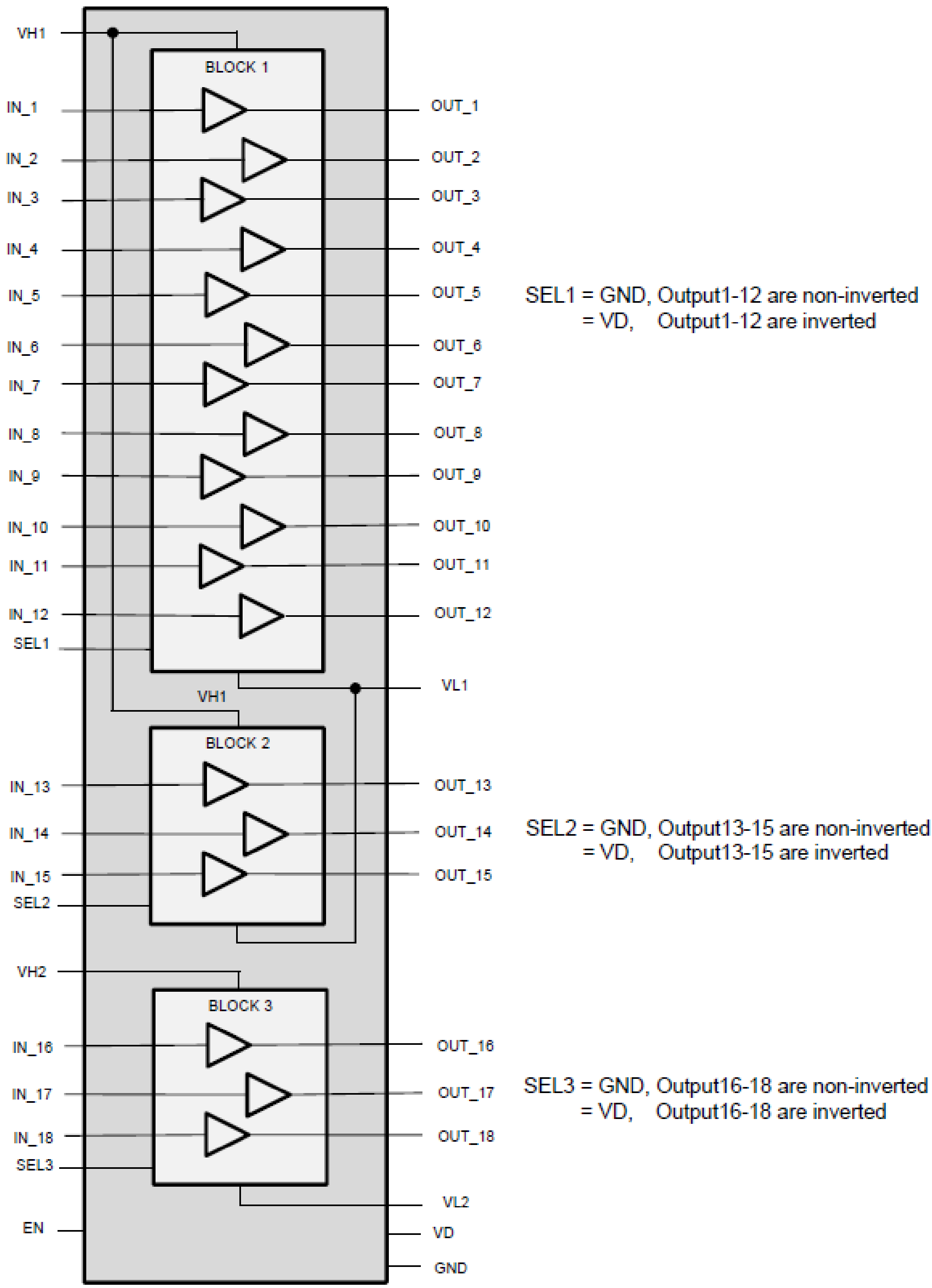


Figure 1. Simplified Schematic − Option I ($V_{L1} \le V_{L2}$)

FUNCTION TABLE (X Input = 'Don't Care, Hi−Z = High Impedance Tri−State Output)

Input				Output		
EN	**SEL1**	**SEL2**	**SEL3**	**Block 1 (OUT1−OUT12)**	**Block 2 (OUT13 − OUT15)**	**Block 3 (OUT16 − OUT18)**
GND	X	X	X	Hi−Z	Hi−Z	Hi−Z
V_D	GND	GND	GND	Normal	Normal	Normal
V_D	GND	GND	V_D	Normal	Normal	Inverted
V_D	GND	V_D	GND	Normal	Inverted	Normal
V_D	GND	V_D	V_D	Normal	Inverted	Inverted
V_D	V_D	GND	GND	Inverted	Normal	Normal
V_D	V_D	GND	V_D	Inverted	Normal	Inverted
V_D	V_D	V_D	GND	Inverted	Inverted	Normal
V_D	V_D	V_D	V_D	Inverted	Inverted	Inverted

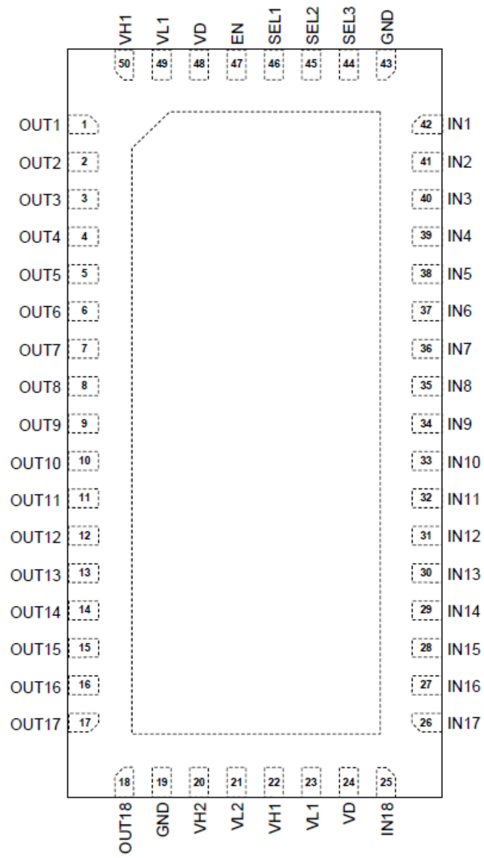


Figure 2. Pin Assignments

(Top View)

PIN ASSIGNMENTS

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
OUT1	1	OUT18	18	IN8	35
OUT2	2	GND	19	IN7	36
OUT3	3	VH2	20	IN6	37
OUT4	4	VL2	21	IN5	38
OUT5	5	VH1	22	IN4	39
OUT6	6	VL1	23	IN3	40
OUT7	7	VD	24	IN2	41
OUT8	8	IN18	25	IN1	42
OUT9	9	IN17	26	GND	43
OUT10	10	IN16	27	SEL3	44
OUT11	11	IN15	28	SEL2	45
OUT12	12	IN14	29	SEL1	46
OUT13	13	IN13	30	EN	47
OUT14	14	IN12	31	VD	48
OUT15	15	IN11	32	VL1	49
OUT16	16	IN10	33	VH1	50
OUT17	17	IN9	34	No Connect	Center Tap

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
V_{Hx}	High−side DC Supply Voltage		−0.5 to +30	V
V_{Lx}	Low−side DC Supply Voltage		−15 to +0.5	V
$V_{Hx} - V_{Lx}$	Differential $V_H - V_L$ Voltage		0 to +30	V
V_D	Logic Supply Voltage		−0.5 to +5.5	V
V_I	Input (IN1 – IN18), Invert (SEL1 – SEL3) and Enable (EN) Control Pins		-0.5 to $V_D + 0.5$	V
V_{OUT}	Output Voltage Pins (OUT1 – OUT18)		$V_{Lx} - 0.5$ to $V_{Hx} + 0.5$	V
I_{OUT}	Continuous Output Current (OUT1 – OUT18)	One channel is sinking or sourcing current while the remaining seventeen channels are disconnected (I_{OUT} = 0 A)	100	mA
I_{HX}	DC Supply Current Through V_{HX}		100	mA
I_{LX}	DC Supply Current Through V_{LX}		100	mA
I_D	DC Supply Current Through V_D		50	mA
$R_{\theta JA}$	Junction to Ambient Resistance	(Note 1)	68	°C/W
T_J	Junction Temperature		+115	°C
T_{STG}	Storage Temperature		−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 4 layer PCB with 100 sq. mm, 1 oz. heat spreading including traces, JEDEC 51.7 equivalent.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{H1}	High−side DC Supply Voltage	5	25	V
V_{H2}	High−side DC Supply Voltage (Note 2)	5	25	V
V_{L1}	Low−side Negative DC Supply Voltage (Note 3) ($V_{L1} \leq V_{L2}$)	−13	0	V
V_{L2}	Low−side Negative DC Supply Voltage (Note 4)	V_{L1}	0	V
$V_{Hx} - V_{Lx}$	Differential $V_H - V_L$ Voltage	5	25	V
V_D	Logic Supply Voltage	2	5.5	V
V_I	Input (IN1 – IN18), Invert (SEL1 – SEL3) and Enable (EN)	GND	V_D	V
V_{OUT}	Output Voltage (OUT1 – OUT18)	V_{Lx}	V_{Hx}	V
T_A	Operating Temperature Range	−40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Rate V_I, V_{IO} from 30% to 70% of V_D; V_D =3.3 ± 0.3 V	0	10	nS

2. V_{H1} and V_{H2} can be connected together.
3. V_{L1} must be at the lowest DC supply voltage.
4. V_{L1} and V_{L2} can be connected together.

ELECTRICAL CHARACTERISTICS (V_{Hx} =15 V, V_{Lx} = −5 V, V_D = 2 to 5.5 V and EN = V_D; unless otherwise specified)

Symbol	Parameter	Parameter	Test Conditions	−40°C to +85°C Min	Typ	Max	Unit
POWER SUPPLY							
I_D	Digital Supply Static Current	Enabled (EN = V_D)	IN1 to IN18 = 0 V or IN1 to IN18 = V_D		2		mA
		Disabled (EN = 0 V), (Power Down)			5	10	μA
I_{H1}	Block 1 and 2 High Voltage Supply Static Current	Enabled (EN = V_D)	IN1 to IN18 = 0 V or IN1 to IN18 = V_D		2		mA
		Disabled (EN = 0 V), (Power Down)			5		μA
I_{H2}	Block 3 High Voltage Supply Static Current	Enabled (EN = V_D)	IN1 to IN18 = 0 V or IN1 to IN18 = V_D		2		mA
		Disabled (EN = 0 V), (Power Down)			5		μA
I_{L1}	Block 1 and 2 Low Voltage Supply Static Current	Enabled (EN = V_D)	IN1 to IN18 = 0 V or IN1 to IN18 = V_D		2		mA
		Disabled (EN = 0 V), (Power Down)			5		μA
I_{L2}	Block 3 Low Voltage Supply Static Current	Enabled (EN = V_D)	IN1 to IN18 = 0 V or IN1 to IN18 = V_D		2		mA
		Disabled (EN = 0 V), (Power Down)			5		μA
V_{H1}	High−Side DC Supply 1			5	15	25	V
V_{H2}	High−Side DC Supply 2			5	17	25	V
V_{L1}	Low−Side DC Supply 1		$V_{L1} \le V_{L2}$ V_{L1} must be the lowest voltage in all conditions	−13	−5	0	V
V_{L2}	Low−Side DC Supply 2			V_{L1}	−5	0	V
$V_{Hx} - V_L$	Differential $V_{Hx} - V_L$ Voltage			5		25	V
INPUT (IN1 – IN18, EN, SEL1 – SEL3)							
V_{IH}	Logic ‘1’ Input Voltage			0.7 x V_D			V
V_{IL}	Logic ‘0’ Input Voltage					0.3 x V_D	V
I_{IH}	Logic ‘1’ Input Current		$V_I = V_{IH}$		0.1	10	μA
I_{IL}	Logic ‘0’ Input Current		$V_I = V_{IL}$		0.1	10	μA
C_{IN}	Input Capacitance		T_A = 25°C		3.5		pF
R_{IN}	Input Resistance		T_A = 25°C		50		MΩ
OUTPUT (OUT1 – OUT18)							
V_{OH}	V_{OUT} High Voltage		INx = 3.3 V, I_L = 20 mA	V_{HX}−0.2			V
V_{OL}	V_{OUT} Low Voltage		INx = 0 V, I_L = 20 mA			V_{LX} + 0.12	V
R_{OH}	ON Resistance, V_H to OUTx		I_L = 20 mA		5	8.5	Ω
R_{OL}	ON Resistance, V_L to OUTx		I_L = 20 mA		5	7.5	Ω
I_{PEAK}	Peak Output Current		C_L = 1000 pF		1100		mA
I_{OZ}	Output Tri−state Mode Leakage Current		INx = 3.3 V, V_D = 3.3 V, EN = GND			5	μA

SWITCHING CHARACTERISTICS (C_L = 1000 pF, V_{Hx} = 15 V, V_{Lx} = −5 V, V_D = 3.3 V and EN = 3.3 V; unless otherwise specified)

Symbol	Parameter	Test Conditions	−40°C to +85°C			Unit
			Min	Typ	Max	
t_R	Output Rise Time	Measured from 10% to 90%		20	35	ns
t_F	Output Fall Time	Measured from 90% to 10%		20	35	ns
t_{RFD}	Output Rise and Fall Time Mismatch (per channel)			5		ns
t_{SK}	Output Skew Matching (channel−to−channel)	Measured from 50% to 50%		5		ns
t_{D+}	Turn−On Propagation Delay	Measured from 50% to 50%		55		ns
t_{D-}	Turn−Off Propagation Delay	Measured from 50% to 50%		55		ns
t_{DD}	High−to−Low/Low−to−High Propagation Delay Mismatch (per channel)	Measured from 50% to 50%		5		ns
$SC\#_{MAX}$	Maximum channels switched in 100 ns sequence	Delta between inputs of channels must be 100 ns if channels are switched in sequence			6	
Con_OUT	Outputs connected together to increase drive capability				3	
f_{MAX}	Maximum switching Frequency	For all V_{Hx} and V_{Lx} voltages			100	kHz
t_{EN}	Enable Time	Measured from 50% EN to 50% OUT_xx	9.8		15	μs
t_{DIS}	Disable Time	Measured from 50% EN to 50% OUT_xx_Hi−Z		2.2		μs

DATA RATES (C_L = 1000 pF, V_{Hx} = 15 V, V_{Lx} = −5 V, V_D = 3.3 V and EN = 3.3 V; unless otherwise specified)

Channel	Conditions	Data Rate	Unit
IN1 − IN6 (Note 5)	Simultaneous Switching (Turn ON and OFF in sequence, 100 ns between channels)	120	Hz
	Per Channel	56	kHz
IN7− IN12 (Note 5)	Per Channel	120	Hz
IN13 – IN 15 (Note 5)	Per Channel	120	Hz
IN16 – IN18 (Note 5)	Simultaneous Switching (Turn ON and OFF sequence, 100 ns between channels)	120	Hz

5. While IN1 − IN6 are switching, IN1 − IN18 are not switching.

APPLICATIONS INFORMATION

Power−Up Sequence

The recommended power−up sequence of the power supplies is provided in Figure 3.

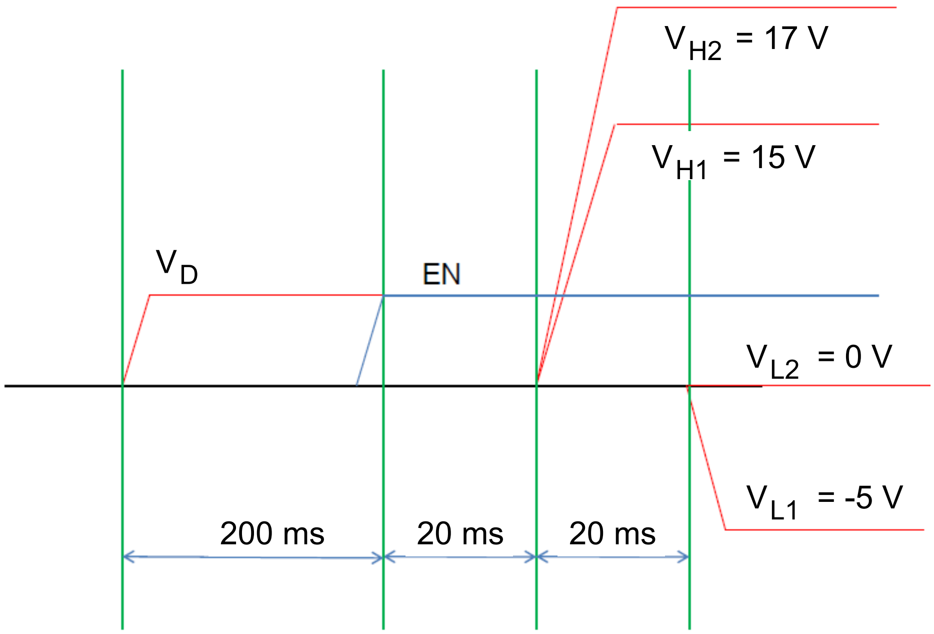


Figure 3. Power−Up Sequence

Power Supply Guidelines

Supply voltage V_{L1} must be less than or equal to voltage V_{L2}. The substrate is connected to V_{L1}; thus, V_{L1} must be the at lowest voltage potential to ensure proper biasing of the internal level shifting circuits. In addition, setting V_{L1} to the lowest voltage ensures proper operation of the overvoltage and ESD protection circuits connected on the supply voltage and input/output lines, respectively.

For optimal performance, 0.1 and 1 μF decoupling capacitors are recommended for the V_D, V_{L1}, V_{L2}, V_{H1}, and V_{H2} power supply pins. High frequency ceramic or tantalum capacitors are good design choices to filter and bypass any noise signals on the supply voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces. In addition, a ferrite bead can be placed between the two decoupling capacitors to form a bi-directional LC Tee filter if additional noise immunity is required.

Recommended PCB Options

2 Layer PCB

- Traces = 1.4 mm width, tin plating, copper 2 oz
- Routing of power lines will be in top layer
- In order to minimize inductance, returning current will be routed as close as possible to the power lines

4 Layer PCB

- Traces = 1.4 mm width, tin plating, copper 2 oz
- In order to reduce inductance, construction of layers will be as drawing below
- Power lines will be routed in top and returning current will be routed in inner1 right below the power lines

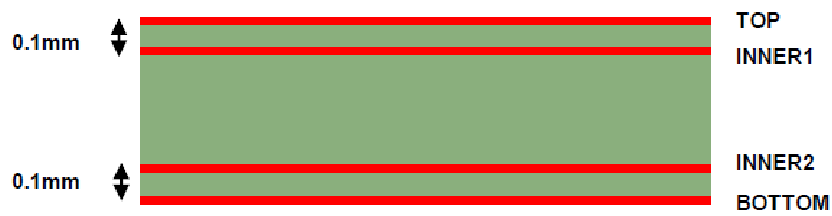


Figure 4. Recommended 4Layer PCB Options

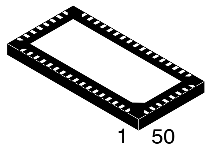
PCB Layout Instructions

- The power devices should be placed as close as possible to each other in order to reduce inductance
- Decoupling filter capacitors should be placed as close as possible to the device in order to reduce ripple on supply.
- The V_H, V_L and V_D decoupling filter capacitors connected between the power supply and GND should be constructed from scaled capacitors. A small value capacitor of 0.1 μF, which filters high frequency, should be placed as close as possible to the device. A larger value capacitor of 1 μF, which filters low frequency should be placed adjacent to the small capacitor, but farther away from the device.
- All output line should be far from each other to prevent cross talk
- All input lines should be matched in length to meet skew timing

ORDERING INFORMATION

Device	Package	Shipping†
NLHV18T3244MNTWG	QFN−50 (Pb−Free)	2500 / Tape & Reel

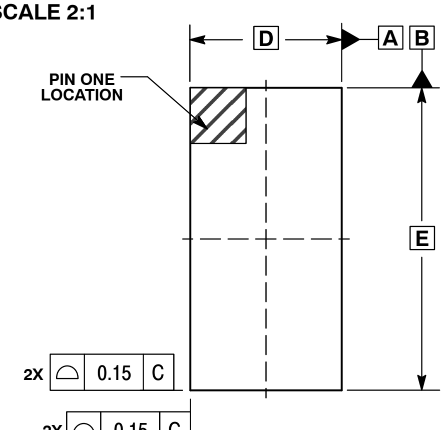
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



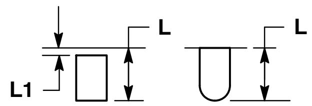
SCALE 2:1

QFN50 10x5, 0.5P
CASE 485BW
ISSUE O

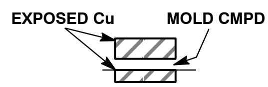
DATE 21 JUL 2011



TOP VIEW



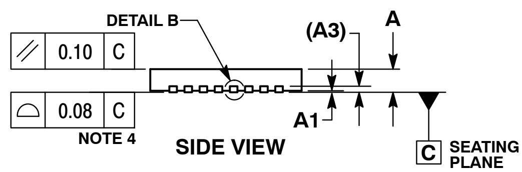
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



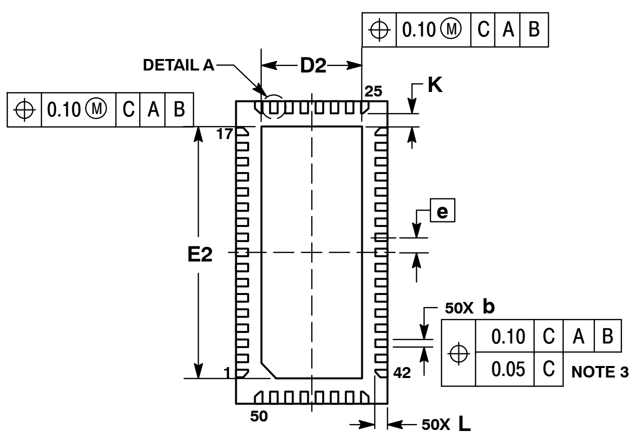
DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	3.20	3.45
E	10.00 BSC	
E2	8.20	8.45
e	0.50 BSC	
K	0.20 MIN	
L	0.30	0.50
L1	0.00	0.15



SIDE VIEW



BOTTOM VIEW

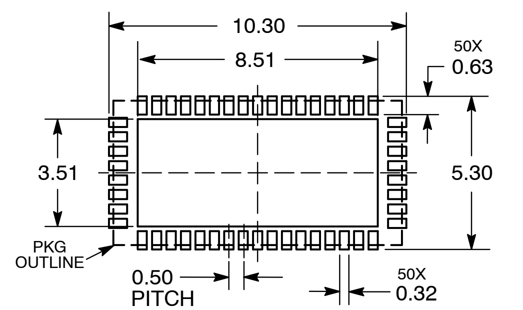
GENERIC
MARKING DIAGRAM*

XXXXXXXX
XXXXXXXX
AWLYYWWG
∘

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON57518E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	QFN50, 10x5, 0.5MM PITCH	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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