NCP2991

1.35 Watt Audio Power Amplifier with Selectable Fast Turn On Time

The NCP2991 is an audio power amplifier designed for portable communication device applications such as mobile phone applications. The NCP2991 is capable of delivering 1.35 W of continuous average power to an 8.0 Ω BTL load from a 5.0 V power supply, and 1.1 W to a 4.0 Ω BTL load from a 3.6 V power supply.

The NCP2991 provides high quality audio while requiring few external components and minimal power consumption. It features a low−power consumption shutdown mode, which is achieved by driving the $\overline{\text{SHUTDOWN}}$ pin with logic low.

The NCP2991 contains circuitry to prevent from "pop and click" noise that would otherwise occur during turn−on and turn−off transitions. It is a zero pop noise device when a single ended or a differential audio input is used.

For maximum flexibility, the NCP2991 provides an externally controlled gain (with resistors). In addition, it integrates 2 different Turn On times (15 ms or 30 ms) adjustable with the TON pin.

Due to its superior PSRR, it can be directly connected to the battery, saving the use of an LDO.

This device is available in a 9−Pin Flip−Chip CSP (Lead−Free).

Features

- 1.35 W to an 8.0 Ω BTL Load from a 5.0 V Power Supply
- Best−in−Class PSRR: up to −100 dB, Direct Connection to the Battery
- Zero Pop Noise Signature with a Single Ended Audio Input
- Ultra Low Current Shutdown Mode: 10 nA
- 2.5 V−5.5 V Operation
- External Gain Configuration Capability
- External Turn−on Time Configuration Capability: 15 ms or 30 ms
- Thermal Overload Protection Circuitry
- This is a Pb−Free Device*

Typical Applications

- Portable Electronic Devices
- PDAs
- Wireless Phones

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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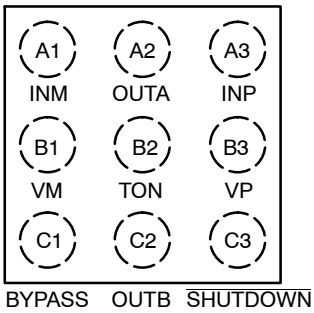
MARKING DIAGRAMS

9−Pin Flip−Chip CSP
FC SUFFIX
CASE 499E

MRH	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

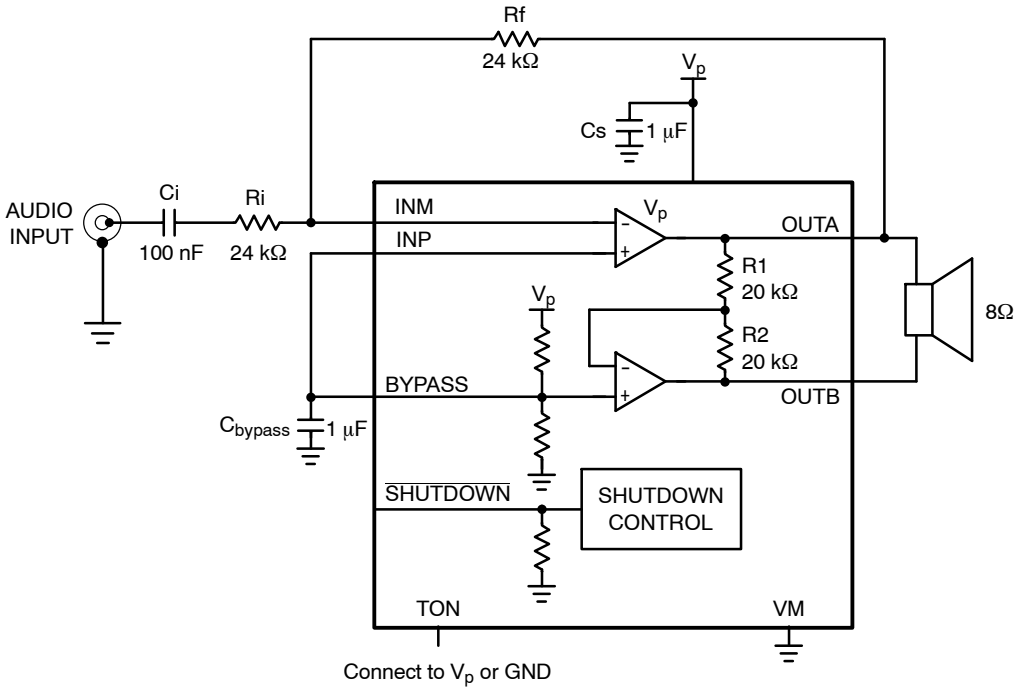


Figure 1. Typical Audio Amplifier Application Circuit with Single Ended Input

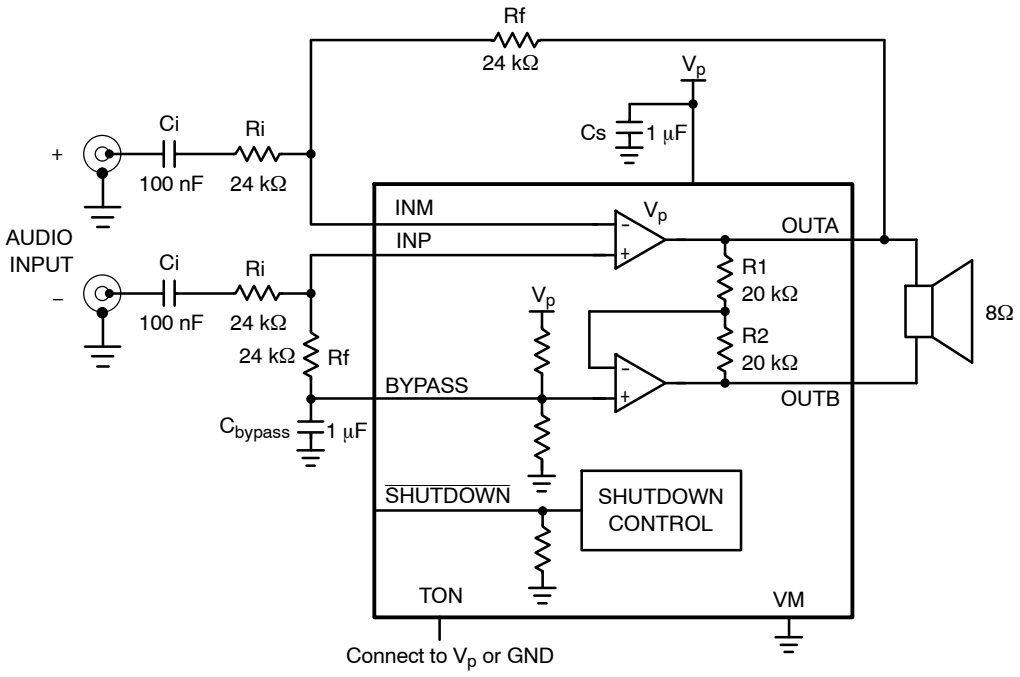


Figure 2. Typical Audio Amplifier Application Circuit with a Differential Input

PIN DESCRIPTION

Pin	Name	Type	Description
A1	INM	I	Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor R_f and to the input resistor R_{in}.
A2	OUTA	O	Negative output of the NCP2991. Connected to the load and to the feedback resistor Rf.
A3	INP	I	Positive input of the first amplifier, receives the common mode voltage.
B1	VM	I	Analog Ground.
B2	TON	I	TON pin selects 2 different Turn On times: TON = GND –> 30 ms TON = VP –> 15 ms
B3	VP	I	Positive analog supply of the cell. Range: 2.5 V–5.5 V.
C1	BYPASS	I	Bypass capacitor pin which provides the common mode voltage (Vp/2).
C2	OUTB	O	Positive output of the NCP2991. Connected to the load.
C3	$\overline{\text{SHUTDOWN}}$	I	The device enters in shutdown mode when a low level is applied on this pin.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_p	6.0	V
Operating Supply Voltage	Op Vp	2.5 to 5.5 V	–
Input Voltage	V_{in}	–0.3 to V_{CC} +0.3	V
Power Dissipation (Note 2)	Pd	Internally Limited	–
Operating Ambient Temperature	T_A	–40 to +85	°C
Max Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Thermal Resistance Junction–to–Air	$R_{\theta JA}$	(Note 3)	°C/W
ESD Protection Human Body Model (HBM) (Note 4) Machine Model (MM) (Note 5)	–	2000 200	V
Latchup Current @ T_A = 85°C (Note 6)	–	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.
2. The thermal shutdown set to 160°C (typical) avoids irreversible damage on the device due to power dissipation.
3. The $R_{\theta JA}$ is highly dependent of the PCB Heatsink area. For example, $R_{\theta JA}$ can equal 195°C/W with 50 mm^2 total area and also 135°C/W with 500 mm^2. The bumps have the same thermal resistance and all need to be connected to optimize the power dissipation.
4. Human Body Model, 100 pF discharge through a 1.5 kΩ resistor following specification JESD22/A114.
5. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

ELECTRICAL CHARACTERISTICS Limits apply for T_A between −40°C to +85°C (Unless otherwise noted).

Characteristic	Symbol	Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Supply Quiescent Current	I_{dd}	V_p = 2.5 V, No Load V_p = 5.0 V, No Load	– –	1.8 1.95	3.5	mA
		V_p = 2.5 V, 8 Ω V_p = 5.0 V, 8 Ω	– –	1.8 1.95	3.5	
Common Mode Voltage	V_{cm}	–	–	V_p/2	–	V
Shutdown Current	I_{SD}		–	0.02	0.5	μA
Shutdown Pull−Down	R_{SD}		–	300	–	kΩ
Shutdown Voltage High	V_{SDIH}	–	1.2	–	–	V
Shutdown Voltage Low	V_{SDIL}	–	–	–	0.4	V
Turn On Time (Note 8)	T_{WU}	TON = GND TON = VP	–	30 15	–	ms
Turn Off Time	T_{OFF}	–	–	1.0	–	μs
Output Impedance in Shutdown Mode	Z_{SD}	–	–	8.5	–	kΩ
Output Swing	$V_{loadpeak}$	V_p = 2.5 V, R_L = 8.0 Ω V_p = 5.0 V, R_L = 8.0 Ω (Note 7) T_A = +25°C	1.9 3.8	2.4 4.7	– –	V
RMS Output Power	P_O	V_p = 2.5 V, R_L = 4.0 Ω THD + N < 1% V_p = 2.5 V, R_L = 8.0 Ω THD + N < 1% V_p = 5.0 V, R_L = 8.0 Ω THD + N < 1%	– –	0.5 0.3 1.35	– –	W
Maximum Power Dissipation (Note 8)	P_{Dmax}	V_p = 5.0 V, R_L = 8.0 Ω	–	–	0.65	W
Output Offset Voltage	V_{OS}	V_p = 2.5 V V_p = 5.0 V	–	1.0	–	mV
Signal−to−Noise Ratio	SNR	V_p = 2.5 V, G = 2.0 20 Hz < F < 20 kHz	–	86	–	dB
Positive Supply Rejection Ratio	PSRR V+	G = 2.0, R_L = 8.0 Ω C_{by} = 1.0 μF Input Grounded F = 217 Hz V_p = 5.0 V V_p = 4.2 V V_p = 3.0 V F = 1.0 kHz V_p = 5.0 V V_p = 4.2 V V_p = 3.0 V	 – – – – – –	 −91 −91 −91 −103 −103 −103	 – – – – – –	dB
Efficiency	η	V_p = 2.5 V, P_{orms} = 320 mW V_p = 5.0 V, P_{orms} = 1.0 W	– –	71 64	– –	%
Thermal Shutdown Temperature	T_{sd}		–	160	–	°C
Total Harmonic Distortion	THD	V_p = 2.5 V, F = 1.0 kHz R_L = 4.0 Ω, A_V = 2.0 P_O = 0.32 W V_p = 5.0 V, F = 1.0 kHz R_L = 8.0 Ω, A_V = 2.0 P_O = 1.0 W	– – – – – –	– 0.03 – – 0.015 –	– – – – – –	%

6. Min/Max limits are guaranteed by design, test or statistical analysis.
7. This parameter is guaranteed but not tested in production in case of a 5.0 V power supply.
8. See page 13 for a theoretical approach of this parameter.

TYPICAL CHARACTERISTICS

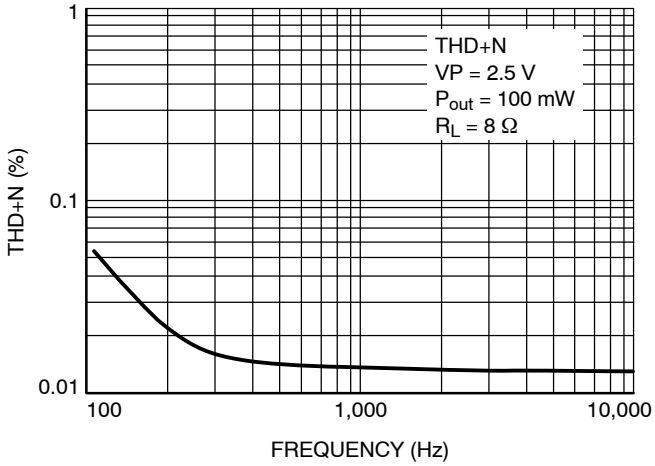


Figure 3. THD+N vs. Frequency

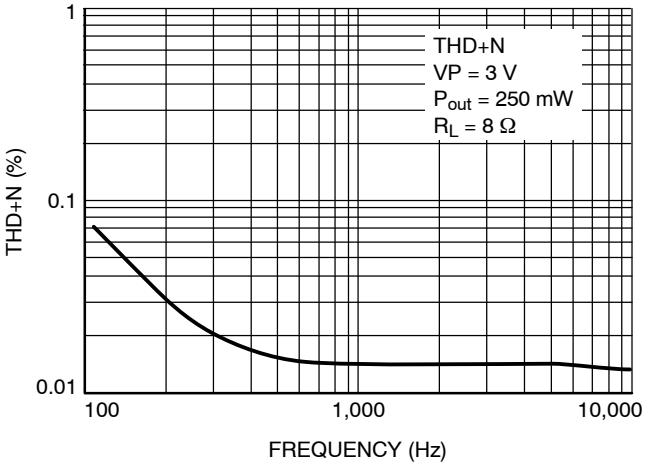


Figure 4. THD+N vs. Frequency

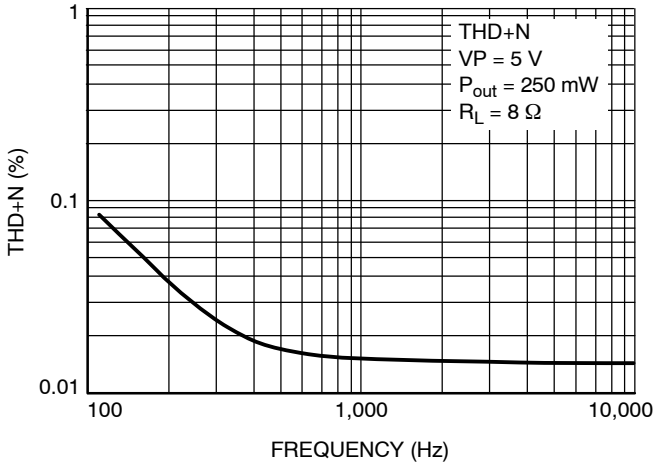


Figure 5. THD+N vs. Frequency

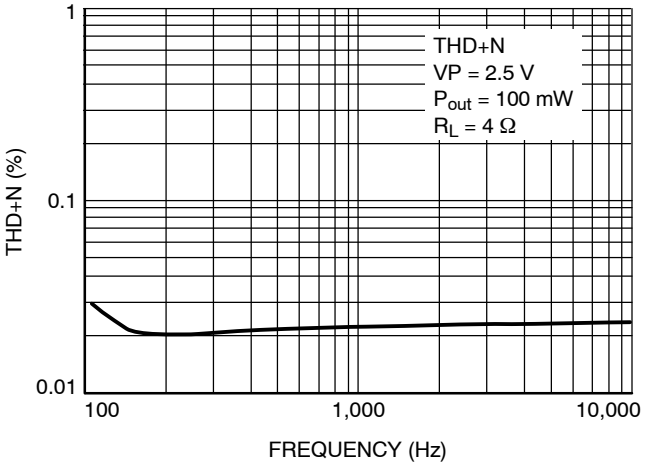


Figure 6. THD+N vs. Frequency

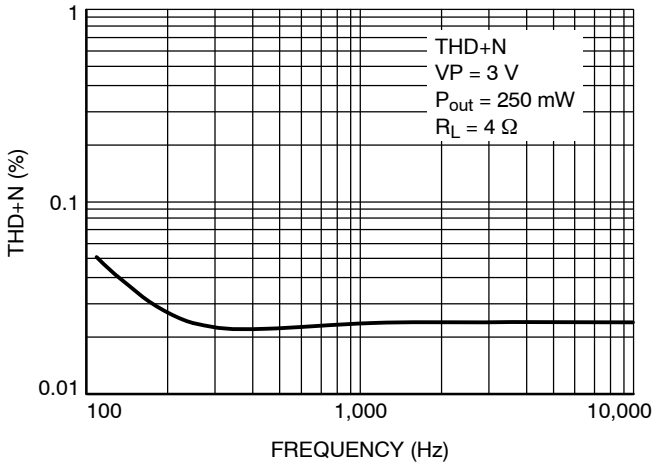


Figure 7. THD+N vs. Frequency

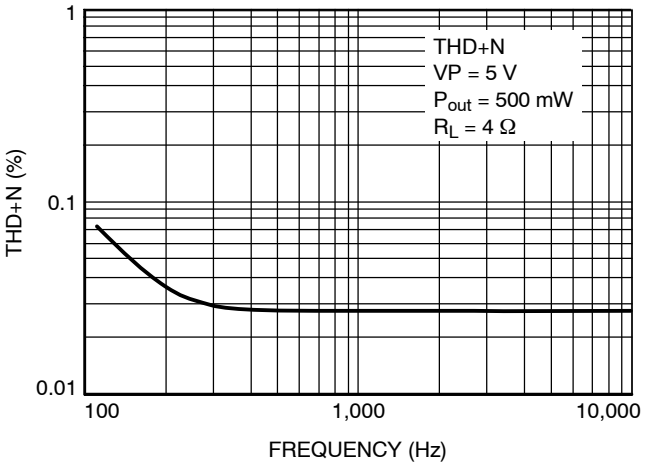


Figure 8. THD+N vs. Frequency

TYPICAL CHARACTERISTICS

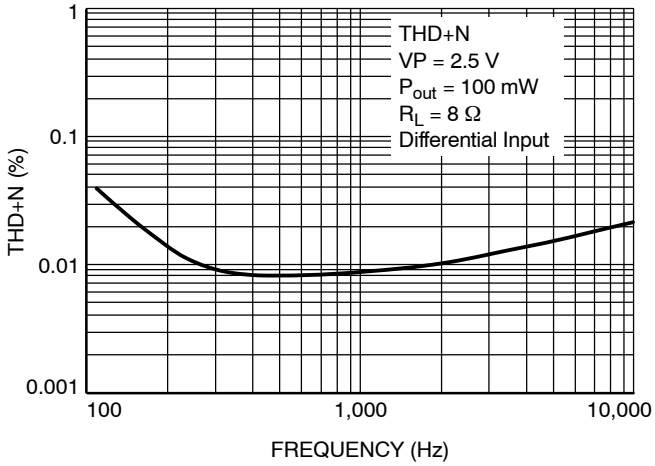


Figure 9. THD+N vs. Frequency

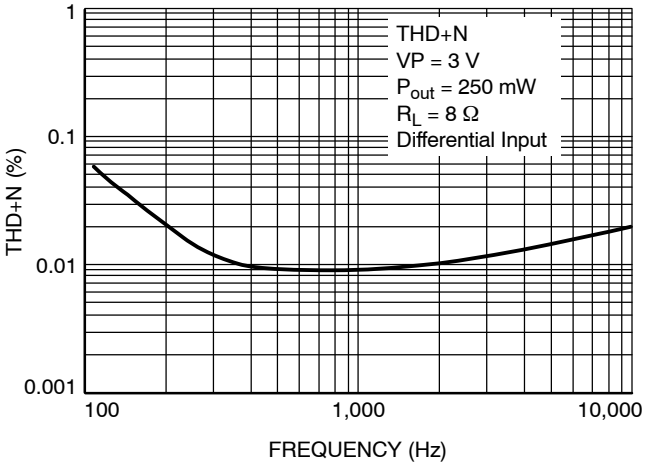


Figure 10. THD+N vs. Frequency

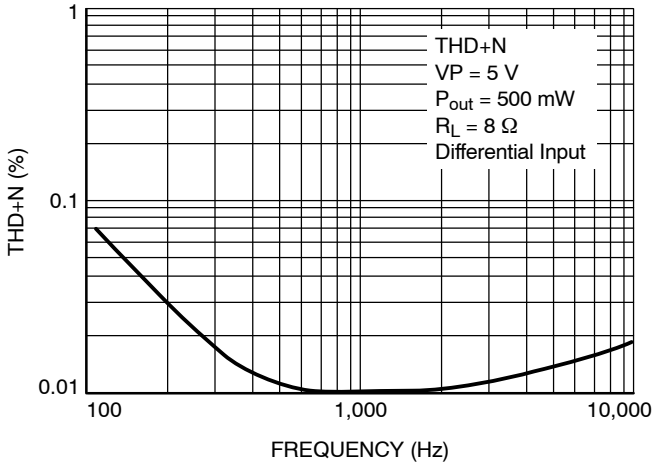


Figure 11. THD+N vs. Frequency

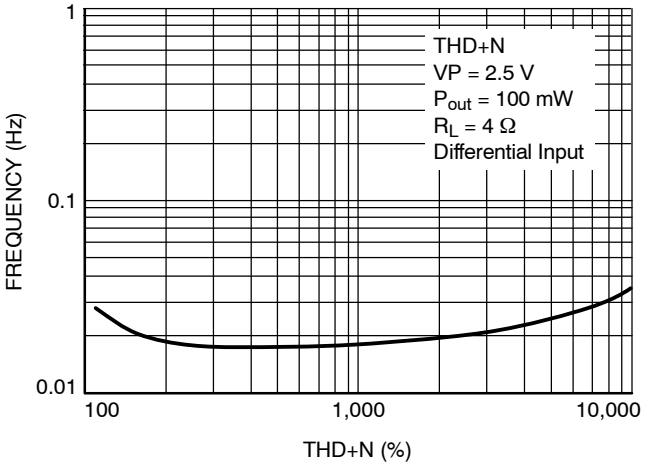


Figure 12. THD+N vs. Frequency

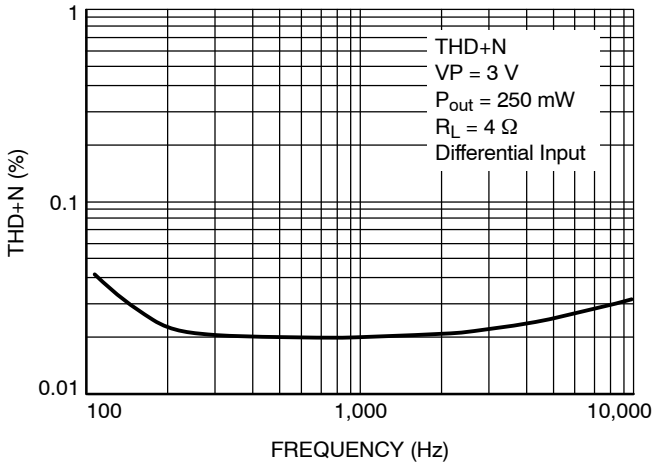


Figure 13. THD+N vs. Frequency

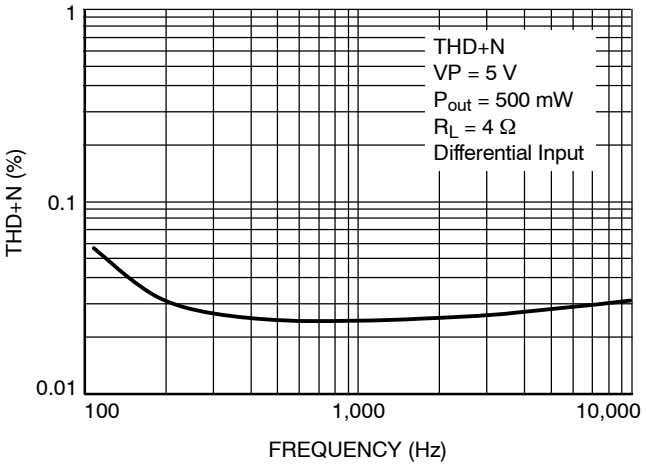


Figure 14. THD+N vs. Frequency

TYPICAL CHARACTERISTICS

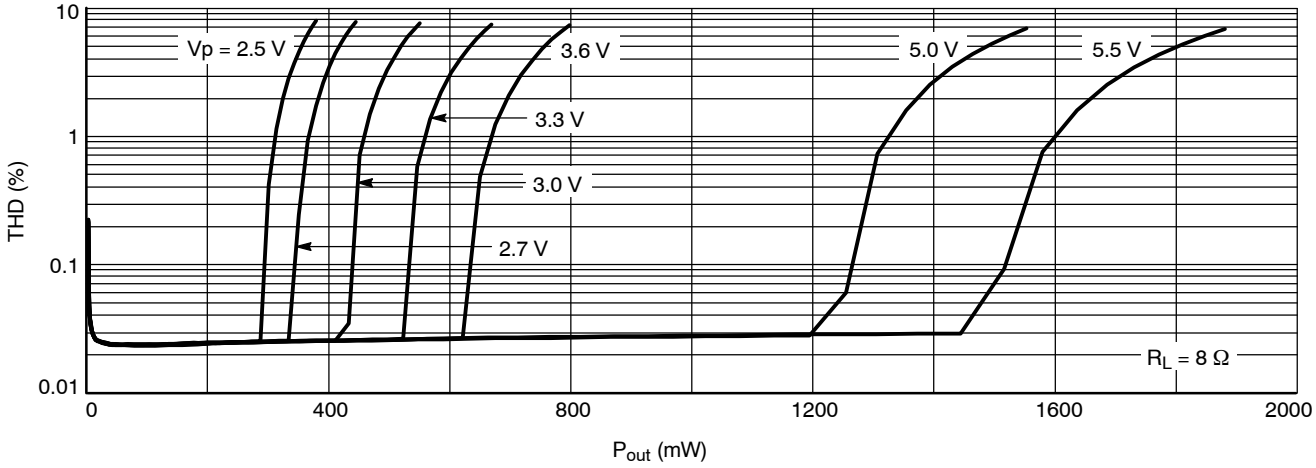


Figure 15. THD+N vs. P_{out}

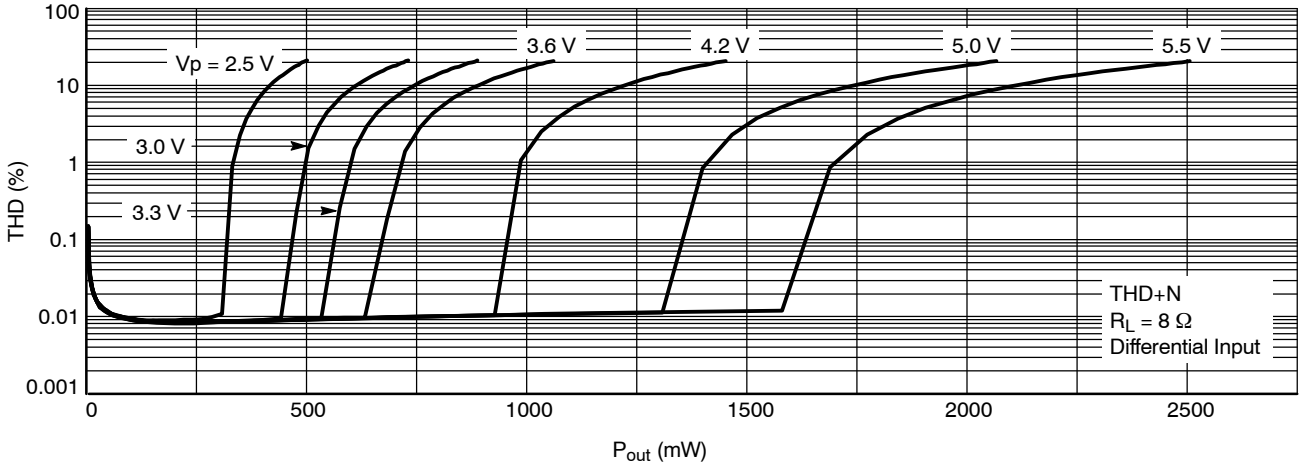


Figure 16. THD+N vs. P_{out}

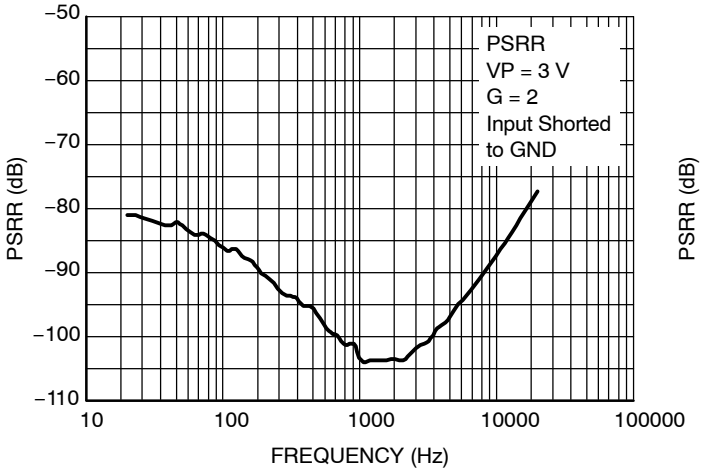


Figure 17. PSRR vs. Frequency

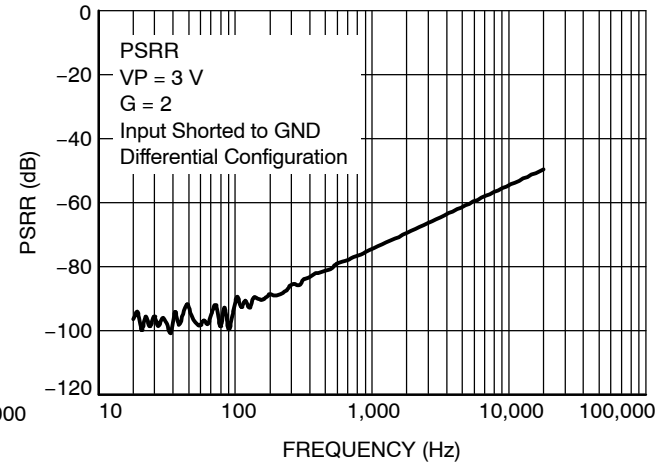


Figure 18. PSRR vs. Frequency

TYPICAL CHARACTERISTICS

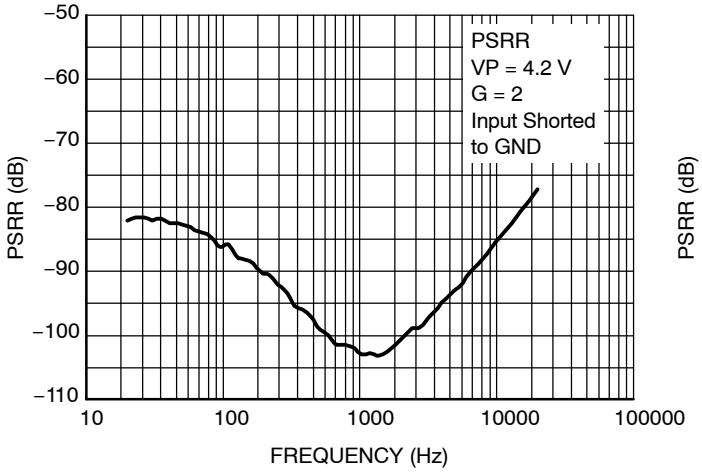


Figure 19. PSRR vs. Frequency

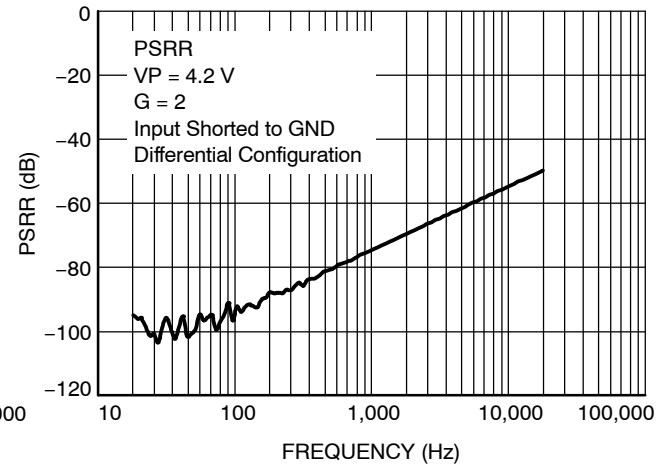


Figure 20. PSRR vs. Frequency

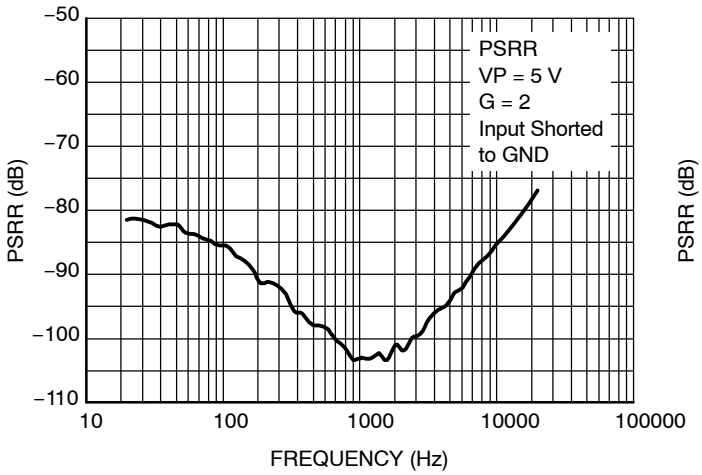


Figure 21. PSRR vs. Frequency

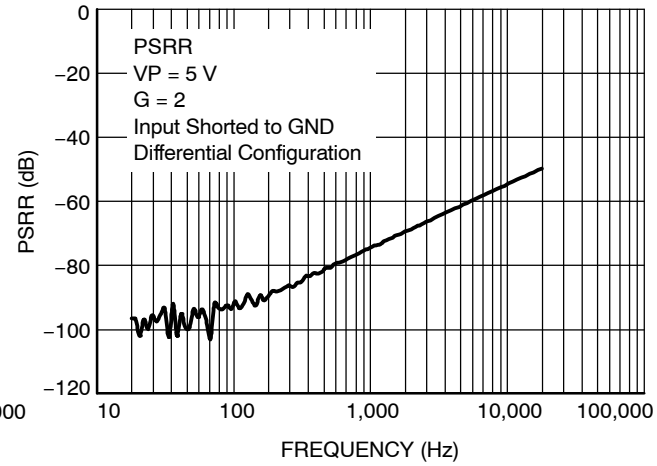


Figure 22. PSRR vs. Frequency

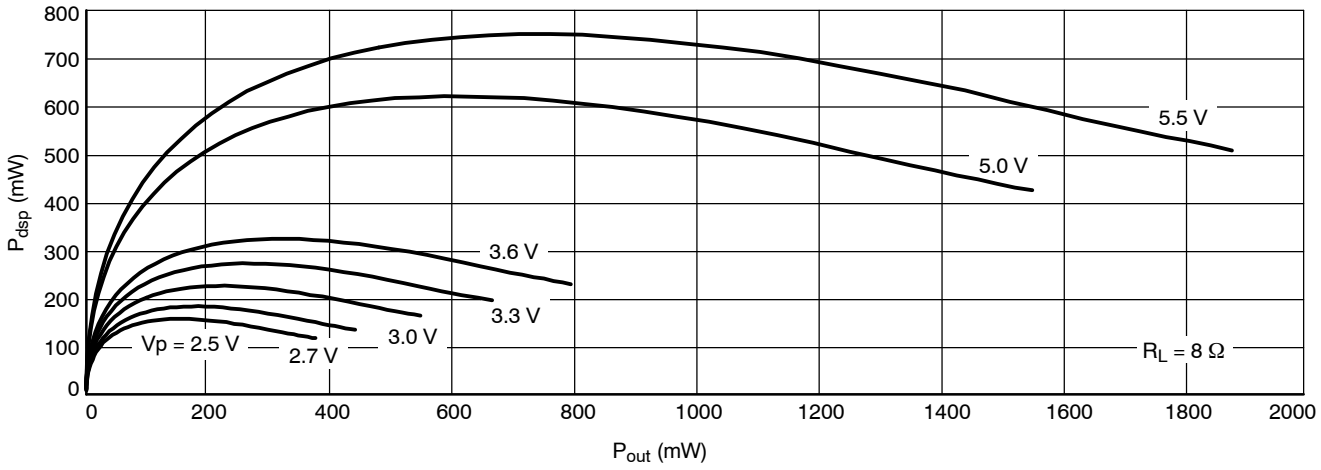


Figure 23. Power Dissipation vs. P_{out}

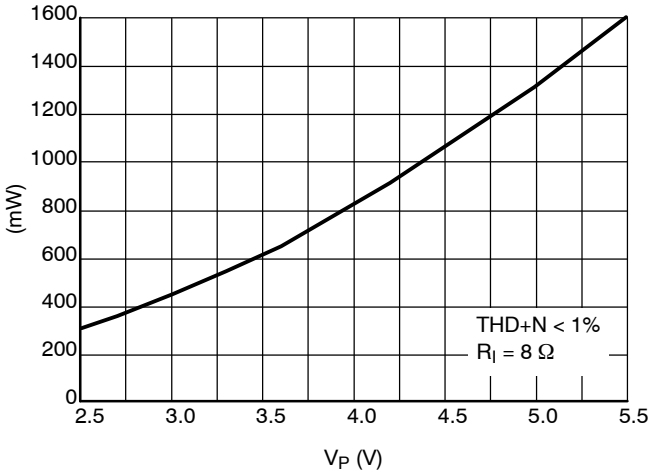


Figure 24. Maximum Output Power vs. V_P

Figure 25. Zero pop noise turn on sequence with single-ended input to ground (Ci = 100 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, RI = 8 Ω, Ton = GND)

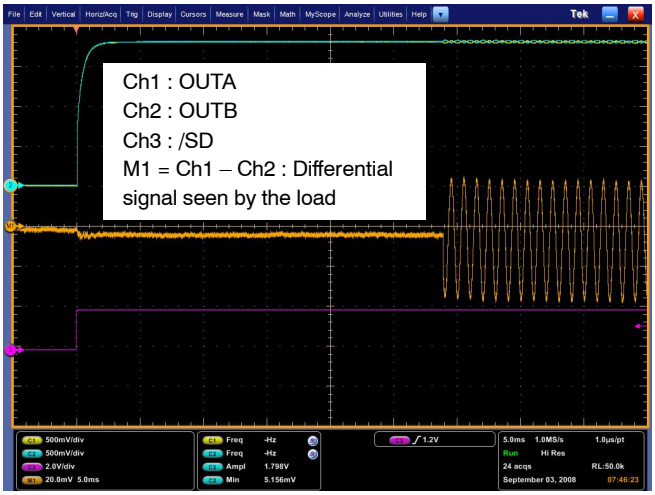


Figure 26. Zero pop noise turn on sequence with single-ended input audio source (Ci = 100 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, RI = 8 Ω, Ton = GND)

Figure 27. Zero pop noise turn off sequence with single-ended input to ground (Ci = 100 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, RI = 8 Ω, Ton = GND)

Figure 28. Zero pop noise turn off sequence with single-ended input audio source (Ci = 100 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, RI = 8 Ω, Ton = GND)

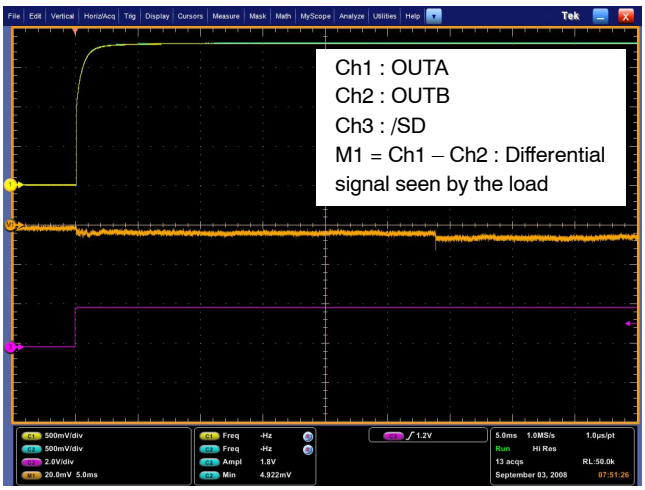


Figure 29. Zero pop noise turn on sequence with differential input to ground (Ci = 100 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = GND)

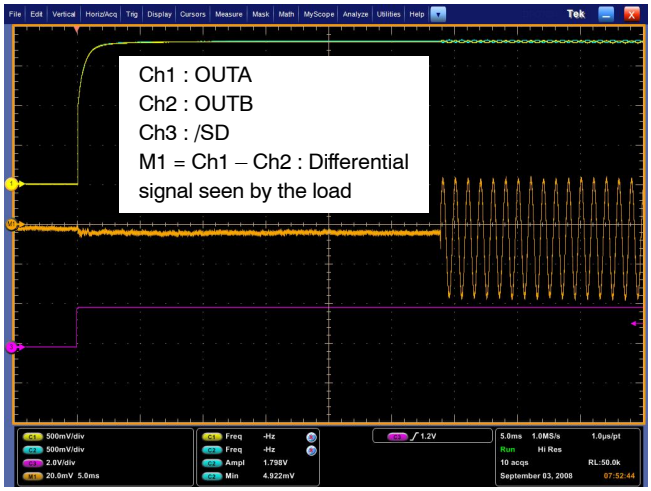


Figure 30. Zero pop noise turn on sequence with differential input audio source (Ci = 100 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = GND)

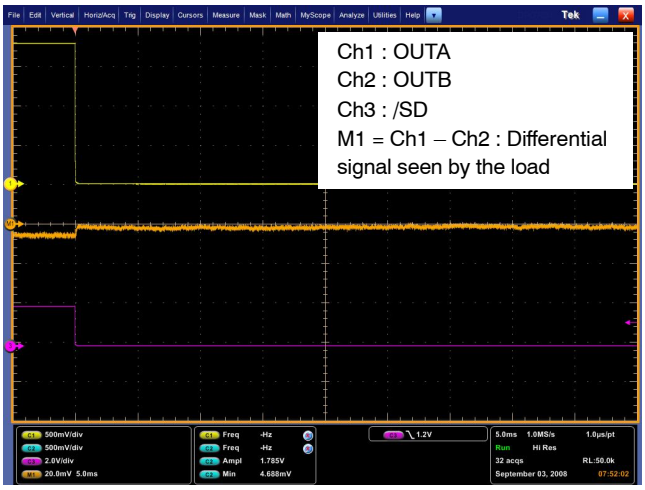


Figure 31. Zero pop noise turn off sequence with differential input to ground (Ci = 100 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = GND)

Figure 32. Zero pop noise turn off sequence with differential input audio source (Ci = 100 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = GND)

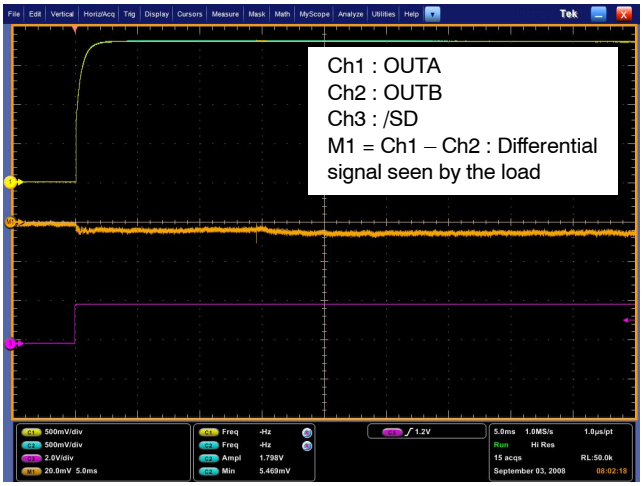


Figure 33. Zero pop noise turn on sequence with single-ended input to ground (Ci = 47 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = Vp)

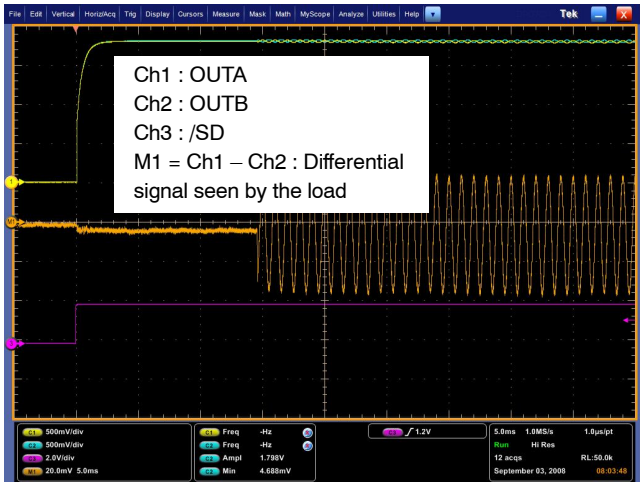


Figure 34. Zero pop noise turn on sequence with single-ended input audio source (Ci = 47 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = Vp)

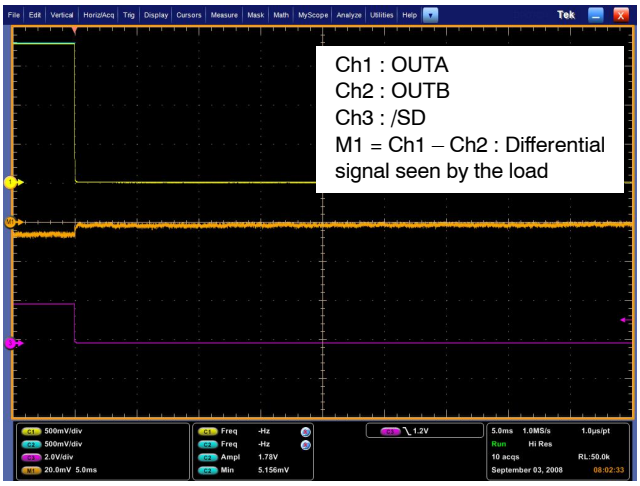


Figure 35. Zero pop noise turn off sequence with single-ended input to ground (Ci = 47 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = Vp)

Figure 36. Zero pop noise turn off sequence with single-ended input audio source (Ci = 47 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = Vp)

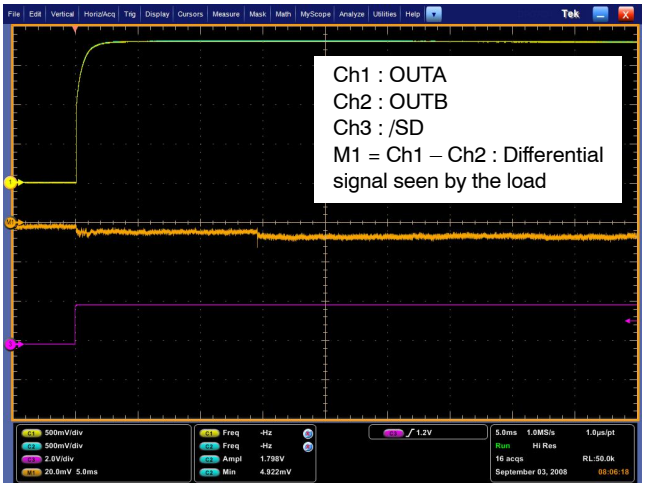


Figure 37. Zero pop noise turn on sequence with differential input to ground (Ci = 47 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = Vp)

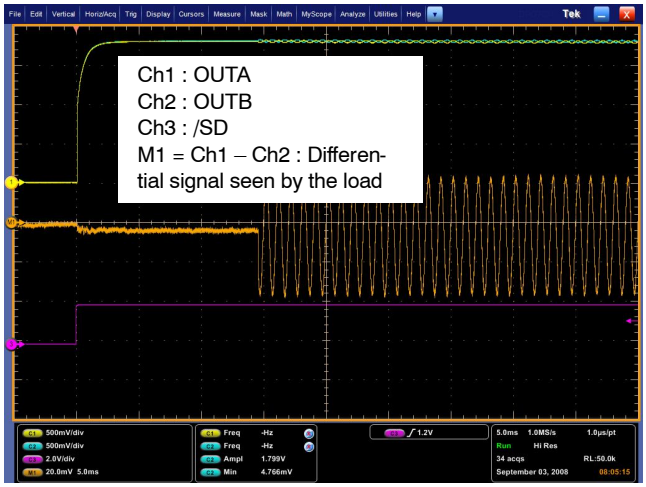


Figure 38. Zero pop noise turn on sequence with differential input audio source (Ci = 47 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = Vp)

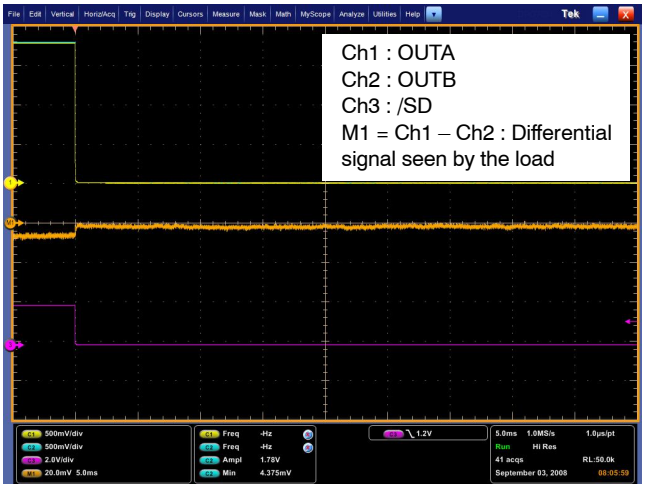


Figure 39. Zero pop noise turn off sequence with differential input to ground (Ci = 47 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = Vp)

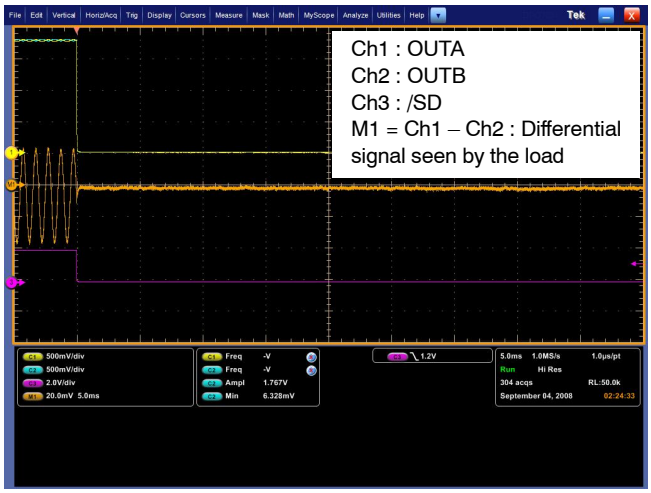


Figure 40. Zero pop noise turn off sequence with differential input audio source (Ci = 47 nF, Ri = 24 kΩ, Rf = 24 kΩ, Cbyp = 1 μF, Rl = 8 Ω, Ton = Vp)

APPLICATION INFORMATION

Detailed Description

The NCP2991 audio amplifier can operate under 2.5 V until 5.5 V power supply. With less than 1% THD + N, it can deliver up to 1.35 W RMS output power to an 8.0 Ω load (V_P = 5.0 V). If application allows to reach 10% THD + N, then 1.65 W can be provided using a 5.0 V power supply.

The structure of the NCP2991 is basically composed of two identical internal power amplifiers; the first one is externally configurable with gain−setting resistors R_{in} and R_f (the closed−loop gain is fixed by the ratios of these resistors) and the second is internally fixed in an inverting unity−gain configuration by two resistors of 20 kΩ. So the load is driven differentially through OUTA and OUTB outputs. This configuration eliminates the need for an output coupling capacitor.

Internal Power Amplifier

The output PMOS and NMOS transistors of the amplifier were designed to deliver the output power of the specifications without clipping. The channel resistance (R_{on}) of the NMOS and PMOS transistors does not exceed 0.6 Ω when they drive current.

The structure of the internal power amplifier is composed of three symmetrical gain stages, first and medium gain stages are transconductance gain stages to obtain maximum bandwidth and DC gain.

Turn−On and Turn−Off Transitions

When a shutdown low level is applied, the output level is tied to Ground on each output after 10 μs.

With T_{ON} = GND, turn on time is set to 30 ms. With T_{ON} = V_P, turn on time is set to 15 ms. To avoid any pop and click noises, $R_{in} * C_{in}$ < 2.4 ms with T_{ON} = GND and $R_{in} * C_{in}$ < 1.2 ms with T_{ON} = Vp. The electrical characteristics are identical with the 2 configurations. This fast turn on time added to a very low shutdown current saves battery life and brings flexibility when designing the audio section of the final application.

NCP2991 is a zero pop noise device when using a single−ended or differential audio input configuration.

Shutdown Function

The device enters shutdown mode when shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 100 nA. In this configuration, the output impedance is 8.5 kΩ on each output.

Current Limit Circuit

The maximum output power of the circuit (P_{orms} = 1.0 W, V_P = 5.0 V, R_L = 8.0 Ω) requires a peak current in the load of 500 mA.

In order to limit the excessive power dissipation in the load when a short−circuit occurs, the current limit in the load is fixed to 1.1 A. The current in the four output MOS transistors are real−time controlled, and when one current exceeds 1.1 A, the gate voltage of the MOS transistor is clipped and no more current can be delivered.

Thermal Overload Protection

Internal amplifiers are switched off when the temperature exceeds 160°C, and will be switched on again only when the temperature decreases fewer than 140°C.

The NCP2991 is unity−gain stable and requires no external components besides gain−setting resistors, an input coupling capacitor and a proper bypassing capacitor in the typical application.

The first amplifier is externally configurable (R_f and R_{in}), while the second is fixed in an inverting unity gain configuration.

The differential−ended amplifier presents two major advantages:

- The possible output power is four times larger (the output swing is doubled) as compared to a single−ended amplifier under the same conditions.
- Output pins (OUTA and OUTB) are biased at the same potential $V_P/2$, this eliminates the need for an output coupling capacitor required with a single−ended amplifier configuration.

The differential closed loop−gain of the amplifier is given by $A_{vd} = 2 * \frac{R_f}{R_{in}} = \frac{V_{orms}}{V_{inrms}}$.

Output power delivered to the load is given by $P_{orms} = \frac{(Vopeak)^2}{2 * R_L}$ (V_{opeak} is the peak differential output voltage).

When choosing gain configuration to obtain the desired output power, check that the amplifier is not current limited or clipped.

The maximum current which can be delivered to the load is 500 mA $I_{opeak} = \frac{V_{opeak}}{R_L}$.

Gain−Setting Resistor Selection (R_{in} and R_f)

R_{in} and R_f set the closed−loop gain of the amplifier.

In order to optimize device and system performance, the NCP2991 should be used in low gain configurations.

The low gain configuration minimizes THD + noise values and maximizes the signal to noise ratio, and the amplifier can still be used without running into the bandwidth limitations.

A closed loop gain in the range from 2 to 5 is recommended to optimize overall system performance.

An input resistor (R_{in}) value of 24 kΩ is realistic in most of applications, and doesn't require the use of a too large capacitor C_{in}.

Input Capacitor Selection (C_{in})

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a

high−pass filter with R_{in}, the cut−off frequency is given by $fc = \frac{1}{2 * \Pi * R_{in} * C_{in}}$.

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation.

IEC 61000-4-2 Level 4

In some particular applications, NCP2991 may need extra ESD protection to pass IEC 61000-4-2 Level 4 qualification.

Depending on the test, user can consider different level of protection:

- up to 22 pF capacitor connected between each amplifier output terminals and ground.
- Dedicated IEC filters such as ESD7.0 series from ON Semiconductor.

In any case, the protection should be placed as close as possible to the ESD stress entry point. Proper and carefull layout is a key factor to ensure optimum protection level is achieved. Designer should make sure the connection impedance between protection and ground / protection and NCP2991 is as low as possible.

ORDERING INFORMATION

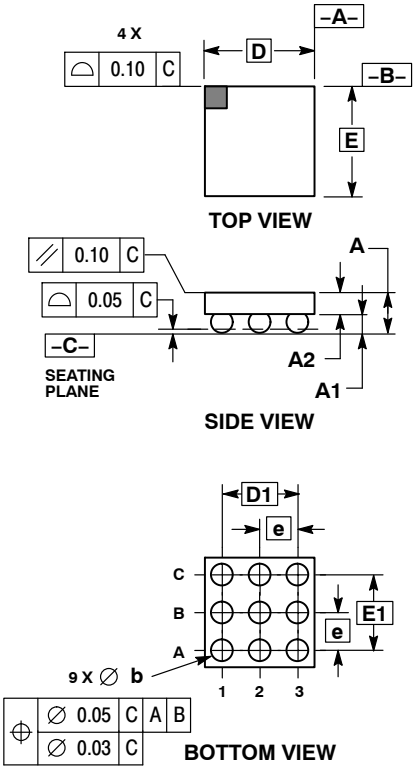
Device	Package	Shipping†
NCP2991FCT2G	9−Pin Flip−Chip (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

9 PIN FLIP−CHIP
CASE 499E−01
ISSUE A

DATE 30 JUN 2004

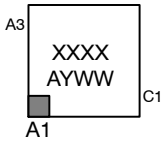
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**9 PIN FLIP−CHIP, 1.45 X 1.45 MM**	**PAGE 1 OF 1**

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