

MJE5740, MJE5742

NPN Silicon Power Darlington Transistors

The MJE5740 and MJE5742 Darlington transistors are designed for high-voltage power switching in inductive circuits.

Features

- These Devices are Pb-Free and are RoHS Compliant*

Applications

- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-------------------|-------------|--------------------------|
| Collector-Emitter Voltage MJE5740 MJE5742 | $V_{CEO(sus)}$ | 300 400 | Vdc |
| Collector-Emitter Voltage MJE5740 MJE5742 | V_{CEV} | 600 800 | Vdc |
| Emitter-Base Voltage | V_{EB} | 8 | Vdc |
| Collector Current – Continuous – Peak (Note 1) | I_C I_{CM} | 8 16 | Adc |
| Base Current – Continuous – Peak (Note 1) | I_B I_{BM} | 2.5 5 | Adc |
| Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 2 0.016 | W W/ $^\circ\text{C}$ |
| Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 100 0.8 | W W/ $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -65 to +150 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristics | Symbol | Max | Unit |
|---|-----------------|------|--------------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 1.25 | $^\circ\text{C/W}$ |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 62.5 | $^\circ\text{C/W}$ |
| Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds | T_L | 275 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

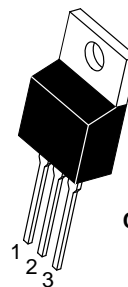
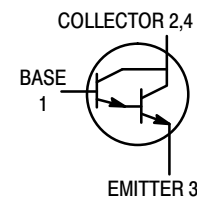
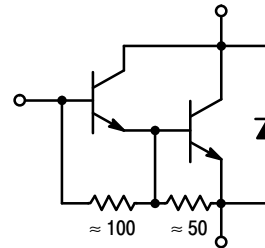
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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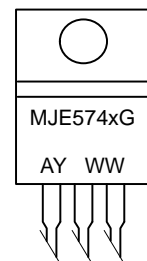
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**POWER DARLINGTON
TRANSISTORS
8 AMPERES
300-400 VOLTS
80 WATTS**



TO-220AB
CASE 221A-09
STYLE 1

MARKING DIAGRAM



MJE574x = Device Code
x = 0 or 2
G = Pb-Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit | |
|---|--------------------|-----------------------|------------|--------|--------|------|
| OFF CHARACTERISTICS (Note 2) | | | | | | |
| Collector–Emitter Sustaining Voltage (I _C = 50 mA, I _B = 0) | MJE5740 MJE5742 | V _{CEO(sus)} | 300 400 | – – | – – | Vdc |
| Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C) | | I _{CEV} | – – | – – | 1 5 | mAdc |
| Emitter Cutoff Current (V _{EB} = 8 Vdc, I _C = 0) | | I _{EBO} | – | – | 75 | mAdc |

SECOND BREAKDOWN

| | | |
|---|------------------|--------------|
| Second Breakdown Collector Current with Base Forward Biased | I _{S/b} | See Figure 6 |
| Clamped Inductive SOA with Base Reverse Biased | RBSOA | See Figure 7 |

ON CHARACTERISTICS

 (Note 2)

| | | | | | |
|---|----------------------|-------------|-------------|-------------------|--------|
| DC Current Gain (I _C = 0.5 Adc, V _{CE} = 5 Vdc) (I _C = 4 Adc, V _{CE} = 5 Vdc) | h _{FE} | 50 200 | 100 400 | – – | – – |
| Collector–Emitter Saturation Voltage (I _C = 4 Adc, I _B = 0.2 Adc) (I _C = 8 Adc, I _B = 0.4 Adc) (I _C = 4 Adc, I _B = 0.2 Adc, T _C = 100°C) | V _{CE(sat)} | – – – | – – – | 2 3 2.2 | Vdc |
| Base–Emitter Saturation Voltage (I _C = 4 Adc, I _B = 0.2 Adc) (I _C = 8 Adc, I _B = 0.4 Adc) (I _C = 4 Adc, I _B = 0.2 Adc, T _C = 100°C) | V _{BE(sat)} | – – – | – – – | 2.5 3.5 2.4 | Vdc |
| Diode Forward Voltage (Note 3) (I _F = 5 Adc) | V _f | – | – | 2.5 | Vdc |

SWITCHING CHARACTERISTICS

| Typical Resistive Load (Table 1) | | | | | | |
|-----------------------------------|---|-----------------|---|------|---|----|
| Delay Time | (V _{CC} = 250 Vdc, I _{C(pk)} = 6 A I _{B1} = I _{B2} = 0.25 A, t _p = 25 μs, Duty Cycle ≤ 1%) | t _d | – | 0.04 | – | μs |
| Rise Time | | t _r | – | 0.5 | – | μs |
| Storage Time | | t _s | – | 8 | – | μs |
| Fall Time | | t _f | – | 2 | – | μs |
| Inductive Load, Clamped (Table 1) | | | | | | |
| Voltage Storage Time | (I _{C(pk)} = 6 A, V _{CE(pk)} = 250 Vdc I _{B1} = 0.06 A, V _{BE(off)} = 5 Vdc) | t _{sv} | – | 4 | – | μs |
| Crossover Time | | t _c | – | 2 | – | μs |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width 300 μs, Duty Cycle = 2%.

3. The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

ORDERING INFORMATION

| Device | Package | Shipping |
|----------|---------------------|-----------------|
| MJE5740G | TO–220 (Pb–Free) | 50 Units / Rail |
| MJE5742G | TO–220 (Pb–Free) | |

TYPICAL CHARACTERISTICS

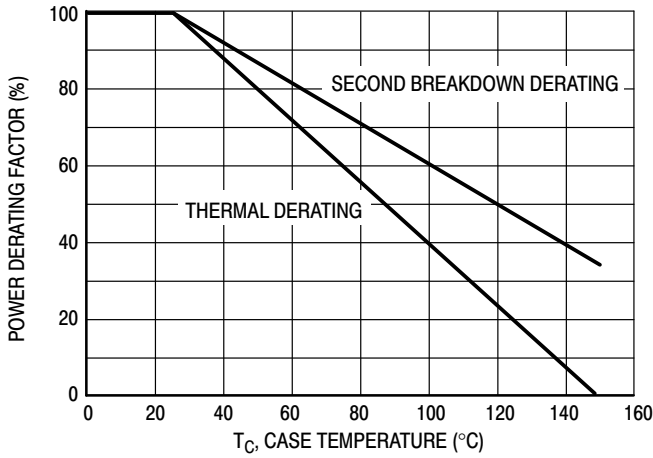


Figure 1. Power Derating

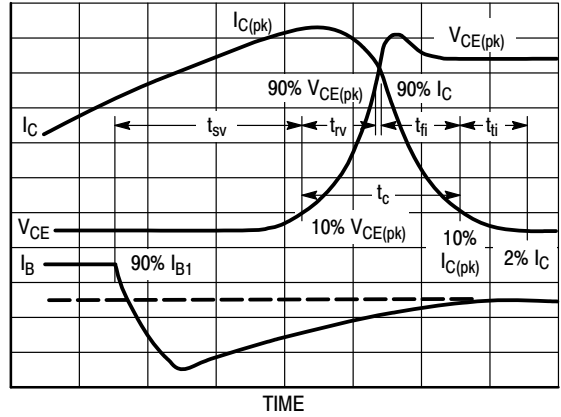


Figure 2. Inductive Switching Measurements

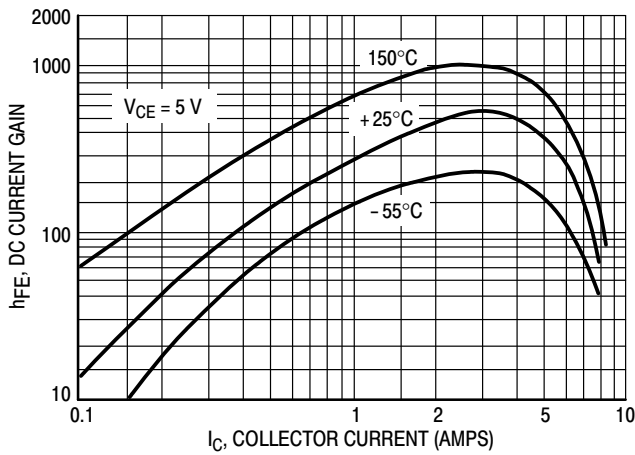


Figure 3. DC Current Gain

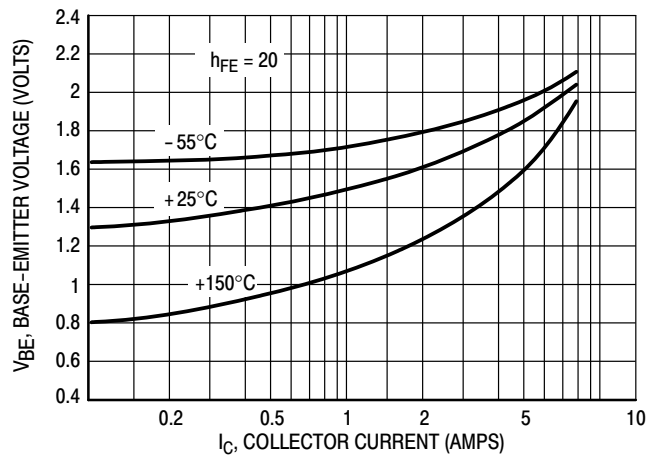


Figure 4. Base-Emitter Voltage

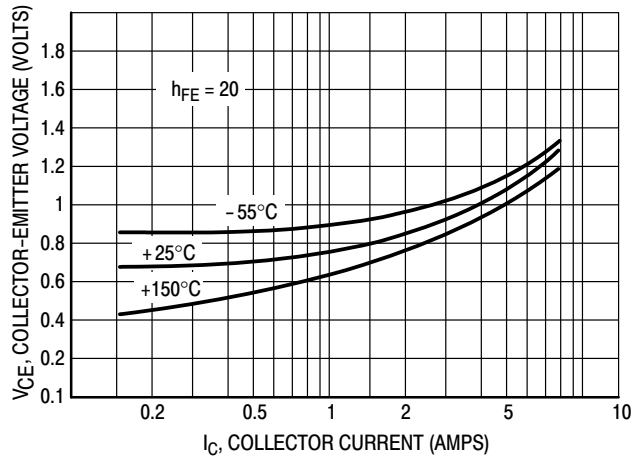


Figure 5. Collector-Emitter Saturation Voltage

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Table 1. Test Conditions for Dynamic Performance

| REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING | | RESISTIVE SWITCHING |
|--|--|--|
| TEST CIRCUITS | <p>DUTY CYCLE \leq 10% $t_r, t_f \leq$ 10 ns</p> <p>NOTE: PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}</p> | |
| CIRCUIT VALUES | <p>COIL DATA: FERROXCUBE CORE #6656 FULL BOBBIN (~16 TURNS) #16</p> <p>GAP FOR 200 μH/20 A $L_{coil} = 200 \mu$H</p> <p>$V_{CC} = 30$ V $V_{CE(pk)} = 250$ Vdc $I_{C(pk)} = 6$ A</p> | <p>$V_{CC} = 250$ V $D1 = 1N5820$ OR EQUIV.</p> |
| TEST WAVEFORMS | <p>OUTPUT WAVEFORMS</p> <p>t_1 ADJUSTED TO OBTAIN I_C</p> $t_1 \approx \frac{L_{coil} (I_{C(pk)})}{V_{CC}}$ <p>TEST EQUIPMENT SCOPE-TEKTRONICS 475 OR EQUIVALENT</p> $t_2 \approx \frac{L_{coil} (I_{C(pk)})}{V_{clamp}}$ | <p>$t_r, t_f < 10$ ns DUTY CYCLE = 1% R_B AND R_C ADJUSTED FOR DESIRED I_B AND I_C</p> |

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SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 1.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives the complete RBSOA characteristics.

The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.

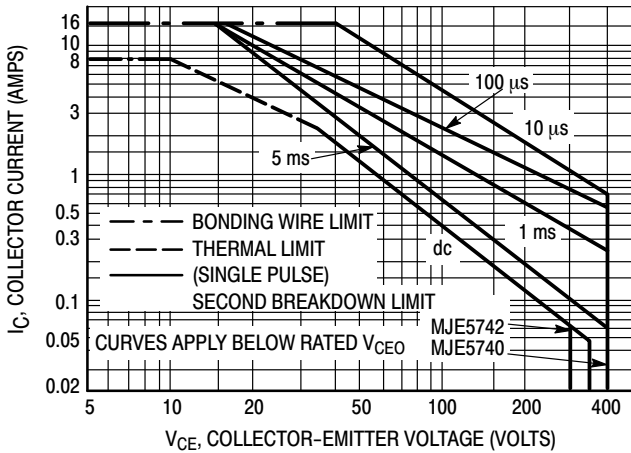


Figure 6. Forward Bias Safe Operating Area

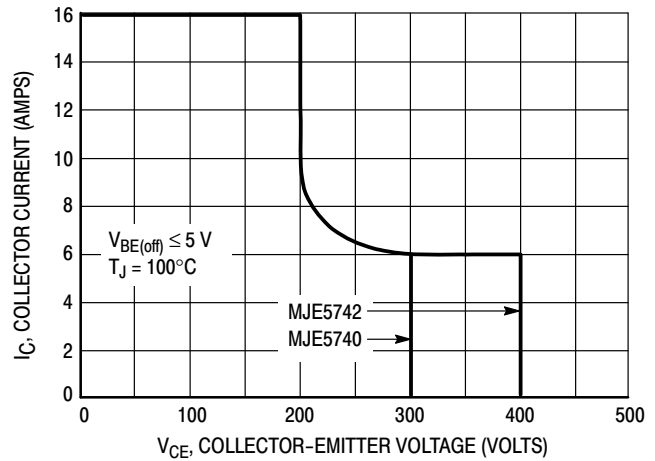


Figure 7. Reverse Bias Safe Operating Area

RESISTIVE SWITCHING PERFORMANCE

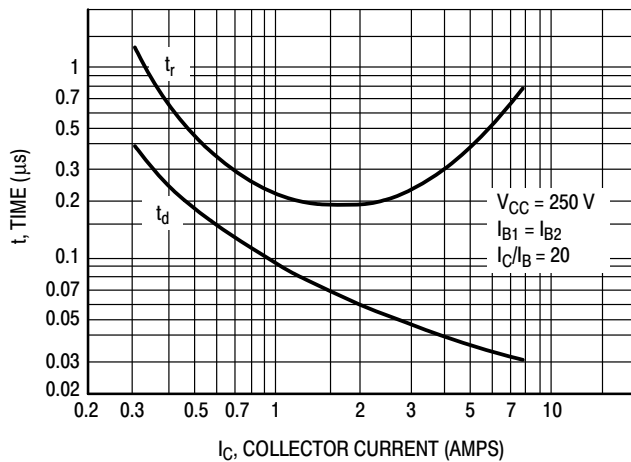


Figure 8. Turn-On Time

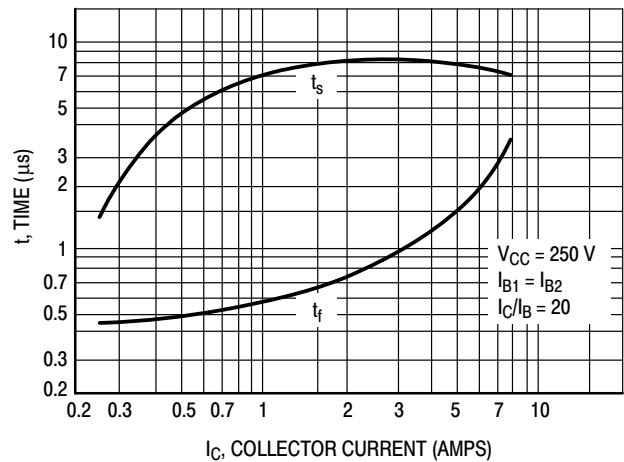


Figure 9. Turn-Off Time

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1



TO-220 CASE 221A ISSUE AK

DATE 13 JAN 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.415 | 9.66 | 10.53 |
| C | 0.160 | 0.190 | 4.07 | 4.83 |
| D | 0.025 | 0.038 | 0.64 | 0.96 |
| F | 0.142 | 0.161 | 3.60 | 4.09 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.161 | 2.80 | 4.10 |
| J | 0.014 | 0.024 | 0.36 | 0.61 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.41 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | --- | 1.15 | --- |
| Z | --- | 0.080 | --- | 2.04 |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

| | | |
|------------------|-------------|--|
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