NTMD5836NL

Power MOSFET

40 V, Dual N−Channel, SOIC−8

Features

- Asymmetrical N Channels
- Low $R_{DS(on)}$
- Low Capacitance
- Optimized Gate Charge
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

	$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max (Notes 1 and 2)
Channel 1	40 V	12 mΩ @ 10 V	11 A
		16 mΩ @ 4.5 V	
Channel 2	40 V	20 mΩ @ 10 V	6.5 A
		36.5 mΩ @ 4.5 V	

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
2. Only selected channel is been powered
   1W applied on channel 1: T_J = 1 W * 85°C/W + 25°C = 110°C

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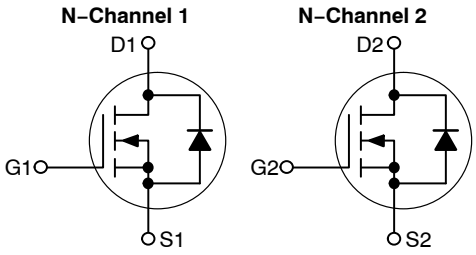
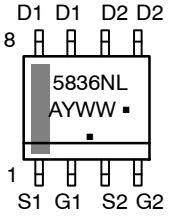


SOIC−8
CASE 751

MARKING DIAGRAM* AND PIN ASSIGNMENT



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMD5836NLR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Ch 1	Ch 2	Unit
Drain−to−Source Voltage			V_{DSS}	40	40	V
Gate−to−Source Voltage			V_{GS}	±20	±20	V
Continuous Drain Current $R_{\theta JA}$ (Notes 3 and 4)	Steady State	T_A = 25°C	I_D	9.0	5.7	A
		T_A = 70°C		7.2	4.6	
Power Dissipation $R_{\theta JA}$ (Notes 3 and 4)		T_A = 25°C	P_D	1.5	1.5	W
		T_A = 70°C		0.9	0.9	
Continuous Drain Current $R_{\theta JA}$ (Notes 3 and 4)	t ≤ 10s	T_A = 25°C	I_D	11	6.5	A
		T_A = 70°C		8.6	4.6	
Power Dissipation $R_{\theta JA}$ (Notes 3 and 4)		T_A = 25°C	P_D	2.1	1.9	W
		T_A = 70°C		1.3	1.2	
Pulsed Drain Current	t_p = 10 μs		I_{DM}	43	26	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150		°C
Source Current (Body Diode)			I_S	10	7.0	A
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 40 V, V_{GS} = 10 V, L = 0.1 mH)			E_{AS}	76	22	mJ
			I_{AS}	39	21	A
Lead Temperature for Soldering Purposes (1/8" from case for 10s)			T_L	260		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
4. Only selected channel is been powered
   1W applied on channel 1: T_J = 1 W * 85°C/W + 25°C = 110°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Ch 1	Ch 2	Unit
Junction−to−Ambient Steady State (Notes 5 and 7)	$R_{\theta JA}$	85	86	°C/W
Junction−to−Ambient − t ≤ 10 s (Notes 5 and 7)	$R_{\theta JA}$	60	65	
Junction−to−Ambient Steady State (Notes 5 and 8)	$R_{\theta JA}$	59		
Junction−to−Ambient Steady State (Notes 6 and 7)	$R_{\theta JA}$	136	136	

5. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
6. Surface−mounted on FR4 board using 0.155 in sq (100 mm^2) pad size
7. Only selected channel is been powered
   1W applied on channel 1: T_J = 1 W * 85°C/W + 25°C = 110°C
8. Both channels receive equivalent power dissipation
   1 W applied on each channel: T_J = 2 W * 59°C/W + 25°C = 143°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Ch	Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		Ch 1	40			V
				Ch 2				
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$ / T_J			Ch 1		146		mV/ °C
				Ch 2		25		
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C	Ch 1			1.0	μA
				Ch 2				
			T_J = 125°C	Ch 1			100	
				Ch 2				
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V		Ch 1			±100	nA
				Ch 2				
ON CHARACTERISTICS (Note 9)								
Gate Threshold Voltage	$V_{GS(TH)}$	VGS = VDS, I_D = 250 μA		Ch 1	1.0	1.8	3.0	V
				Ch 2	1.0	1.8	3.0	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}$ / T_J			Ch 1		6.0		mV/°C
				Ch 2		6.0		
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A		Ch 1		9.5	12	mΩ
		V_{GS} = 10 V, I_D = 7 A		Ch 2		16.2	20	
		V_{GS} = 4.5 V, I_D = 10 A		Ch 1		13	16	mΩ
		V_{GS} = 4.5 V, I_D = 7 A		Ch 2		25.0	36.5	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 10 A		Ch 1		10.5		S
		V_{DS} = 15 V, I_D = 7 A		Ch 2		6.0		
CHARGES, CAPACITANCES & GATE RESISTANCE								
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 20 V		Ch 1		2120		pF
				Ch 2		730		
Output Capacitance	C_{OSS}			Ch 1		315		
				Ch 2		123		
Reverse Transfer Capacitance	C_{RSS}			Ch 1		225		
				Ch 2		84		

9. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
10. Switching characteristics are independent of operating junction temperatures

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Ch	Min	Typ	Max	Unit
CHARGES, CAPACITANCES & GATE RESISTANCE								
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10V, V_{DS} = 20V, I_D = 10A		Ch 1		36	50	nC
		V_{GS} = 10 V, V_{DS} = 20 V, I_D = 7 A		Ch 2		16		
		V_{GS} = 4.5 V, V_{DS} = 20 V, CH1: I_D = 10 A, CH2: I_D = 7 A		Ch 1		15	23	
				Ch 2		8.5	11	
Threshold Gate Charge	$Q_{G(TH)}$			Ch 1		2.4		
				Ch 2		1.0		
Gate−to−Source Charge	Q_{GS}			Ch 1		6.9		
				Ch 2		2.8		
Gate−to−Drain Charge	Q_{GD}			Ch 1		7.2		
				Ch 2		4.0		
Plateau Voltage	V_{GP}			Ch 1		3.2		V
				Ch 2		3.3		
Gate Resistance	R_G			Ch 1		1.2		Ω
				Ch 2		2.1		
SWITCHING CHARACTERISTICS (Note 10)								
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 20 V, CH1: I_D = 10 A, CH2: I_D = 7 A, R_G = 2.5 Ω		Ch 1		16		ns
				Ch 2		11.5		
Rise Time	t_r			Ch 1		22		
				Ch 2		14		
Turn−Off Delay Time	$t_{d(OFF)}$			Ch 1		26		
				Ch 2		15.5		
Fall Time	t_f			Ch 1		8.5		
				Ch 2		3.5		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, CH1: I_D = 10 A, CH2: I_D = 7 A	T_J = 25°C	Ch 1		0.9	1.2	V
				Ch 2		0.85	1.2	
			T_J = 125°C	Ch 1		0.65		
				Ch 2		0.73		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dISD/dt = 100 A/μs, CH1: I_D = 10 A, CH2: I_D = 7 A		Ch 1		27		ns
				Ch 2		17		
Charge Time	T_a			Ch 1		14		
				Ch 2		11		
Discharge Time	T_b			Ch 1		13		
				Ch 2		6.0		
Reverse Recovery Charge	Q_{RR}			Ch 1		19		nC
				Ch 2		9.0		

9. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
10. Switching characteristics are independent of operating junction temperatures

TYPICAL PERFORMANCE CURVES

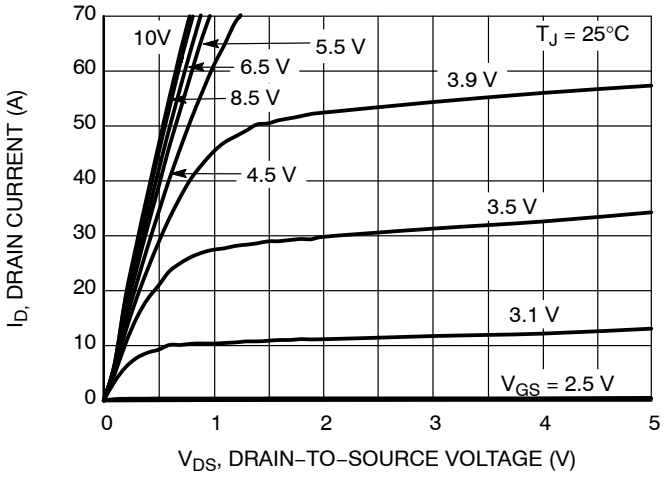


Figure 1. On−Region Characteristics − Channel 1

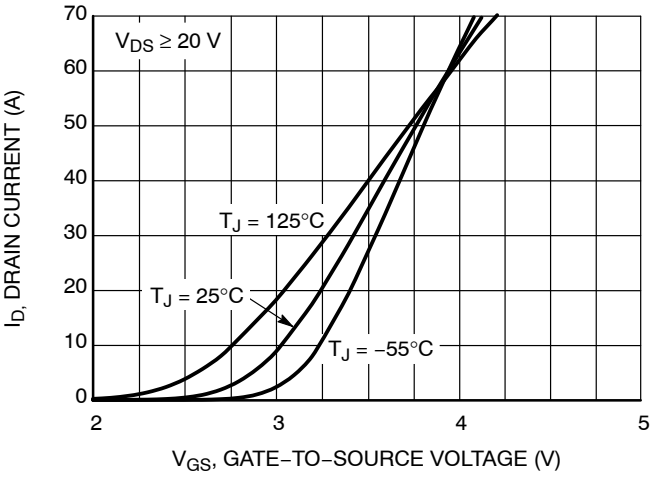


Figure 2. Transfer Characteristics − Channel 1

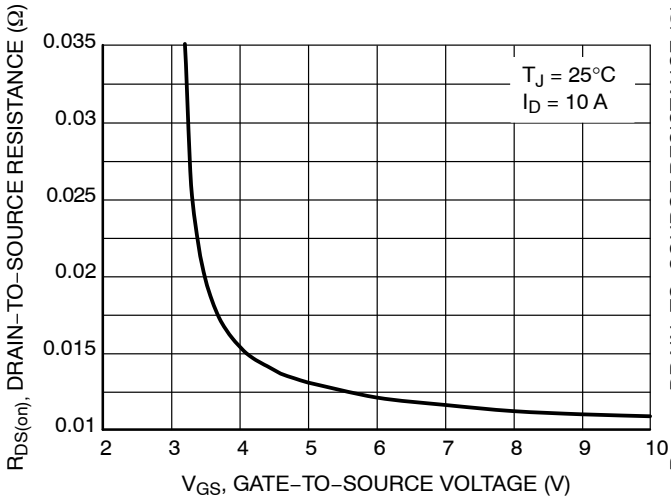


Figure 3. On−Resistance vs. Gate−to−Source Voltage − Channel 1

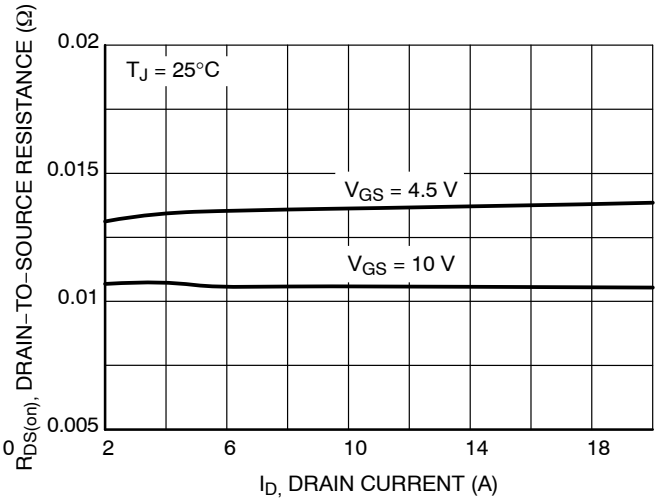


Figure 4. On−Resistance vs. Drain Current and Gate Voltage − Channel 1

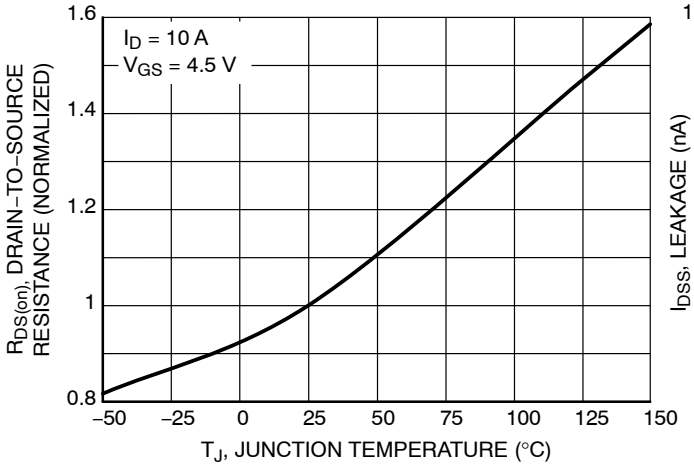


Figure 5. On−Resistance Variation with Temperature − Channel 1

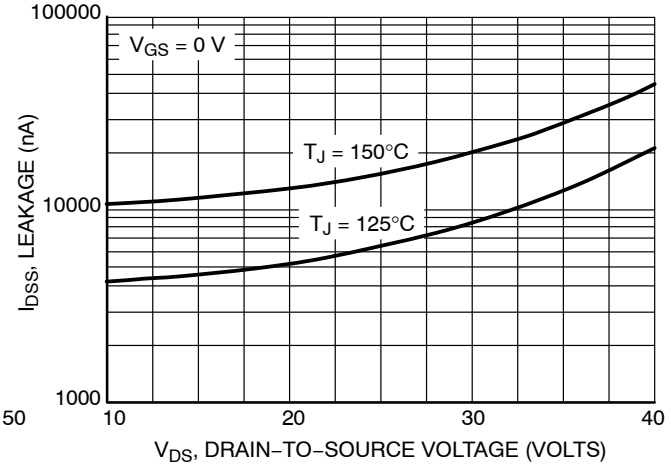


Figure 6. Drain−to−Source Leakage Current vs. Voltage − Channel 1

TYPICAL PERFORMANCE CURVES

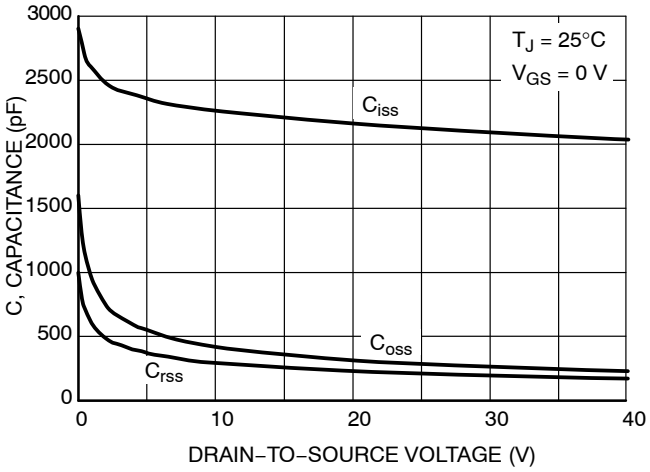


Figure 7. Capacitance Variation − Channel 1

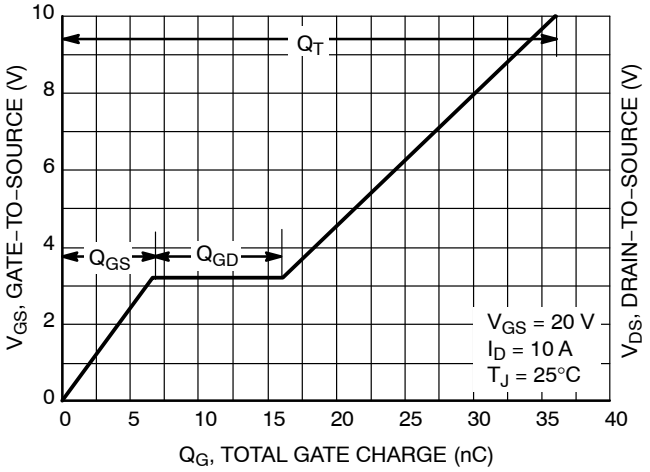


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge − Channel 1

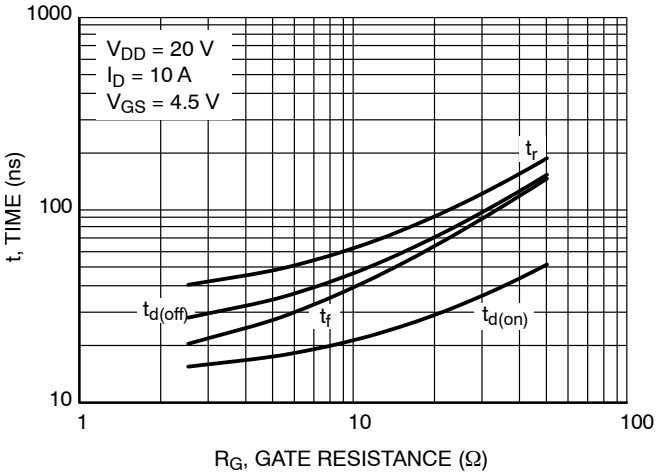


Figure 9. Resistive Switching Time Variation vs. Gate Resistance − Channel 1

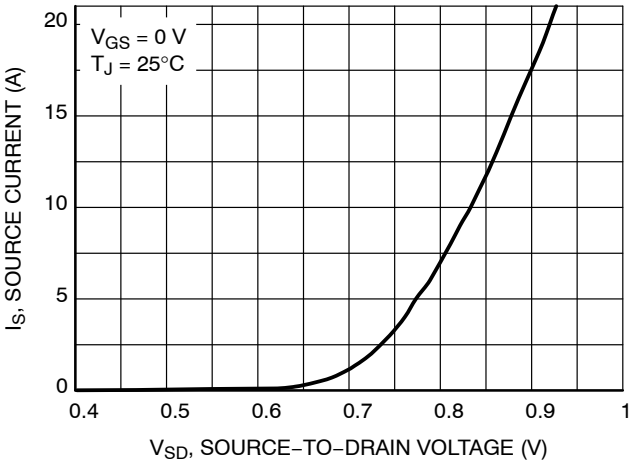


Figure 10. Diode Forward Voltage vs. Current − Channel 1

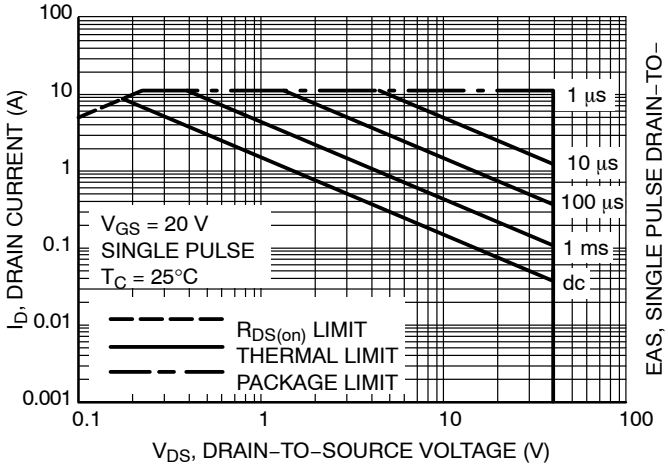


Figure 11. Maximum Rated Forward Biased Safe Operating Area − Channel 1

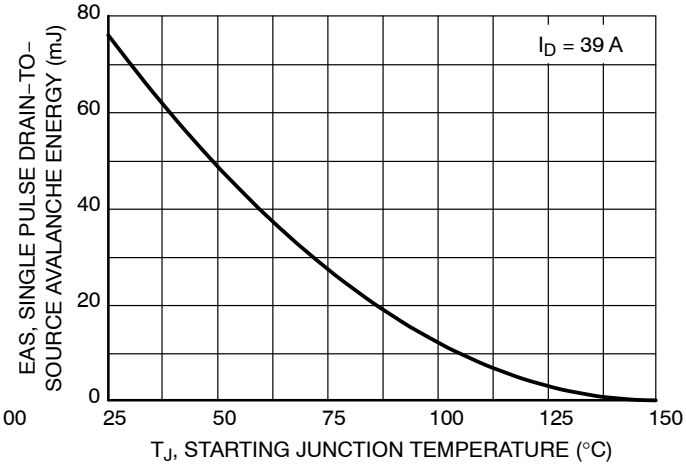


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature − Channel 1

TYPICAL PERFORMANCE CURVES

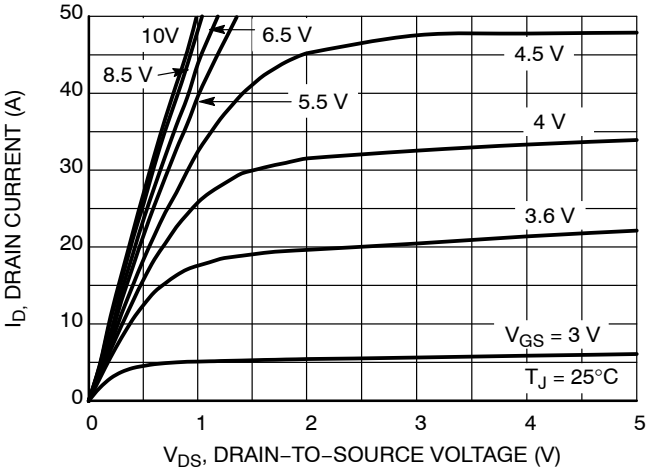


Figure 1. On−Region Characteristics − Channel 2

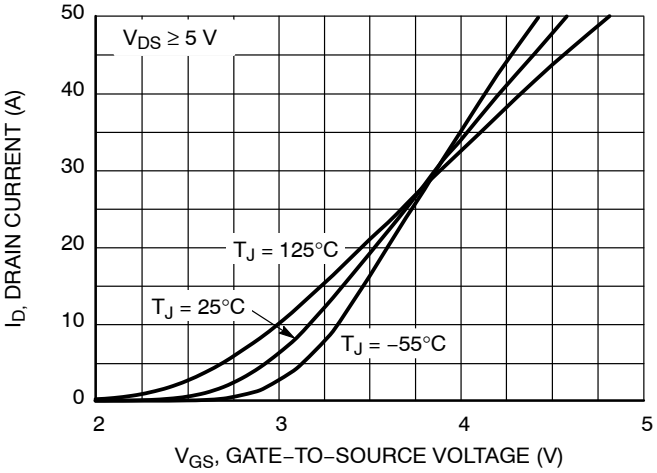


Figure 2. Transfer Characteristics − Channel 2

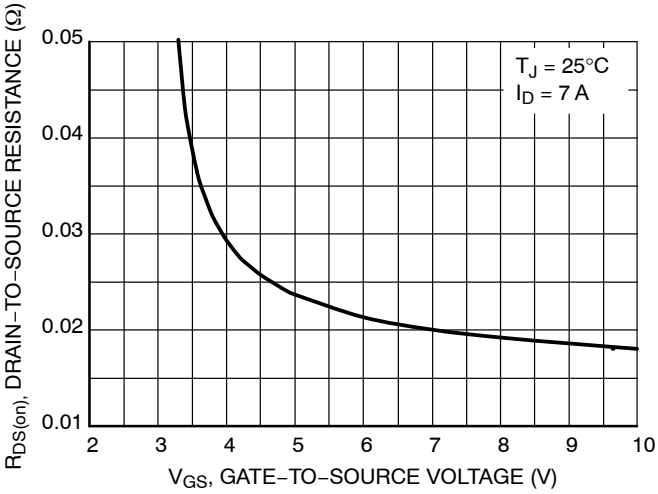


Figure 3. On−Resistance vs. Gate−to−Source Voltage − Channel 2

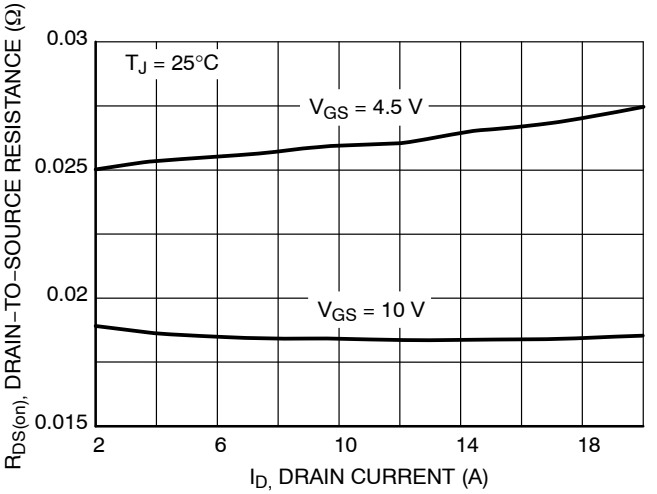


Figure 4. On−Resistance vs. Drain Current and Gate Voltage − Channel 2

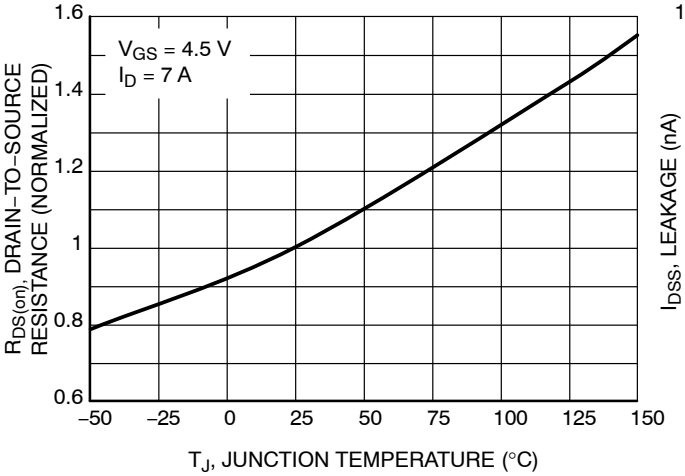


Figure 5. On−Resistance Variation with Temperature − Channel 2

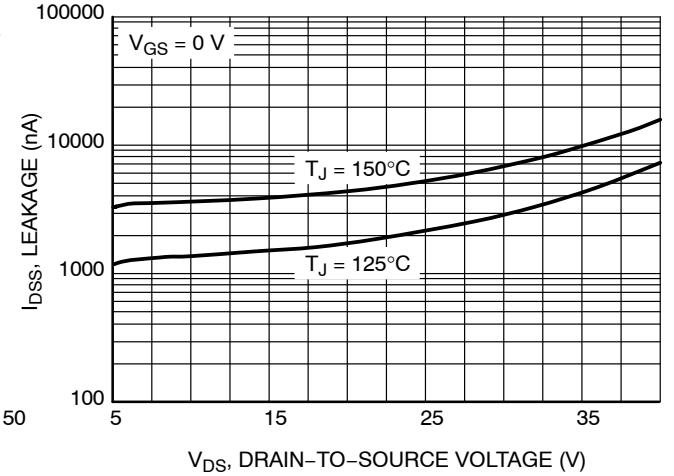


Figure 6. Drain−to−Source Leakage Current vs. Voltage − Channel 2

TYPICAL PERFORMANCE CURVES

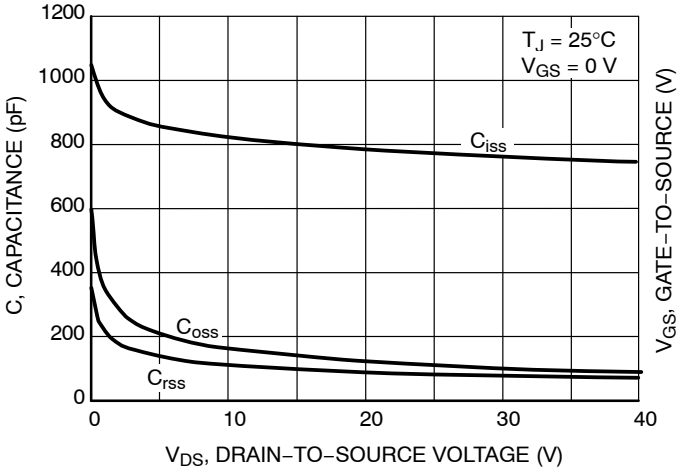


Figure 7. Capacitance Variation − Channel 2

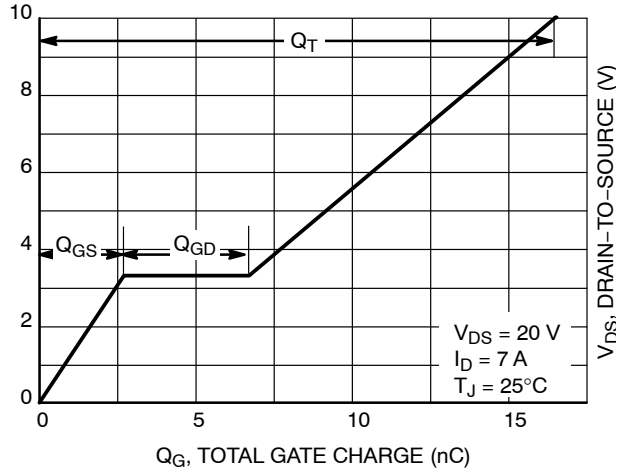


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

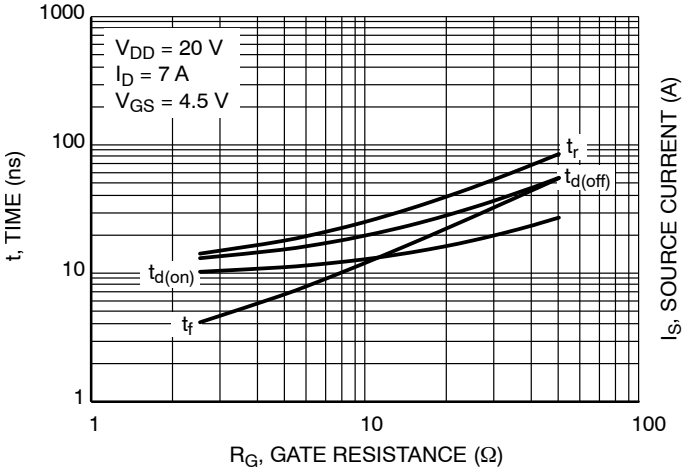


Figure 9. Resistive Switching Time Variation vs. Gate Resistance − Channel 2

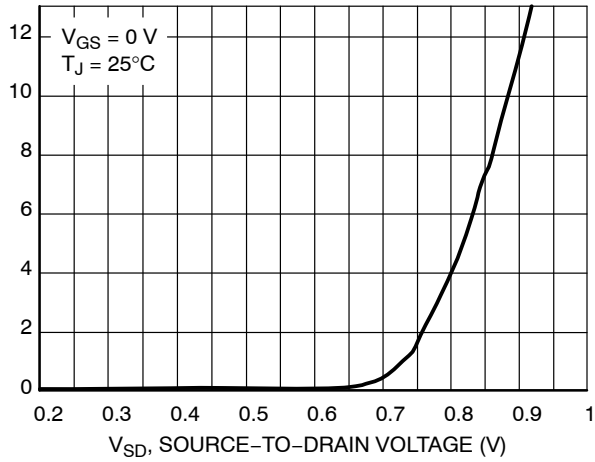


Figure 10. Diode Forward Voltage vs. Current − Channel 2

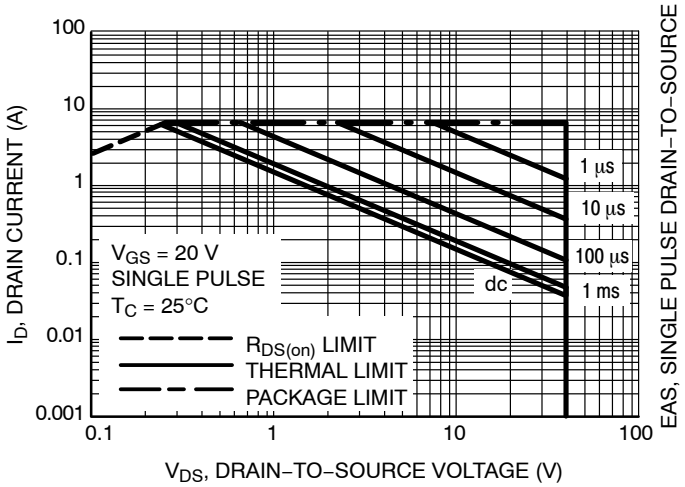


Figure 11. Maximum Rated Forward Biased Safe Operating Area − Channel 2

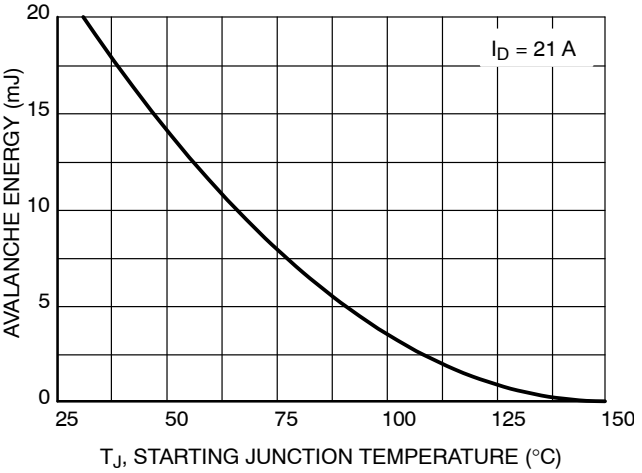


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL PERFORMANCE CURVES

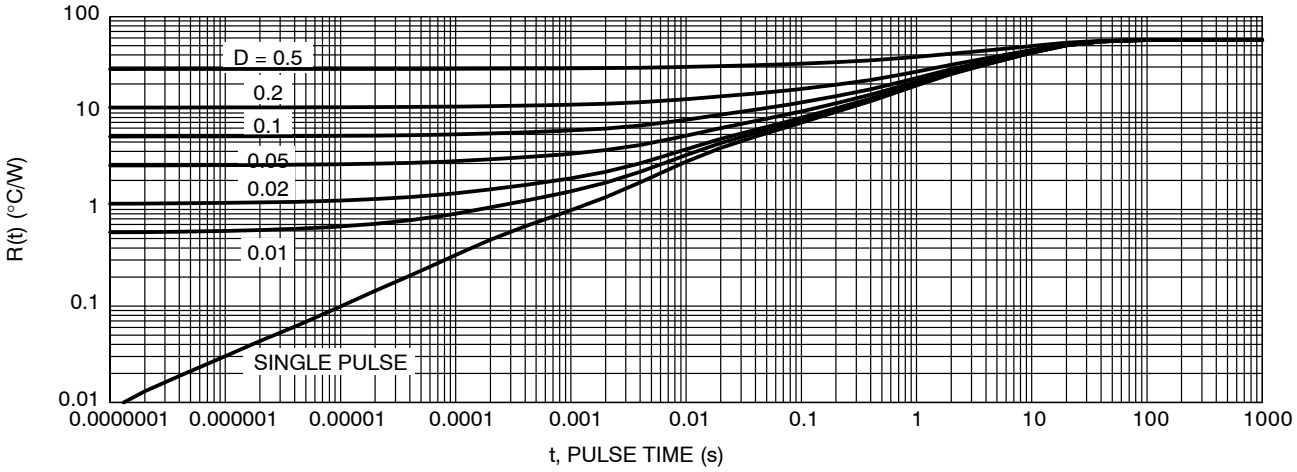


Figure 13. Thermal Response

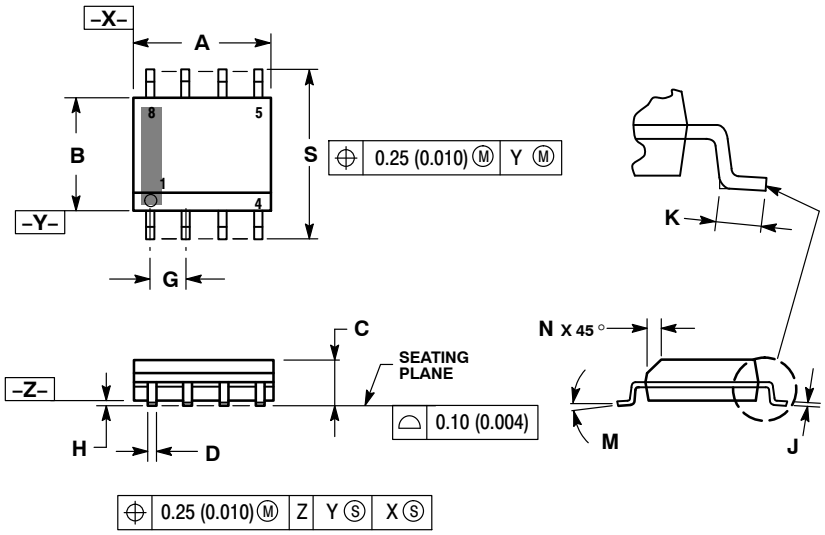
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

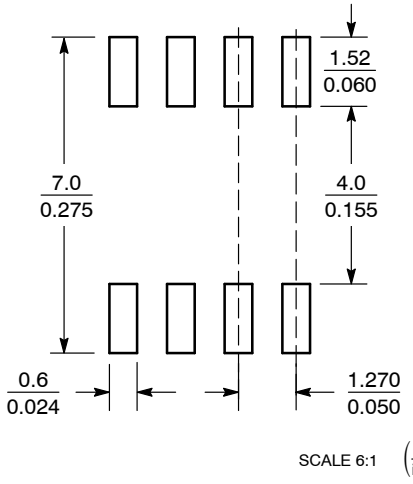
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

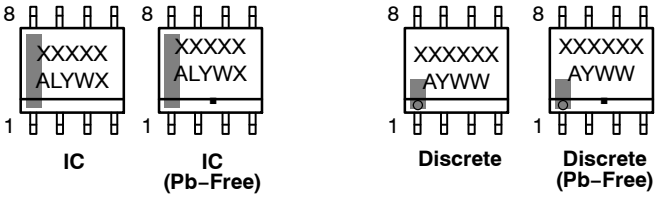
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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