

NTMFS4846N

Power MOSFET

30 V, 100 A, Single N-Channel, SO-8FL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Thermally Enhanced SO8 Package
- These are Pb-Free Devices

Applications

- Refer to Application Note AND8195/D
- CPU Power Delivery
- DC-DC Converters
- Low Side Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DSS}	30	V		
Gate-to-Source Voltage	V_{GS}	± 20	V		
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	20.3	A	
		$T_A = 85^\circ\text{C}$	14.6		
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	$T_A = 25^\circ\text{C}$	2.25	W	
		$T_A = 85^\circ\text{C}$			
Continuous Drain Current $R_{\theta JA} \leq 10$ sec	I_D	$T_A = 25^\circ\text{C}$	32.8	A	
		$T_A = 85^\circ\text{C}$	23.7		
Power Dissipation $R_{\theta JA}, t \leq 10$ sec	P_D	$T_A = 25^\circ\text{C}$	5.90	W	
		$T_A = 85^\circ\text{C}$			
Continuous Drain Current $R_{\theta JA}$ (Note 2)	I_D	$T_A = 25^\circ\text{C}$	12.7	A	
		$T_A = 85^\circ\text{C}$	9.2		
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	$T_A = 25^\circ\text{C}$	0.89	W	
		$T_A = 85^\circ\text{C}$			
Continuous Drain Current $R_{\theta JC}$ (Note 1)	I_D	$T_C = 25^\circ\text{C}$	100	A	
		$T_C = 85^\circ\text{C}$	72		
Power Dissipation $R_{\theta JC}$ (Note 1)	P_D	$T_C = 25^\circ\text{C}$	55.5	W	
		$T_C = 85^\circ\text{C}$			
Pulsed Drain Current	$t_p = 10\mu\text{s}$	$T_A = 25^\circ\text{C}$	I_{DM}	200	A
Current limited by package		$T_A = 25^\circ\text{C}$	$I_{Dmaxpkg}$	100	A
Operating Junction and Storage Temperature	T_J, T_{STG}		-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	55	A		
Drain to Source dV/dt	dV/dt	6	V/ns		
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = 37$ A $_{pk}$, $L = 0.3$ mH, $R_G = 25$ Ω)	EAS	205	mJ		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$		

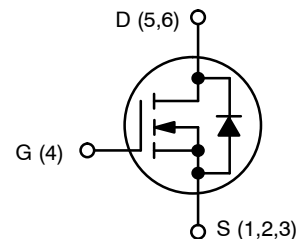
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



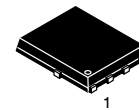
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	3.4 m Ω @ 10 V	100 A
	5.1 m Ω @ 4.5 V	

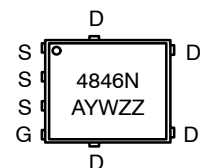


N-CHANNEL MOSFET



SO-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4846NT1G	SO-8FL (Pb-Free)	1500 / Tape & Reel
NTMFS4846NT3G	SO-8FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMFS4846N

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.25	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	55.6	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	140.8	
Junction-to-Ambient – $t \leq 10$ sec	$R_{\theta JA}$	21.2	

- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			25		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.45	1.8	2.5	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.2		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V to } 11.5\text{ V}$	$I_D = 30\text{ A}$		2.5	3.4	m Ω
			$I_D = 15\text{ A}$		2.4		
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$		3.8	5.1	
			$I_D = 15\text{ A}$		3.8		
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 30\text{ A}$		85		S	

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 12\text{ V}$		3250		pF
Output Capacitance	C_{OSS}			562		
Reverse Transfer Capacitance	C_{RSS}			289		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		21.8	32	nC
Threshold Gate Charge	$Q_{G(TH)}$			3.2		
Gate-to-Source Charge	Q_{GS}			8.1		
Gate-to-Drain Charge	Q_{GD}			7.4		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		53		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		18.9		ns
Rise Time	t_r			34		
Turn-Off Delay Time	$t_{d(OFF)}$			24.6		
Fall Time	t_f			9.4		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

NTMFS4846N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 4)						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		10.7		ns
Rise Time	t_r			18.9		
Turn-Off Delay Time	$t_{d(OFF)}$			34.2		
Fall Time	t_f			7.1		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.0	V
			$T_J = 125^\circ\text{C}$		0.66		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$			21.6		ns
Charge Time	t_a				11.4		
Discharge Time	t_b				10.2		
Reverse Recovery Charge	Q_{RR}				8.5		

PACKAGE PARASITIC VALUES

Source Inductance	L_S	$T_A = 25^\circ\text{C}$		0.65		nH
Drain Inductance	L_D			0.005		
Gate Inductance	L_G			1.84		
Gate Resistance	R_G		0.5	1.4	2.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

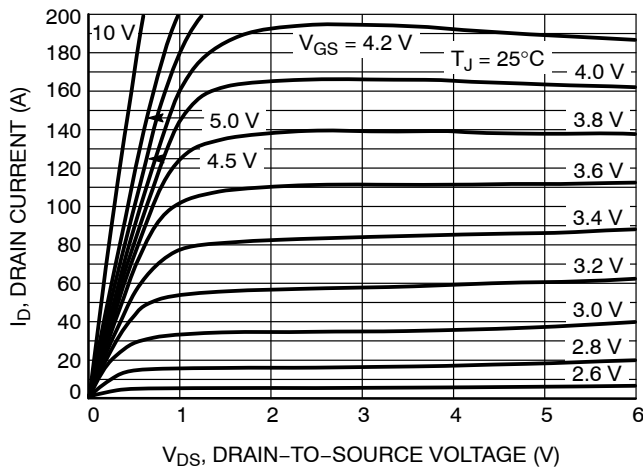


Figure 1. On-Region Characteristics

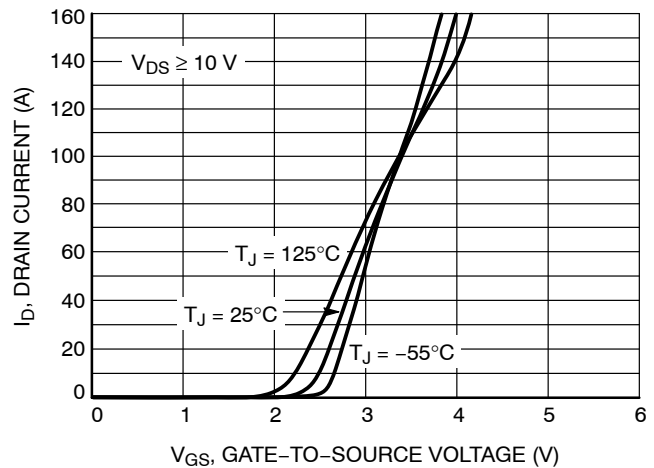


Figure 2. Transfer Characteristics

TYPICAL CHARACTERISTICS

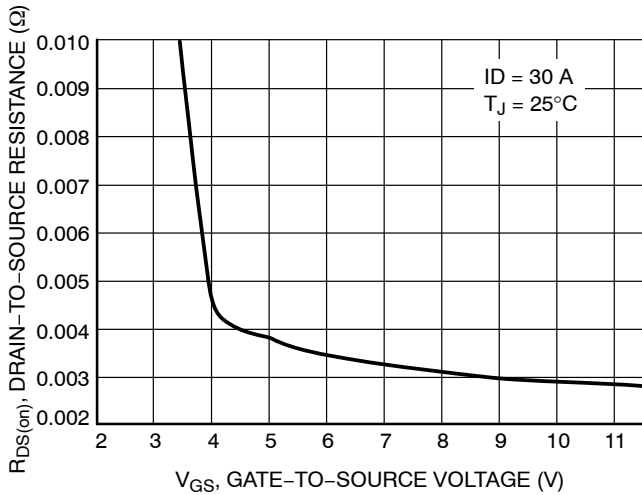


Figure 3. On-Resistance vs. Gate-to-Source Voltage

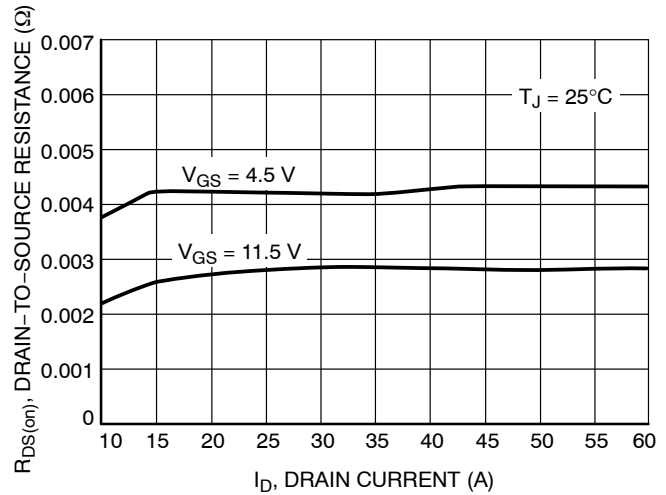


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

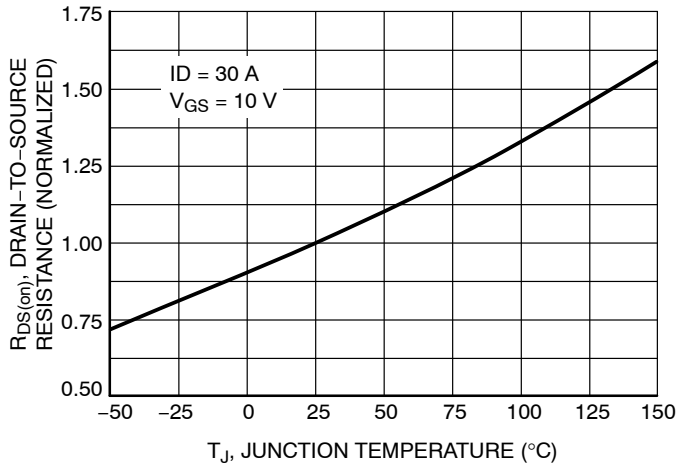


Figure 5. On-Resistance Variation with Temperature

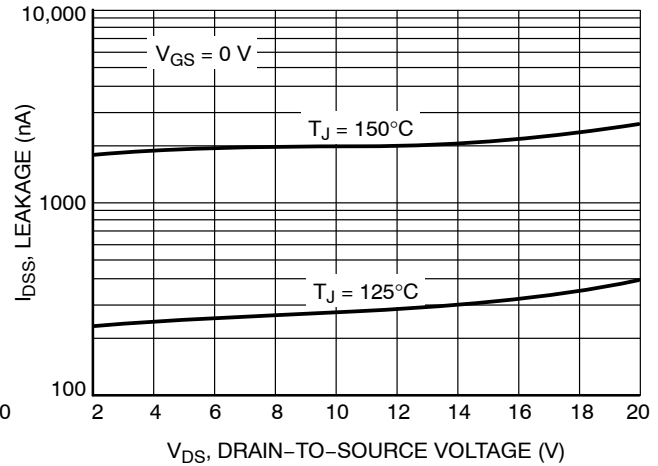


Figure 6. Drain-to-Source Leakage Current vs. Voltage

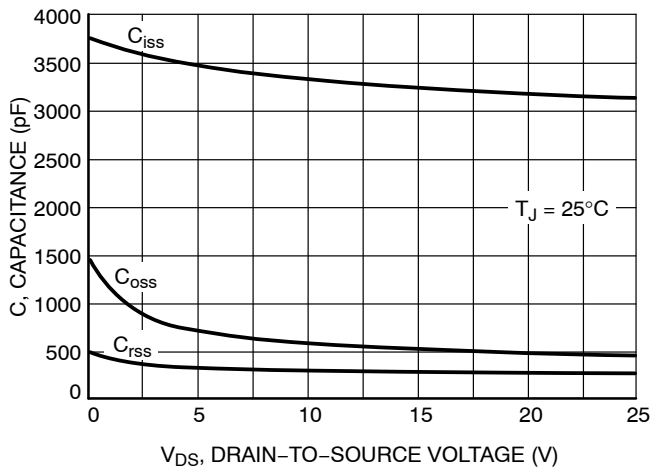


Figure 7. Capacitance Variation

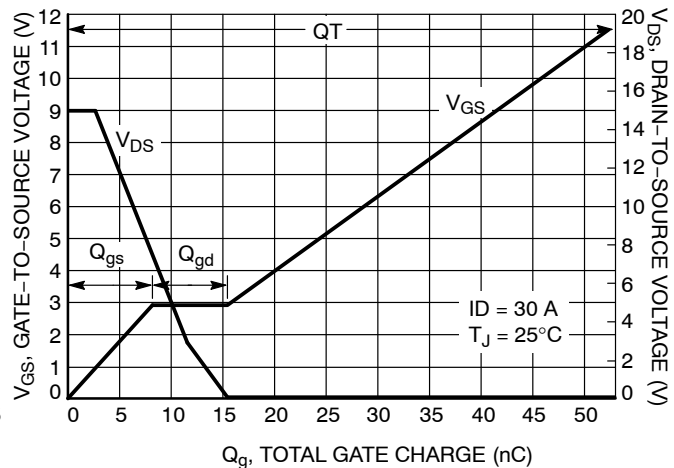


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

TYPICAL CHARACTERISTICS

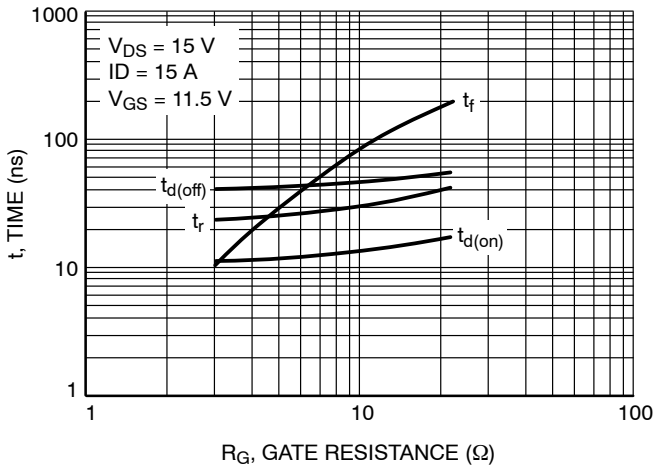


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

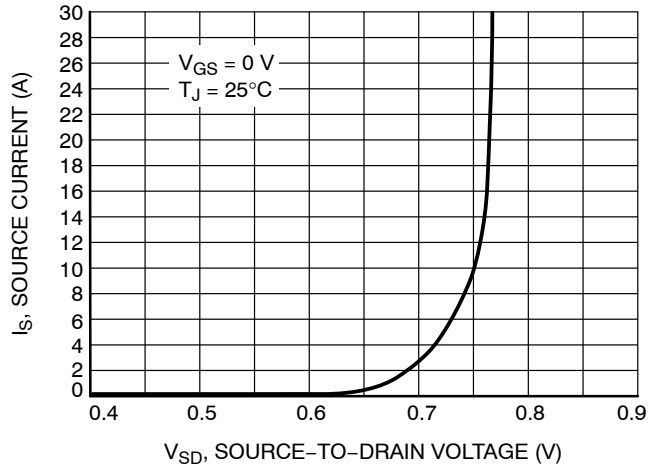


Figure 10. Diode Forward Voltage vs. Current

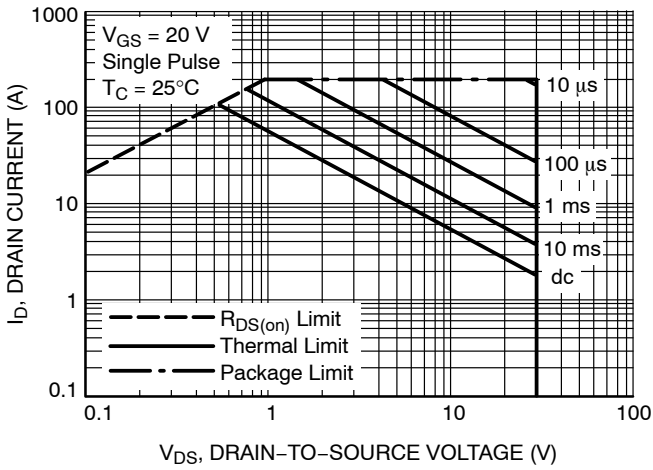


Figure 11. Maximum Rated Forward Biased Safe Operating Area

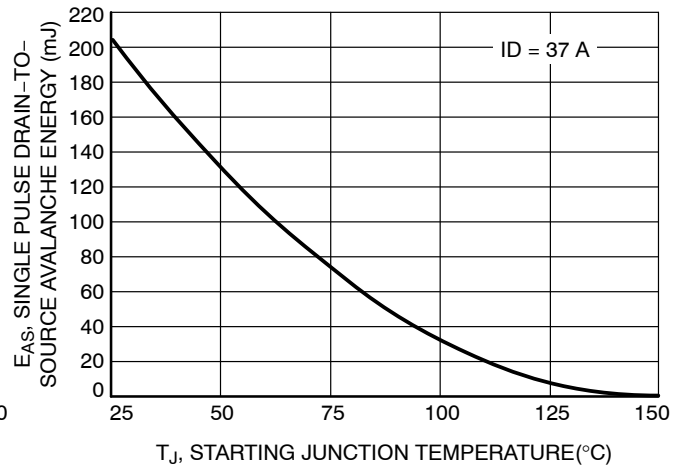


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

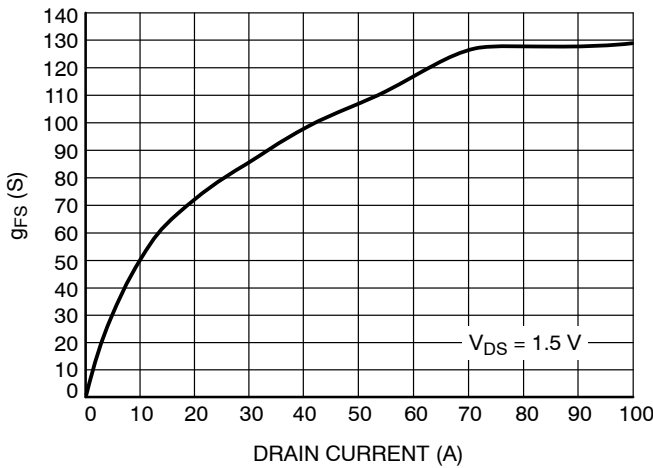


Figure 13. g_{FS} vs. Drain Current

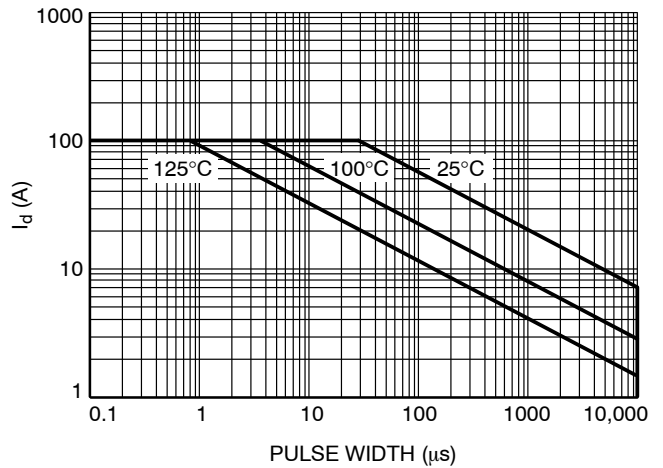


Figure 14. I_d vs. Pulse Width

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

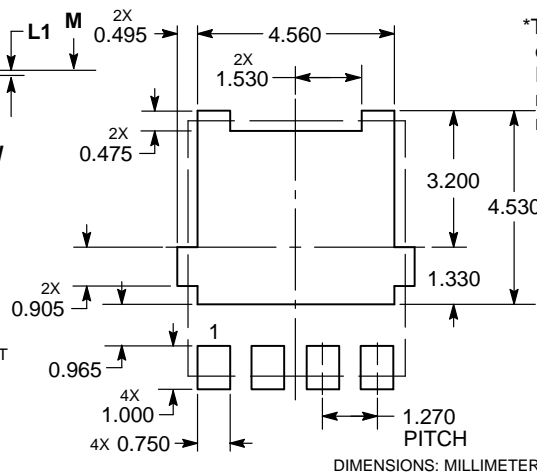
GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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