

# NCP362

## USB Positive Overvoltage and Overcurrent Protection with TVS for $V_{BUS}$ and Low Capacitance ESD Diodes for Data

The NCP362 disconnects systems at its output when wrong  $V_{BUS}$  operating conditions are detected at its input. The system is positive overvoltage protected up to +20 V, overcurrent protected up to 750 mA, and receives protection from ESD diodes for the high speed USB data and  $V_{BUS}$  lines. Thanks to an integrated PMOS FET, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP362 is able to instantaneously disconnect the output from the input if the input voltage exceeds the overvoltage threshold OVLO. Thanks to an overcurrent protection, the integrated PMOS turns off when the charge current exceeds the current limit (see options in ordering information).

The NCP362 provides a negative going flag ( $\overline{FLAG}$ ) output, which alerts the system that voltage, current or overtemperature faults have occurred.

In addition, the device integrates ESD diodes for  $V_{BUS}$  and data lines which are IEC61000-4-2, level 4 compliant. The ESD diodes for D+ and D- are compatible with high speed USB thanks to an ultra low capacitance of 0.5 pF.

### Features

- Overvoltage Protection up to 20 V
- Undervoltage and Overvoltage Lockout (UVLO/OVLO)
- Overcurrent Protection
- Transient Voltage Suppressor for  $V_{BUS}$  Pin
- Ultra Low Capacitance ESD for Data Lines
- Alert  $\overline{FLAG}$  Output and  $\overline{EN}$  Enable Pin
- Thermal Shutdown
- Compliance to IEC61000-4-2 (Level 4)
- Compliance Machine Model and Human Body Model
- 10 Lead UDFN 2x2.5 mm Package
- This is a Pb-Free Device

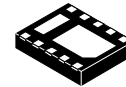
### Applications

- USB Devices
- Mobile Phones
- Peripheral
- Personal Digital Assistant
- MP3/MP4 Players
- TV and Set Top Boxes



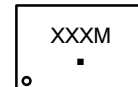
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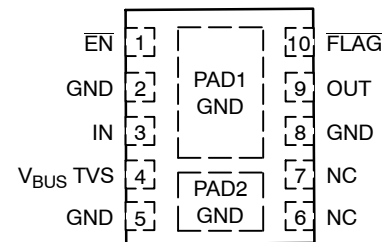
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### MARKING DIAGRAMS

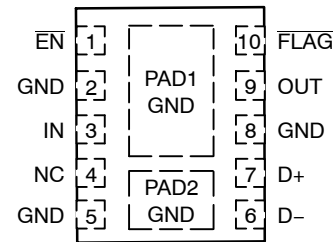


- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

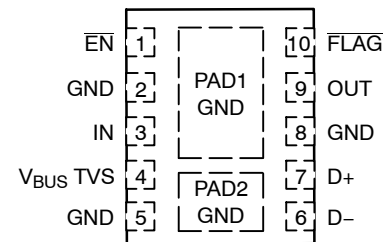
### PIN CONNECTIONS



NCP362A Version  
( $V_{BUS}$  TVS + OVP/OCF)



NCP362B Version  
(D+/- ESD low cap + OVP/OCF)



NCP362C Version  
( $V_{BUS}$  TVS + D+/- ESD low cap + OVP/OCF)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

# NCP362

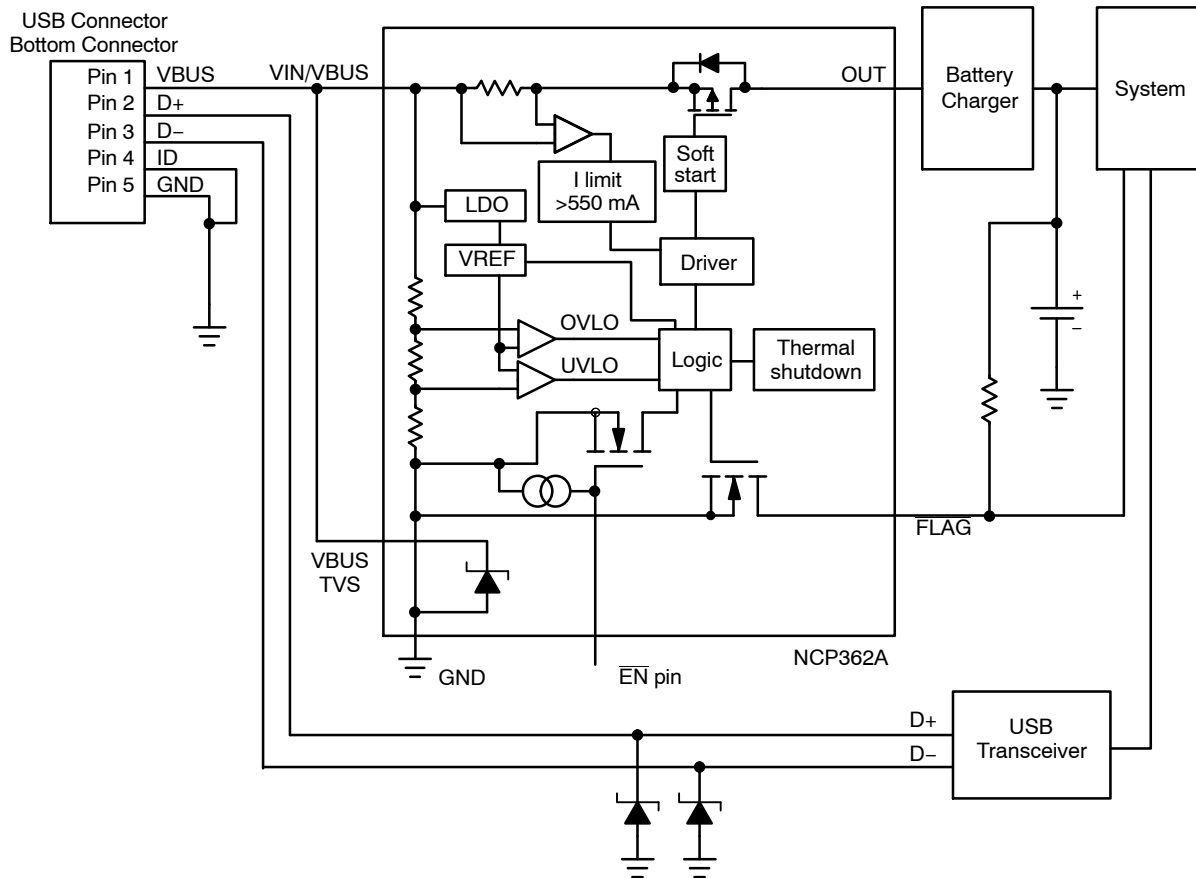


Figure 1. Typical Application Circuit with Wall Adapter /  $V_{BUS}$  TVS Protection (NCP362A)

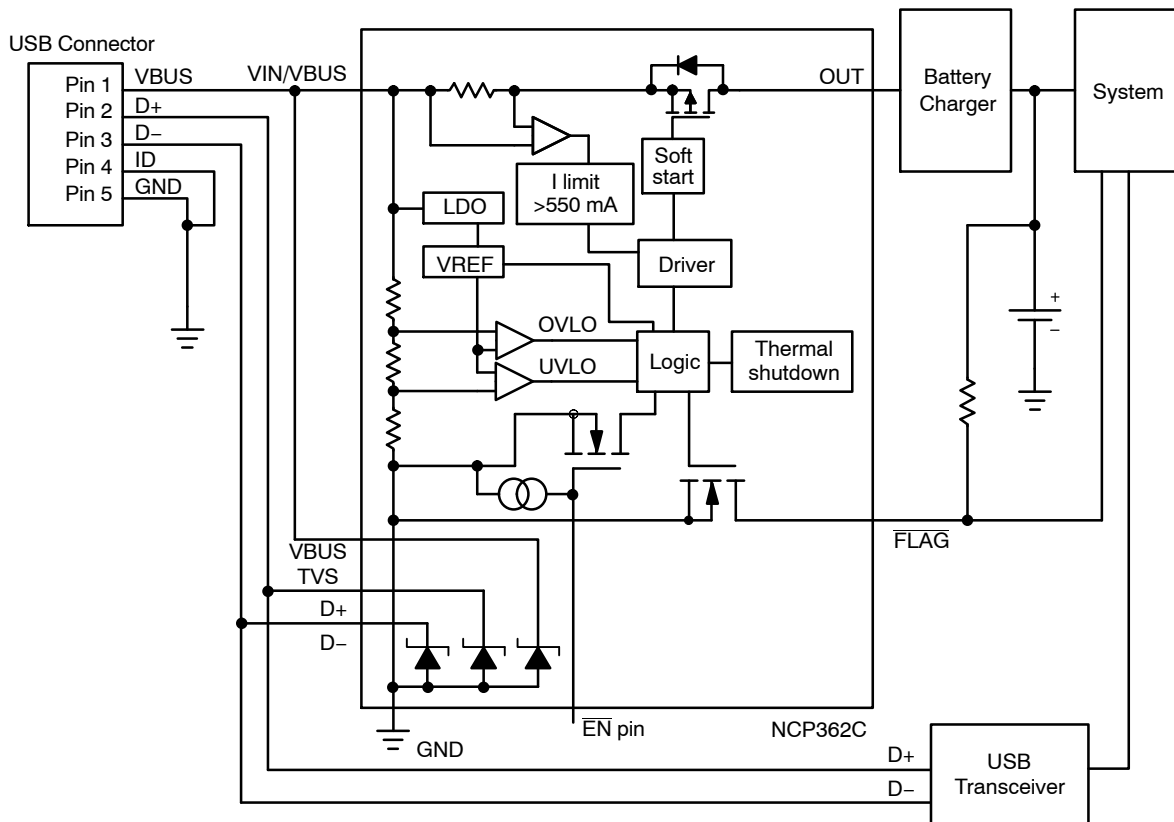


Figure 2. Typical Application Circuit with Full Integrated ESD for USB (NCP362C)

# NCP362

## PIN FUNCTION DESCRIPTION

Pin No.	Name	Type	Description
1	$\overline{EN}$	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin shall be connected to GND or to a I/O pin. This pin does not have an impact on the fault detection.
2	GND	POWER	Ground
3	IN	POWER	Input Voltage Pin. This pin is connected to the $V_{BUS}$ . A 1 $\mu$ F low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
4	$V_{BUS}$ TVS	INPUT	Cathode of the $V_{BUS}$ transient voltage suppressor diode. (NCP362A & NCP362C) This pin is not connected in the NCP362B
5	GND	POWER	Ground
6	D-	INPUT	Cathode of the D- ESD diode. (NCP362B & NCP362C) This pin is not connected in the NCP362A
7	D+	INPUT	Cathode of the D+ ESD diode. (NCP362B & NCP362C) This pin is not connected in the NCP362A
8	GND	POWER	Ground
9	OUT	OUTPUT	Output Voltage Pin. The output is disconnected from the $V_{BUS}$ power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 $\mu$ F capacitor must be connected to this pin. The two OUT pins must be hardwired to common supply.
10	$\overline{FLAG}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on $V_{BUS}$ pin. The $\overline{FLAG}$ pin goes low when input voltage exceeds OVLO threshold. Since the $\overline{FLAG}$ pin is open drain functionality, an external pull up resistor to $V_{CC}$ must be added.
PAD1	GND	POWER	Ground. Must be used for power dissipation. See PCB recommendations.
PAD2	GND	POWER	Anode of the TVS and/or ESD diodes. Must be connected to GND.

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## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage to GND (Pins IN, $\overline{EN}$ , OUT, FLAG)	V <sub>min</sub>	-0.3	V
Maximum Voltage to GND (Pin IN)	V <sub>max,in</sub>	21	V
Maximum Voltage to GND (Pins $\overline{EN}$ , OUT, FLAG)	V <sub>max</sub>	7.0	V
Maximum DC Current from Vin to Vout (PMOS) (Note 1)	I <sub>max</sub>	600	mA
Thermal Resistance, Junction-to-Air	R <sub>θJA</sub>	280	°C/W
Operating Ambient Temperature Range	T <sub>A</sub>	-40 to +85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Junction Operating Temperature	T <sub>J</sub>	150	°C
Human Body Model (HBM) (Note 2) Pins $\overline{EN}$ , IN, OUT, GND V <sub>BUS TVS</sub>		2000 16000	V
Machine Model (MM) (Note 3) Pins $\overline{EN}$ , IN, OUT, GND V <sub>BUS TVS</sub>		200 400	V
IEC 61000-4-2 Pin V <sub>BUS TVS</sub> Contact Air Pins D+ & D- Contact Air	Vesd	30 30 10 15	kV kV kV kV
Forward Voltage @ 10 mA Pin V <sub>BUS TVS</sub> Pins D+ & D-		1.1 1.0	V
Moisture Sensitivity	MSL	Level 1	-

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. With minimum PCB area. By decreasing R<sub>θJA</sub>, the current capability increases. See PCB recommendation page 9.
2. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
3. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

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## ELECTRICAL CHARACTERISTICS

(Min/Max limits values ( $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ ) and  $V_{in} = +5.0\text{ V}$ . Typical values are  $T_A = +25^{\circ}\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{in}$		1.2		20	V
Undervoltage Lockout Threshold	UVLO	$V_{in}$ falls below UVLO threshold	2.85	3.0	3.15	V
Uvoltage Lockout Hysteresis	UVLO <sub>hyst</sub>		50	70	90	mV
Overvoltage Lockout Threshold	OVLO	$V_{in}$ rises above OVLO threshold	5.43	5.675	5.9	V
Overvoltage Lockout Hysteresis	OVLO <sub>hyst</sub>		50	100	125	mV
$V_{in}$ versus $V_{out}$ Dropout	$V_{drop}$	$V_{in} = 5\text{ V}$ , I charge = 500 mA		150	200	mV
Overcurrent Limit	$I_{lim}$	$V_{in} = 5\text{ V}$	550	750	950	mA
Supply Quiescent Current	$I_{dd}$	No Load, $V_{in} = 5.25\text{ V}$		20	35	$\mu\text{A}$
Standby Current	$I_{std}$	$V_{in} = 5\text{ V}$ , EN = 1.2 V		26	37	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$		0.08		$\mu\text{A}$
FLAG Output Low Voltage	$V_{olflag}$	$V_{in} > \text{OVLO}$ Sink 1 mA on FLAG pin			400	mV
FLAG Leakage Current	FLAG <sub>leak</sub>	FLAG level = 5 V		5.0		nA
$\overline{\text{EN}}$ Voltage High	$V_{ih}$	$V_{in}$ from 3.3 V to 5.5 V	1.2			V
$\overline{\text{EN}}$ Voltage Low	$V_{il}$	$V_{in}$ from 3.3 V to 5.5 V			0.55	V
EN Leakage Current	EN <sub>leak</sub>	EN = 5.5 V or GND		170		nA

## TIMINGS

Start Up Delay	$t_{on}$	From $V_{in} > \text{UVLO}$ to $V_{out} = 0.8 \times V_{in}$ , See Fig 3 & 9		4.0	15	ms
FLAG going up Delay	$t_{start}$	From $V_{in} > \text{UVLO}$ to FLAG = 1.2 V, See Fig 3 & 10		3.0		$\mu\text{s}$
Output Turn Off Time	$t_{off}$	From $V_{in} > \text{OVLO}$ to $V_{out} \leq 0.3\text{ V}$ , See Fig 4 & 11 $V_{in}$ increasing from 5 V to 8 V at 3 V/ $\mu\text{s}$ .		0.7	1.5	$\mu\text{s}$
Alert Delay	$t_{stop}$	From $V_{in} > \text{OVLO}$ to FLAG $\leq 0.4\text{ V}$ , See Fig 4 & 12 $V_{in}$ increasing from 5 V to 8 V at 3 V/ $\mu\text{s}$		1.0		$\mu\text{s}$
Disable Time	$t_{dis}$	From $\overline{\text{EN}} 0.4$ to 1.2V to $V_{out} \leq 0.3\text{ V}$ , See Fig 5 & 13 $V_{in} = 4.75\text{ V}$ .		3.0		$\mu\text{s}$
Thermal Shutdown Temperature	$T_{sd}$			150		$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	$T_{sdhyst}$			30		$^{\circ}\text{C}$

## ESD DIODES ( $T_A = 25^{\circ}\text{C}$ , unless otherwise noted)

Capacitance (Note 7) Pin $V_{BUS}$ TVS Pins D+ & D-	C			30 0.5	0.9	pF
Clamping Voltage (Notes 5, 6, 7) Pin $V_{BUS}$ TVS Pins D+ & D-	$V_C$	@ $I_{PP} = 5.9\text{ A}$ @ $I_{PP} = 1.0\text{ A}$			23.7 9.8	V
Working Peak Reverse Voltage (Note 7) Pin $V_{BUS}$ TVS Pins D+ & D-	$V_{RWM}$				12 5.0	V
Maximum Reverse Leakage Current	$I_R$	@ $V_{RWM}$			1.0	$\mu\text{A}$
Breakdown Voltage (Note 4) Pin $V_{BUS}$ TVS Pins D+ & D-	$V_{BR}$	@ $I_T = 1.0\text{ mA}$	13.5 5.4			V

4.  $V_{BR}$  is measured with a pulse test current  $I_T$  at an ambient temperature of  $25^{\circ}\text{C}$ .

5. Surge current waveform per Figure 28 in ESD paragraph.

6. For test procedures see Figures 26 and 27: IEC61000-4-2 spec, diagram of ESD test setup and Application Note AND8307/D.

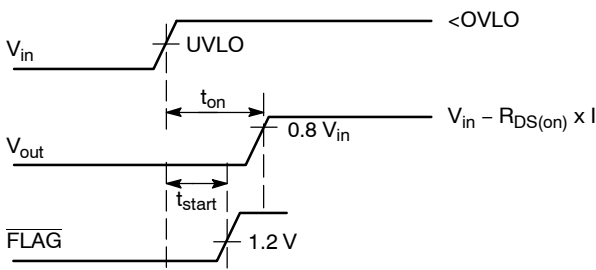
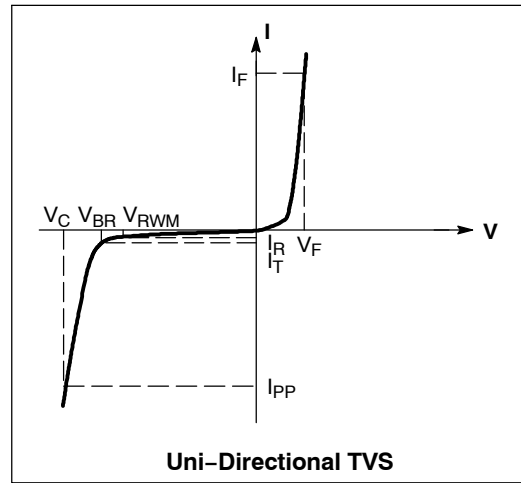
7. ESD diode parameters are guaranteed by design.

**ELECTRICAL CHARACTERISTICS**

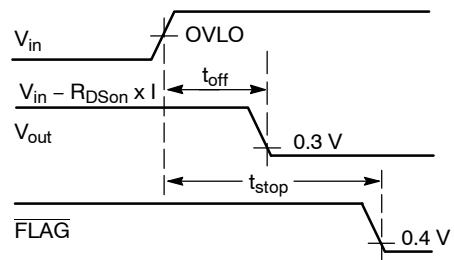
( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$
$P_{pk}$	Peak Power Dissipation
C	Max. Capacitance @ $V_R = 0$ and $f = 1$ MHz

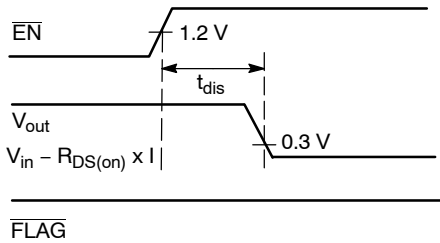
\*Additional  $V_C$ ,  $V_{RWM}$  and  $V_{BR}$  voltage can be available. Please contact your ON Semiconductor representative for availability.



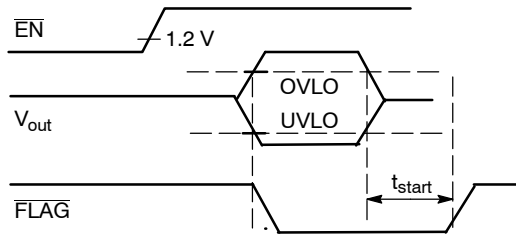
**Figure 3. Start Up Sequence**



**Figure 4. Shutdown on Over Voltage Detection**



**Figure 5. Disable on  $\overline{EN} = 1$**



**Figure 6.  $\overline{FLAG}$  Response with  $\overline{EN} = 1$**

# NCP362

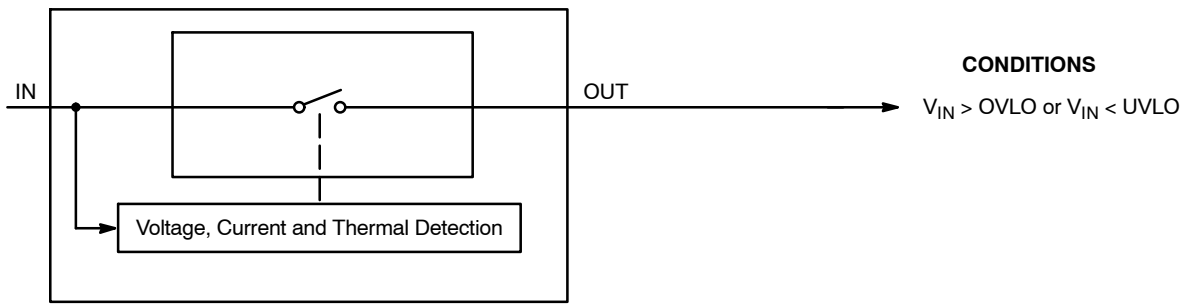


Figure 7.

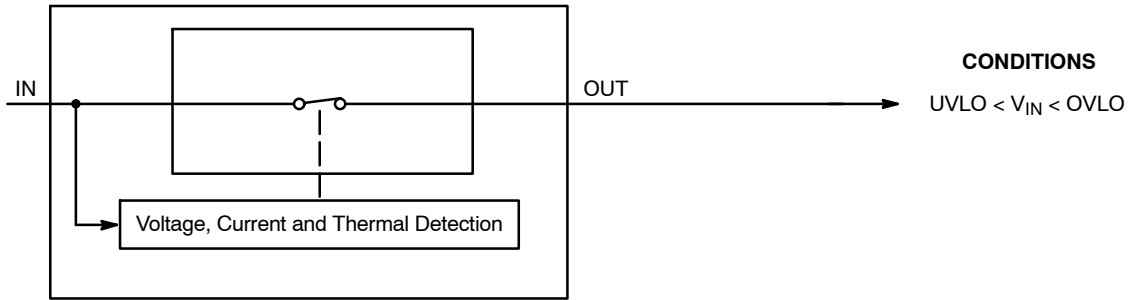


Figure 8.

TYPICAL OPERATING CHARACTERISTICS

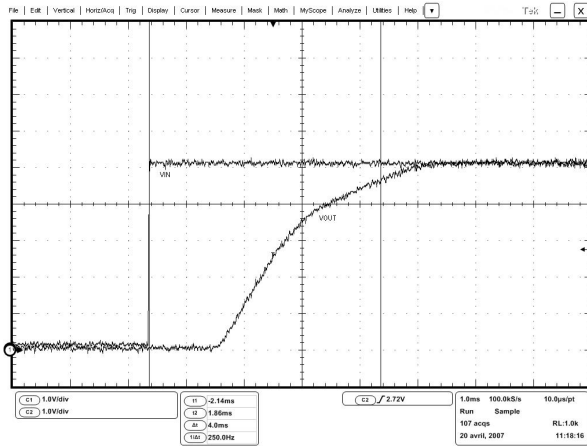


Figure 9. Start Up. Vin=Ch1, Vout=Ch2

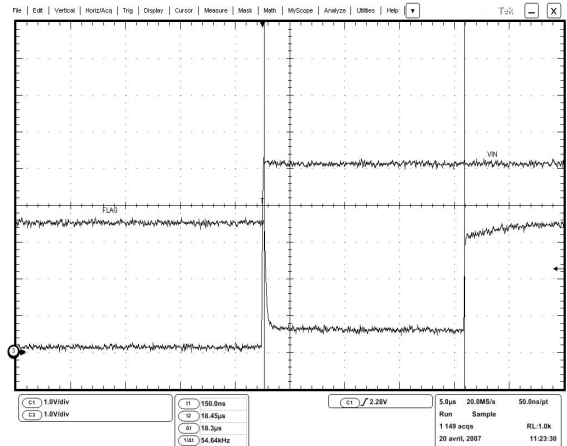


Figure 10. FLAG Going Up Delay. Vin=Ch1, FLAG=Ch3

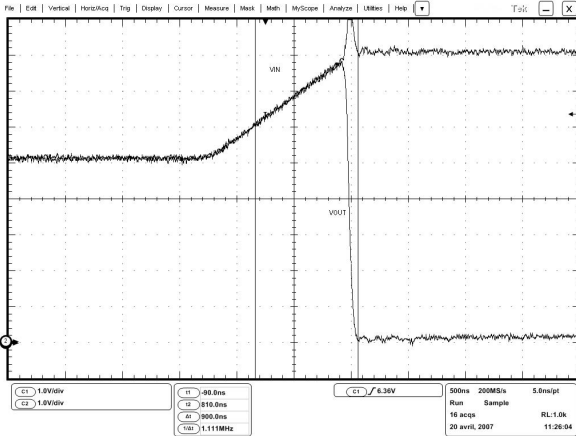


Figure 11. Output Turn Off time. Vin=Ch1, Vout=Ch2

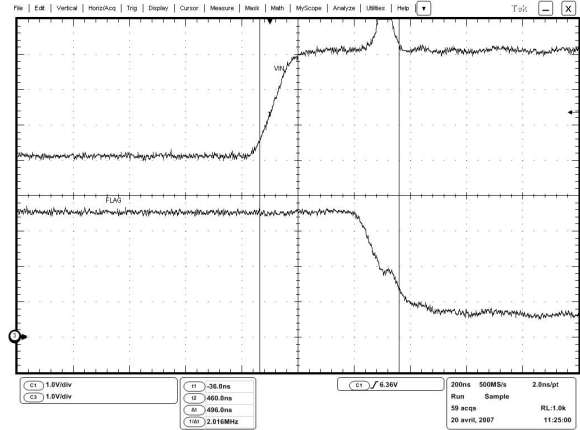


Figure 12. Alert Delay. Vout=Ch1, FLAG=Ch3

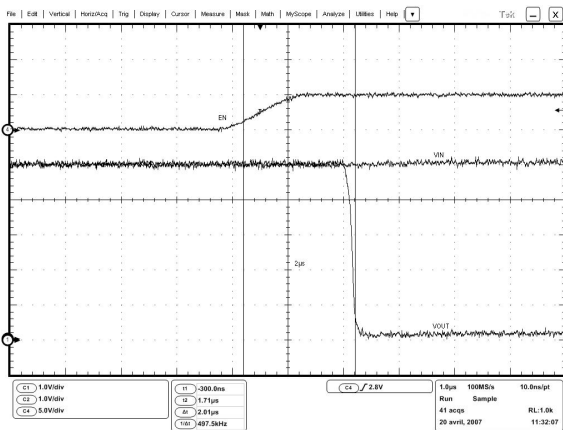


Figure 13. Disable Time. EN=Ch4, Vin=Ch1, Vout=Ch2

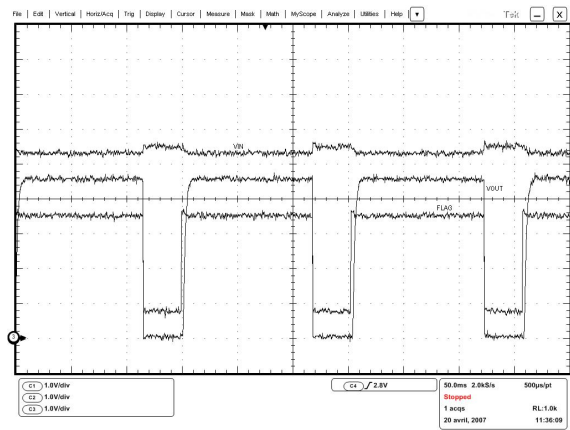


Figure 14. Thermal Shutdown. Vin=Ch1, Vout=Ch2, FLAG=Ch3



TYPICAL OPERATING CHARACTERISTICS

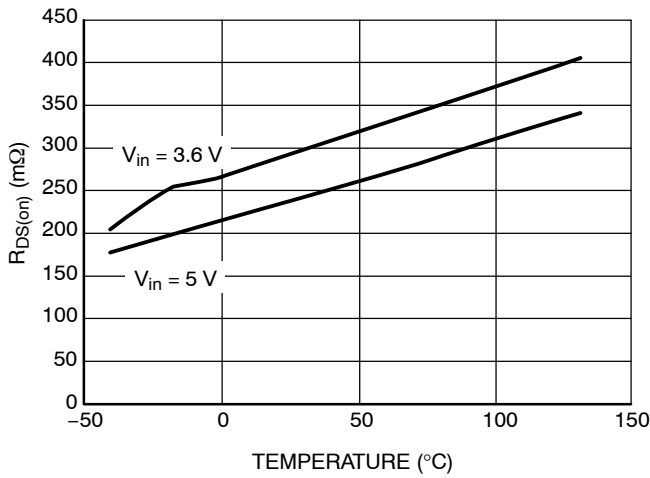


Figure 15.  $R_{DS(on)}$  vs. Temperature (Load = 500 mA)

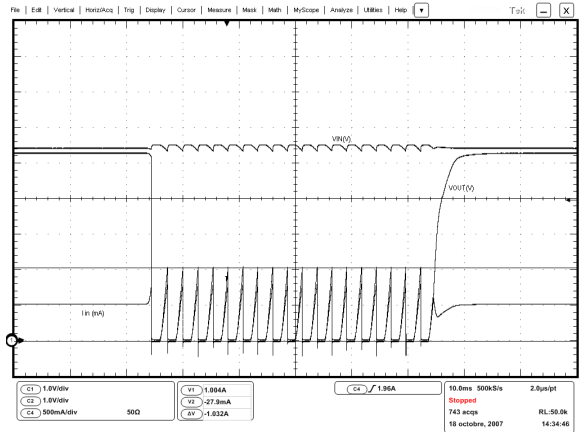


Figure 16. Output Short Circuit

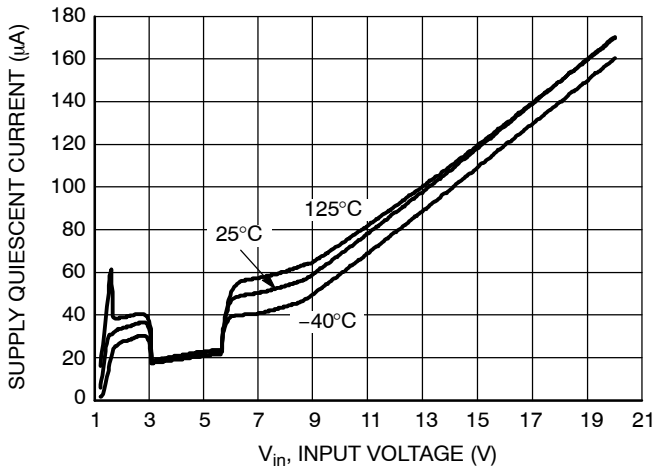


Figure 17. Quiescent Current vs. Input Voltage

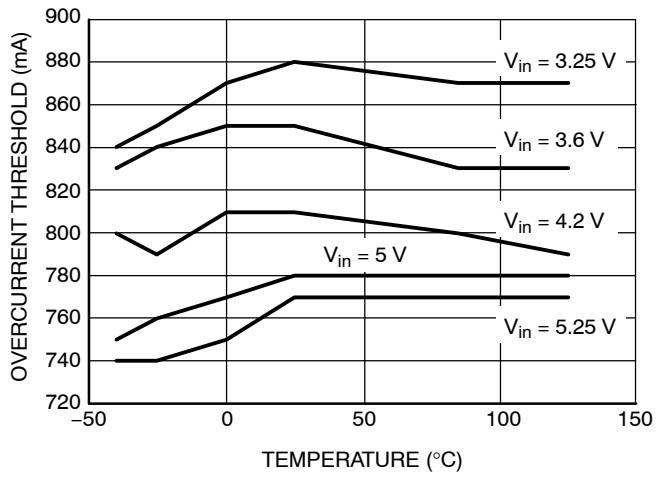


Figure 18. Overcurrent Protection Threshold vs. Temperature

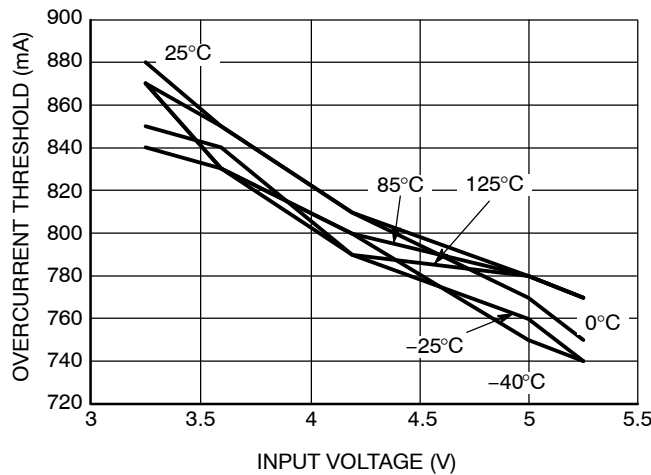


Figure 19. Overcurrent Protection Threshold vs. Input Voltage

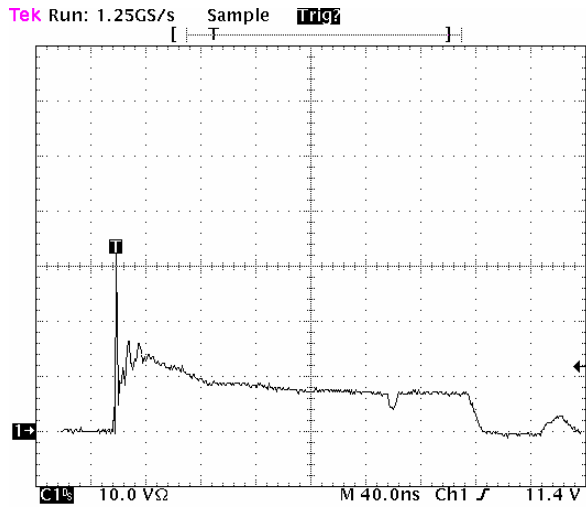


Figure 20.  $V_{BUS}$  TVS Clamping Voltage Screenshot Positive 8 kV contact per IEC 61000-4-2

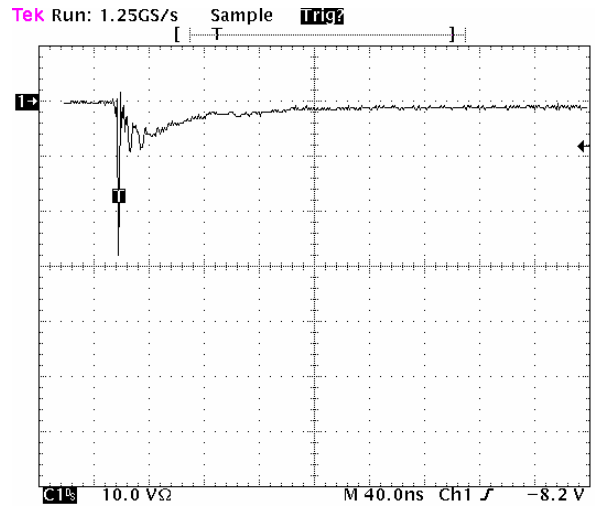


Figure 21.  $V_{BUS}$  TVS Clamping Voltage Screenshot Negative 8 kV contact per IEC 61000-4-2

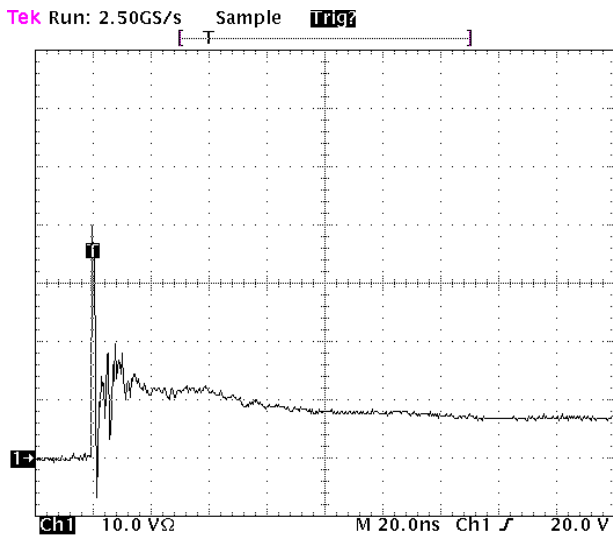


Figure 22. D+ & D- Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

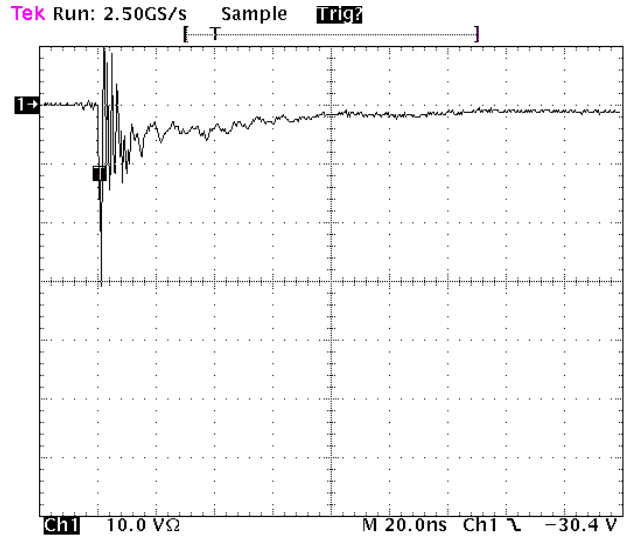


Figure 23. D+ & D- Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

**Operation**

NCP362 provides overvoltage protection for positive voltage, up to 20 V. A PMOS FET protects the systems (i.e.: VBUS) connected on the V<sub>out</sub> pin, against positive overvoltage. The Output follows the VBUS level until OVLO threshold is overtaken.

**Undervoltage Lockout (UVLO)**

To ensure proper operation under any conditions, the device has a built-in undervoltage lock out (UVLO) circuit. During V<sub>in</sub> positive going slope, the output remains disconnected from input until V<sub>in</sub> voltage is above 3.0 V nominal. The  $\overline{\text{FLAG}}$  output is pulled to low as long as V<sub>in</sub> does not reach UVLO threshold. This circuit has a 70 mV hysteresis to provide noise immunity to transient condition.

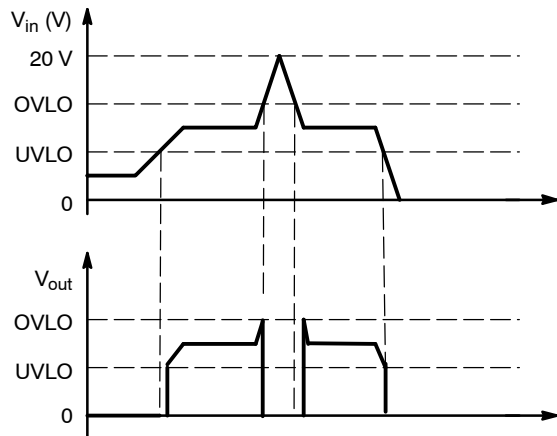


Figure 24. Output Characteristic vs. V<sub>in</sub>

**Overvoltage Lockout (OVLO)**

To protect connected systems on V<sub>out</sub> pin from overvoltage, the device has a built-in overvoltage lock out (OVLO) circuit. During overvoltage condition, the output remains disabled until the input voltage exceeds 6.0 V.

$\overline{\text{FLAG}}$  output is tied to low until V<sub>in</sub> is higher than OVLO. This circuit has a 100 mV hysteresis to provide noise immunity to transient conditions.

**Overcurrent Protection (OCP)**

The NCP362 integrates overcurrent protection to prevent system/battery overload or defect. The current limit threshold is internally set at 750 mA. This value can be changed from 150 mA to 750 mA by a metal tweak, please contact your ON Semiconductor representative for availability. During current fault, the internal PMOS FET

is automatically turned off (5  $\mu$ s) if the charge current exceeds I<sub>lim</sub>. NCP362 goes into turn on and turn off mode as long as defect is present. The internal t<sub>on</sub> delay (4 ms typical) allows limiting thermal dissipation. The Flag pin goes to low level when an overcurrent fault appears. That allows the microcontroller to count defect events and turns off the PMOS with EN pin.

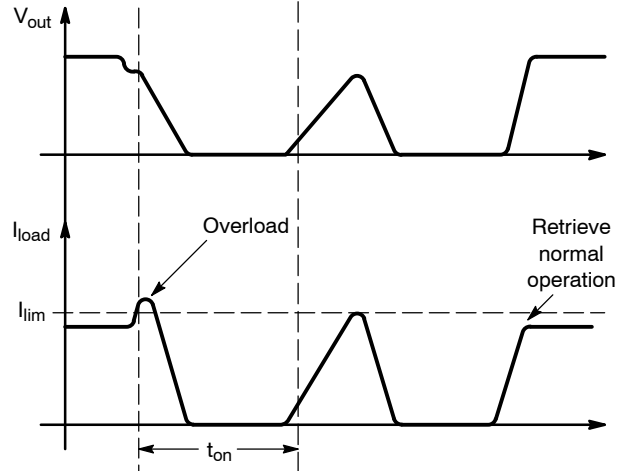


Figure 25. Overcurrent Event Example

**$\overline{\text{FLAG}}$  Output**

NCP362 provides a  $\overline{\text{FLAG}}$  output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon as:  $1.2 \text{ V} < V_{in} < \text{UVLO}$ ,  $V_{in} > \text{OVLO}$ ,  $I_{\text{charge}} > I_{\text{limit}}$ ,  $T_J > 150^\circ\text{C}$ . When NCP362 recovers normal condition,  $\overline{\text{FLAG}}$  is held high. The pin is an open drain output, thus a pull up resistor (typically 1 M $\Omega$  – Minimum 10 k $\Omega$ ) must be provided to V<sub>CC</sub>.  $\overline{\text{FLAG}}$  pin is an open drain output.

**$\overline{\text{EN}}$  Input**

To enable normal operation, the  $\overline{\text{EN}}$  pin shall be forced to low or connected to ground. A high level on the pin disconnects OUT pin from IN pin.  $\overline{\text{EN}}$  does not overdrive an OVLO or UVLO fault.

**Internal PMOS FET**

The NCP362 includes an internal PMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the R<sub>DS(on)</sub>, during normal operation, will create low losses on V<sub>out</sub> pin, characterized by V<sub>in</sub> versus V<sub>out</sub> dropout.

# NCP362

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

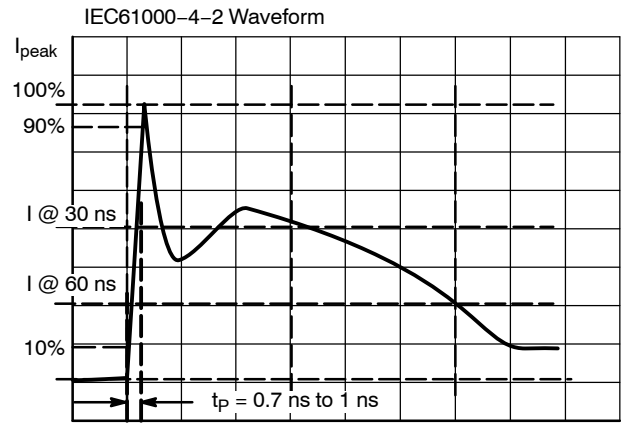


Figure 26. IEC61000-4-2 Spec

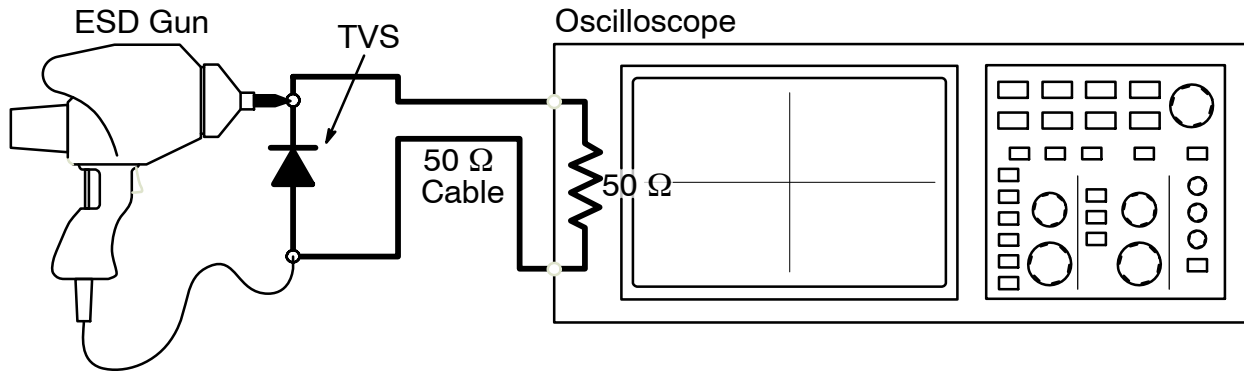


Figure 27. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

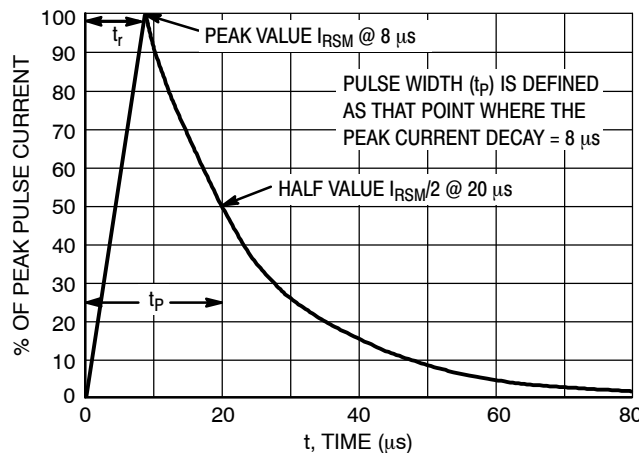


Figure 28. 8 X 20 μs Pulse Waveform

# NCP362

## PCB Recommendations

The NCP362 integrates a 500 mA rated PMOS FET, and the PCB rules must be respected to properly evacuate the heat out of the silicon. The UDFN PAD1 must be connected to ground plane to increase the heat transfer if necessary from an application standpoint. Of course, in any case, this pad shall be not connected to any other potential.

By increasing PCB area, the  $R_{\theta JA}$  of the package can be decreased, allowing higher charge current to fill the battery.

Taking into account that internal bondings (wires between package and silicon) can handle up to 1 A (higher than thermal capability), the following calculation shows

two different example of current capability, depending on PCB area:

- With 280°C/W (without PCB area), allowing DC current is 500 mA
- With 210°C/W (200 mm<sup>2</sup>), the charge DC current allows with a 85°C ambient temperature is:  

$$I = \sqrt{(T_J - T_A) / (R_{\theta JA} \times R_{DSON})}$$

$$I = 800 \text{ mA}$$

In every case, we recommend to make thermal measurement on final application board to make sure of the final Thermal Resistance.

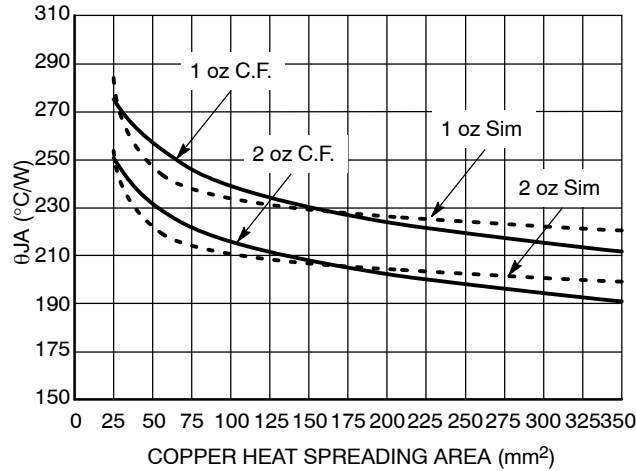


Figure 29.

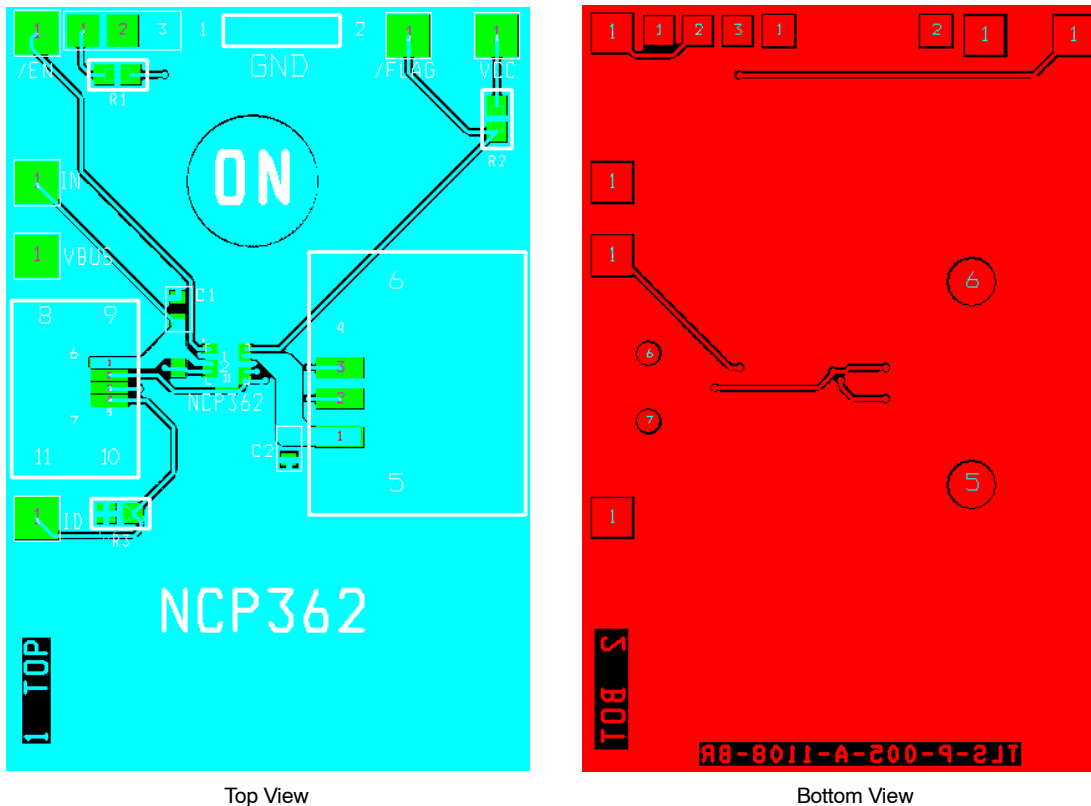


Figure 30. Demo Board Layout



# NCP362

## ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP362AMUTBG	ADA	UDFN10 (Pb-Free)	3000 / Tape & Reel
NCP362BMUTBG	ADG	UDFN10 (Pb-Free)	3000 / Tape & Reel
NCP362CMUTBG	ADC	UDFN10 (Pb-Free)	3000 / Tape & Reel

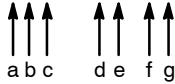
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## SELECTION GUIDE

The NCP362 can be available in several undervoltage, overvoltage, overcurrent and clamping voltage versions.

Part number is designated as follows:

**NCP362xxxMUxxTBG**



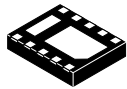
Code	Contents
a	ESD diode options A: TVS diode on pin 4 B: ESD diodes on pins 6 & 7 C: Option A & B
b	TVS Pin 4 $V_{RWM}$ voltage -: 12 V ESD Pin 6 & 7 $V_{RWM}$ voltage -: 5 V
c	Overcurrent Typical Threshold -: 750 mA
d	UVLO Typical Threshold -: 3.00 V
e	OVLO Typical Threshold -: 5.675 V
f	Tape & Reel Type B: = 3000
g	Pb-Free

NOTE: Please contact your ON Semiconductor representative for availability of additional options.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

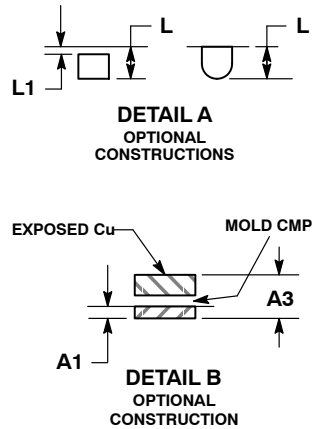
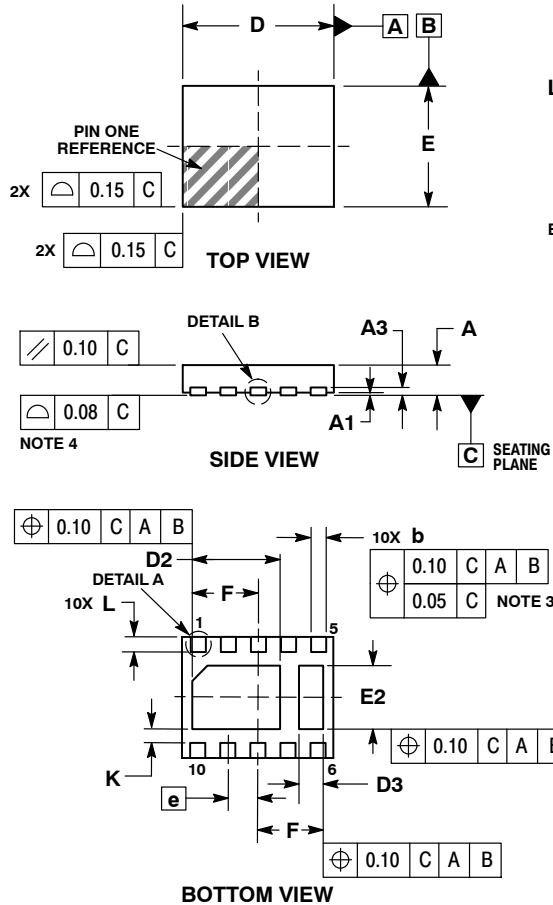
ON Semiconductor®



SCALE 4:1

UDFN10 2.5x2, 0.5P  
CASE 517AV-01  
ISSUE A

DATE 12 FEB 2009

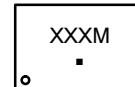


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	2.50 BSC	
D2	1.35	1.55
D3	0.30	0.50
E	2.00 BSC	
E2	0.95	1.15
e	0.50 BSC	
F	1.08 BSC	
K	0.20	---
L	0.20	0.30
L1	---	0.15

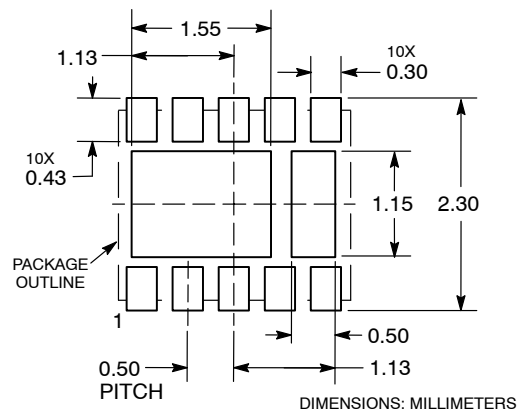
**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>UDFN10 2.5X2, 0.5P</b>	<b>PAGE 1 OF 1</b>

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