NDF10N60Z

N-Channel Power MOSFET 600 V, 0.75 Ω

Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode−Protected Gate
- 100% Avalanche Tested
- 100% R_g Tested
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	NDF	Unit
Drain−to−Source Voltage	V_{DSS}	600	V
Continuous Drain Current, $R_{\theta JC}$ (Note 1)	I_D	10	A
Continuous Drain Current T_A = 100°C, $R_{\theta JC}$ (Note 1)	I_D	6.0	A
Pulsed Drain Current, t_P = 10 μs	I_{DM}	40	A
Power Dissipation, $R_{\theta JC}$	P_D	39	W
Gate−to−Source Voltage	V_{GS}	±30	V
Single Pulse Avalanche Energy (L = 6.0 mH, I_D = 10 A)	E_{AS}	300	mJ
ESD (HBM) (JESD22−A114)	V_{esd}	3900	V
RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T_A = 25°C) (Figure 13)	V_{ISO}	4500	V
Peak Diode Recovery (Note 2)	dV/dt	4.5	V/ns
MOSFET dV/dt	dV/dt	60	V/ns
Continuous Source Current (Body Diode)	I_S	10	A
Maximum Temperature for Soldering Leads	T_L	260	°C
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by maximum junction temperature.
2. I_S ≤ 10 A, di/dt ≤ 200 A/μs, V_{DD} = 80% BV_{DSS}

ON Semiconductor®

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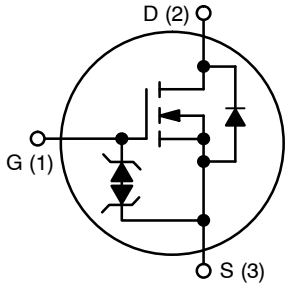
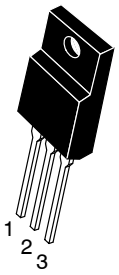
V_{DSS} (@ T_{Jmax})	$R_{DS(ON)}$ (MAX) @ 5 A
650 V	0.75 Ω

N−Channel





NDF10N60ZG
NDF10N60ZH
TO−220FP
CASE 221AH

ORDERING AND MARKING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

THERMAL RESISTANCE

Parameter	Symbol	NDF10N60Z	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	3.2	°C/W
Junction−to−Ambient Steady State (Note 3)	$R_{\theta JA}$	50	

3. Insertion mounted

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Test Conditions		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA		BV_{DSS}	600			V
Breakdown Voltage Temperature Coefficient	Reference to 25°C, I_D = 1 mA		$\Delta BV_{DSS}/\Delta T_J$		0.6		V/°C
Drain−to−Source Leakage Current	V_{DS} = 600 V, V_{GS} = 0 V	25°C	I_{DSS}			1	μA
		150°C				50	
Gate−to−Source Forward Leakage	V_{GS} = ±20 V		I_{GSS}			±10	μA
ON CHARACTERISTICS (Note 4)							
Static Drain−to−Source On−Resistance	V_{GS} = 10 V, I_D = 5.0 A		$R_{DS(on)}$		0.65	0.75	Ω
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 100 μA		$V_{GS(th)}$	3.0	3.9	4.5	V
Forward Transconductance	V_{DS} = 15 V, I_D = 10 A		g_{FS}		7.9		S
DYNAMIC CHARACTERISTICS							
Input Capacitance (Note 5)	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		C_{iss}	1097	1373	1645	pF
Output Capacitance (Note 5)			C_{oss}	118	150	178	
Reverse Transfer Capacitance (Note 5)			C_{rss}	20	35	50	
Total Gate Charge (Note 5)	V_{DD} = 300 V, I_D = 10 A, V_{GS} = 10 V		Q_g	23	47	68	nC
Gate−to−Source Charge (Note 5)			Q_{gs}	5.0	9.0	14	
Gate−to−Drain (“Miller”) Charge (Note 5)			Q_{gd}	12	26	36	
Plateau Voltage			V_{GP}		6.4		V
Gate Resistance			R_g	0.5	1.5	4.5	Ω
RESISTIVE SWITCHING CHARACTERISTICS							
Turn−On Delay Time	V_{DD} = 300 V, I_D = 10 A, V_{GS} = 10 V, R_G = 5 Ω		$t_{d(on)}$		15		ns
Rise Time			t_r		31		
Turn−Off Delay Time			$t_{d(off)}$		40		
Fall Time			t_f		23		

SOURCE−DRAIN DIODE CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Diode Forward Voltage	I_S = 10 A, V_{GS} = 0 V	V_{SD}			1.6	V
Reverse Recovery Time	V_{GS} = 0 V, V_{DD} = 30 V, I_S = 10 A, di/dt = 100 A/μs	t_{rr}		395		ns
Reverse Recovery Charge		Q_{rr}		3.0		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.
5. Guaranteed by design.

TYPICAL CHARACTERISTICS

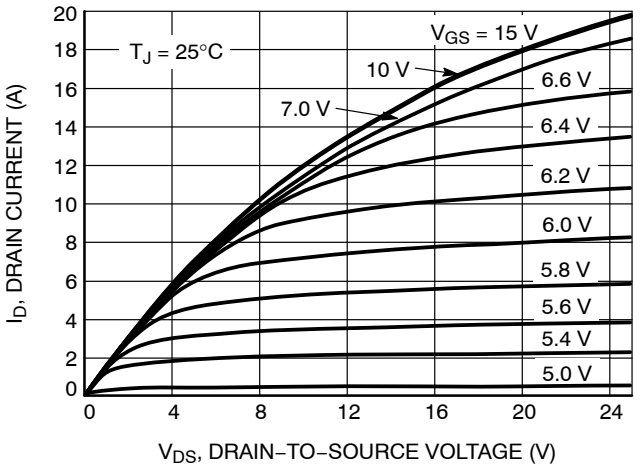


Figure 1. On−Region Characteristics

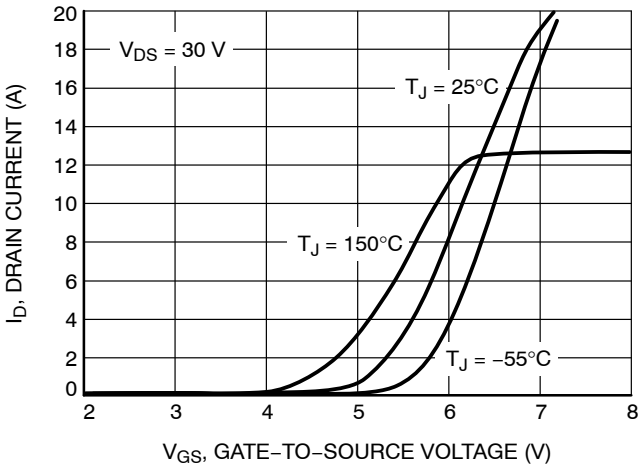


Figure 2. Transfer Characteristics

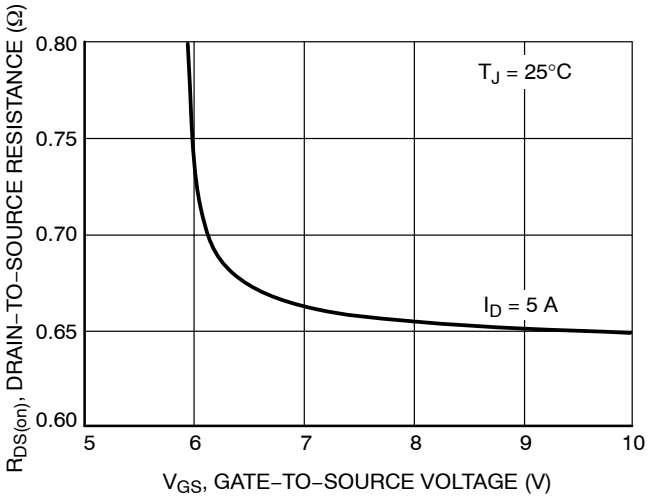


Figure 3. On−Resistance vs. Gate Voltage

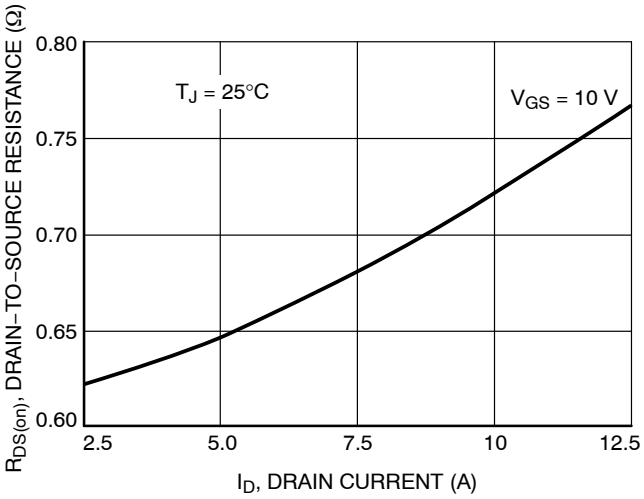


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

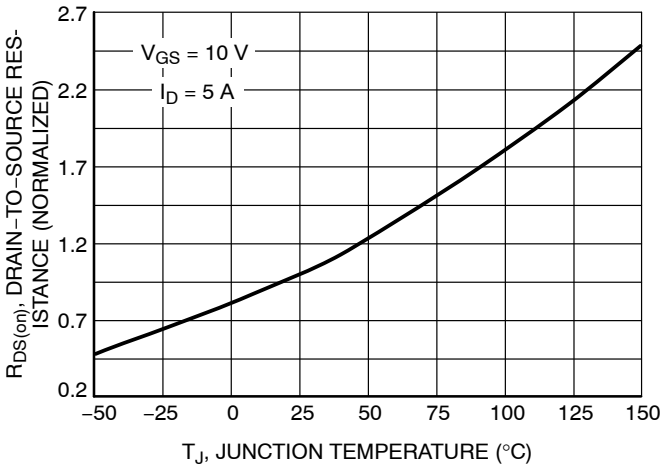


Figure 5. On−Resistance Variation with Temperature

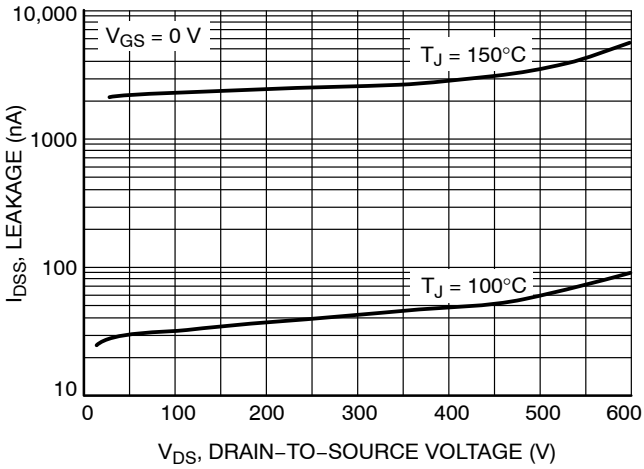


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

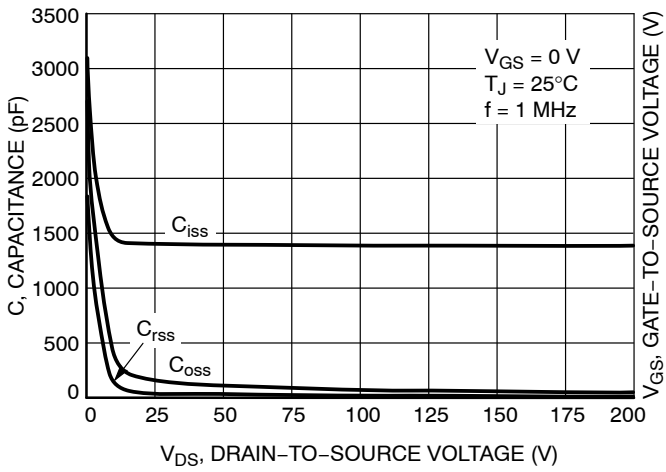


Figure 7. Capacitance Variation

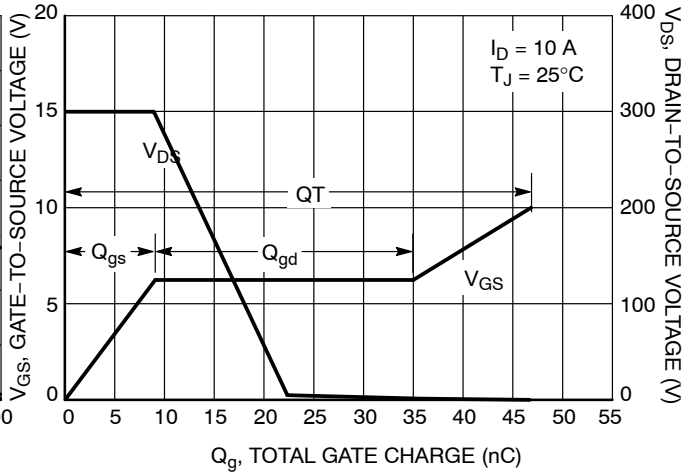


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

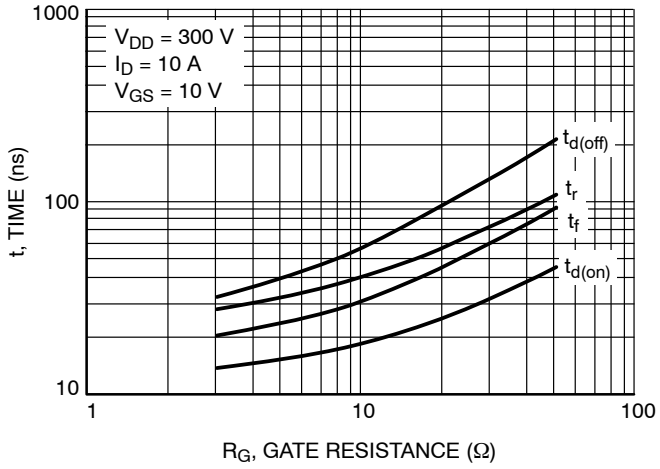


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

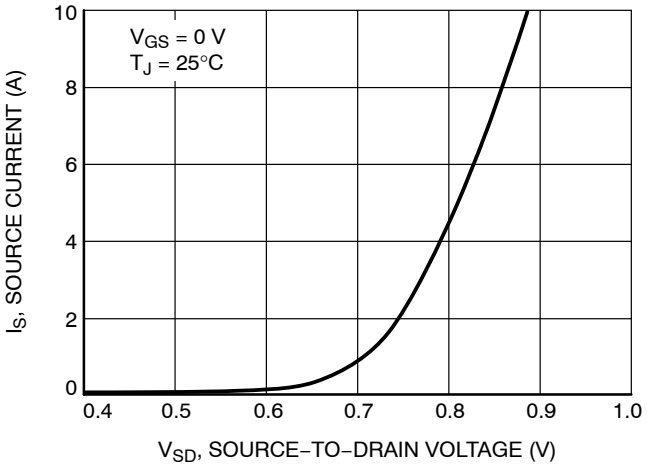


Figure 10. Diode Source Current vs. Forward Voltage

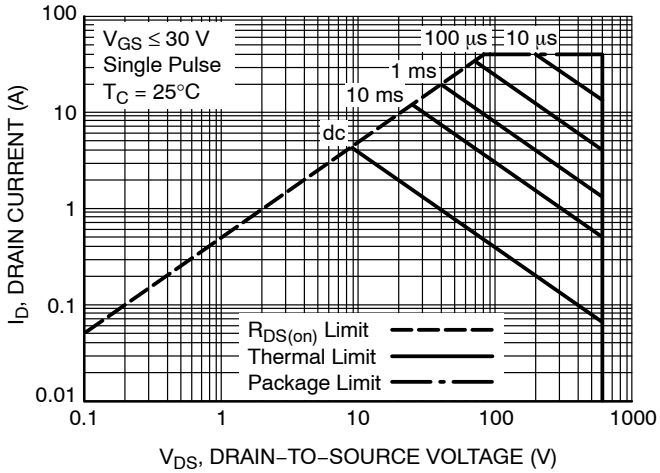


Figure 11. Maximum Rated Forward Biased Safe Operating Area for NDF10N60Z

TYPICAL CHARACTERISTICS

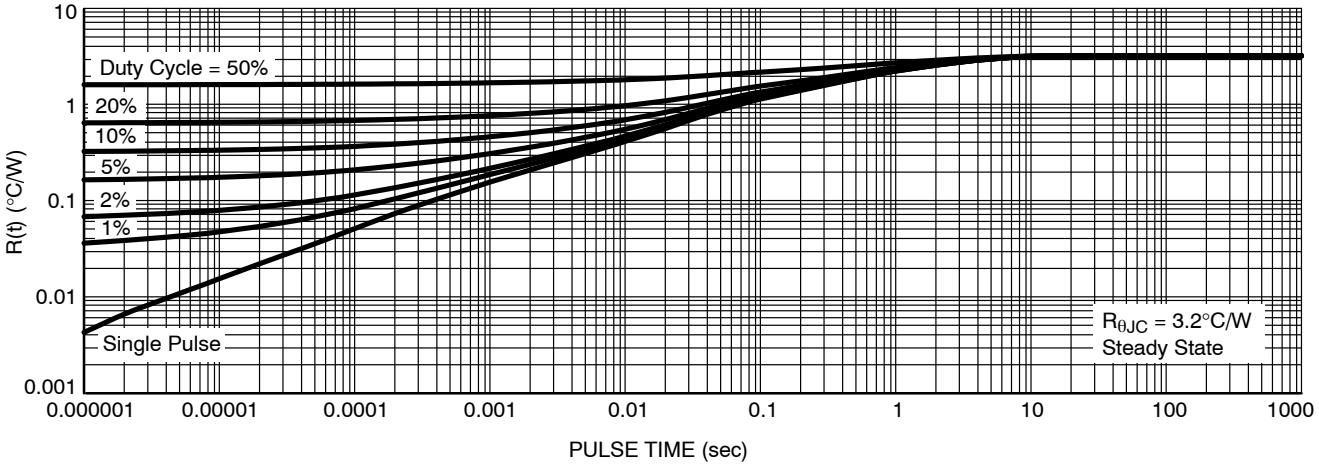


Figure 12. Thermal Impedance for NDF10N60Z

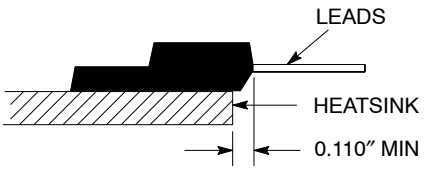


Figure 13. Mounting Position for Isolation Test

Measurement made between leads and heatsink with all leads shorted together.

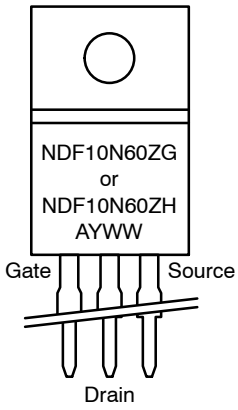
*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

Order Number	Package	Shipping†
NDF10N60ZG	TO−220FP (Pb−Free, Halogen−Free)	50 Units / Rail
NDF10N60ZH	TO−220FP (Pb−Free, Halogen−Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

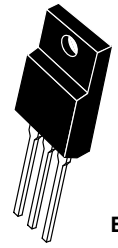


TO−220FP

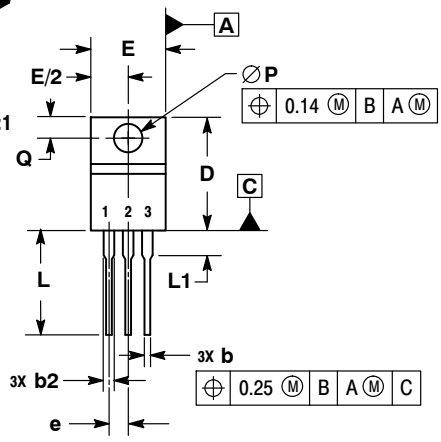
A = Location Code
Y = Year
WW = Work Week
G, H = Pb−Free, Halogen−Free Package

TO−220 FULLPACK, 3−LEAD
CASE 221AH
ISSUE F

DATE 30 SEP 2014

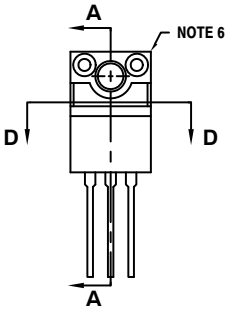


SCALE 1:1

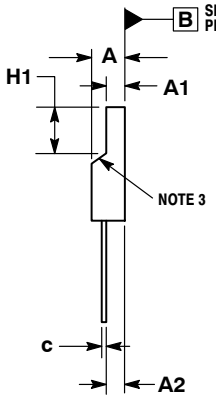


FRONT VIEW

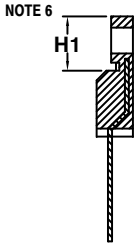
SECTION D−D



ALTERNATE CONSTRUCTION



SIDE VIEW

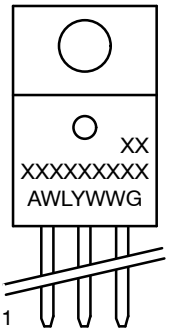


SECTION A−A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR UNCONTROLLED IN THIS AREA.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.
6. CONTOURS AND FEATURES OF THE MOLDED PACKAGE BODY MAY VARY WITHIN THE ENVELOP DEFINED BY DIMENSIONS A1 AND H1 FOR MANUFACTURING PURPOSES.

	MILLIMETERS	
DIM	MIN	MAX
A	4.30	4.70
A1	2.50	2.90
A2	2.50	2.90
b	0.54	0.84
b2	1.10	1.40
c	0.49	0.79
D	14.70	15.30
E	9.70	10.30
e	2.54 BSC	
H1	6.60	7.10
L	12.50	14.73
L1	---	2.80
P	3.00	3.40
Q	2.80	3.20

GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. GATE

DOCUMENT NUMBER:	**98AON52577E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−220 FULLPACK, 3−LEAD**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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