

NB2969A

Low Power, Reduced EMI Clock Synthesizer

The NB2969A is a versatile spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. The NB2969A reduces ElectroMagnetic Interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The NB2969A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads and shielding that are traditionally required to pass EMI regulations.

The NB2969A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all digital method.

The NB2969A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

The NB2969A is targeted towards all portable devices with very low power requirements like MP3 players, Notebooks and digital still cameras.

Features

- Generates an EMI Optimized Clocking Signal at the Output
- Integrated Loop Filter Components
- Operates with a 3.3 V / 2.5 V Supply
- Operating Current less than 4.0 mA
- Low Power CMOS Design
- Input Frequency Range: 6.0 MHz to 12 MHz for 2.5 V
Input Frequency Range: 6.0 MHz to 13 MHz for 3.3 V
- Generates a 1X Low EMI Spread Spectrum clock of the Input Frequency
- Frequency Deviation $\pm 1\%$ @ 10 MHz
- Available in TSOP-6 Package (TSOT-23-6)
- Pb-Free Package is Available



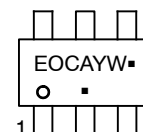
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*



TSOP-6
(TSOT-23-6)
SN SUFFIX
CASE 318G



EOC = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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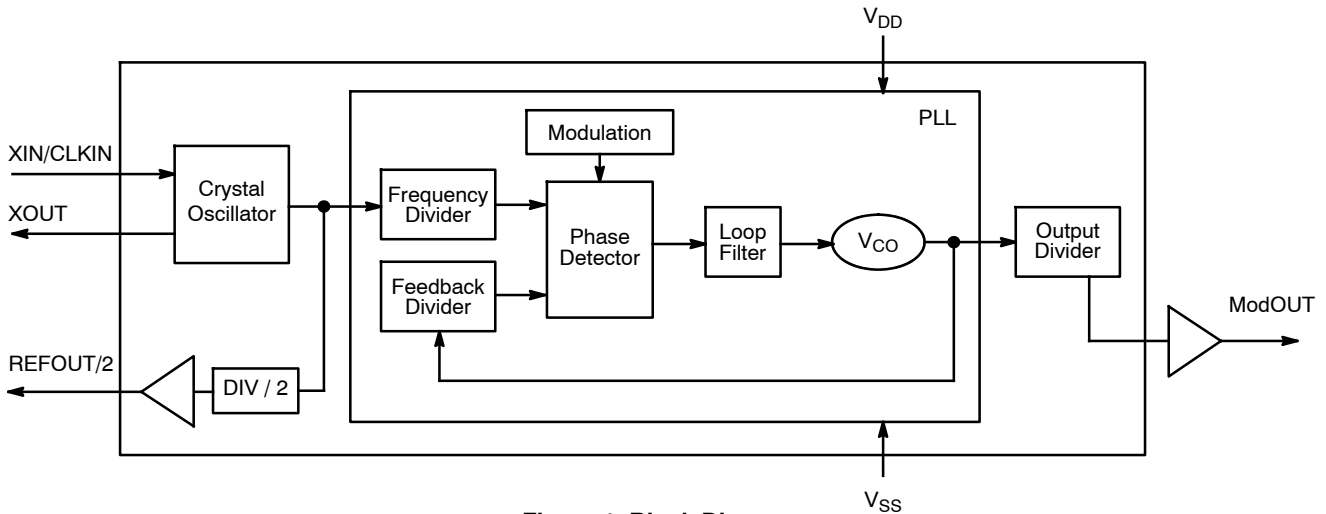


Figure 1. Block Diagram

Table 1. KEY SPECIFICATIONS

| Description | Specification |
|--------------------------|--|
| Supply Voltages | $V_{DD} = 3.3 \text{ V} / 2.5 \text{ V}$ |
| Frequency Range | For 2.5 V Supply For 3.3 V Supply 6.0 MHz < CLKIN < 12 MHz 6.0 MHz < CLKIN < 13 MHz |
| Cycle-to-Cycle Jitter | 200 ps (maximum) |
| Output Duty Cycle | 45/55% (worst case) |
| Modulation Rate Equation | $F_{IN}/256$ |
| Frequency Deviation | $\pm 1\% @ 10 \text{ MHz}$ |

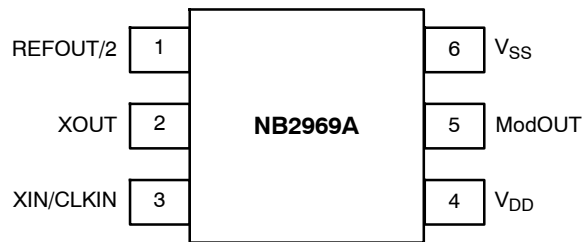


Figure 2. Pin Configuration

Table 2. PIN DESCRIPTION

| Pin # | Pin Name | Type | Description |
|-------|-----------|------|--|
| 1 | REFOUT/2 | O | Buffered and divided by 2 output of the input frequency. |
| 2 | XOUT | O | Crystal connection. If using an external reference, this pin must be left unconnected. |
| 3 | XIN/CLKIN | I | Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock. |
| 4 | V_{DD} | P | Power supply for the entire chip. |
| 5 | ModOUT | O | Spread spectrum clock output. |
| 6 | V_{SS} | P | Ground connection. |

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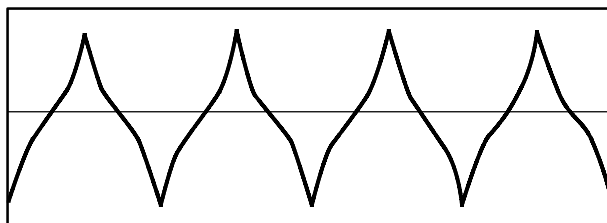


Figure 3. Modulation Profile

Table 3. MAXIMUM RATINGS

| Symbol | Description | Rating | Unit |
|------------------|--|-------------|------|
| V_{DD}, V_{IN} | Voltage on any pin with respect to Ground | 0.5 to +7.0 | V |
| T_{STG} | Storage Temperature | -65 to +125 | °C |
| T_A | Operating Temperature | 0 to 70 | °C |
| T_s | Max. Soldering Temperature (10 sec) | 260 | °C |
| T_J | Junction Temperature | 150 | °C |
| T_{DV} | Static Discharge Voltage (As per MIL-STD-883, Method 3015) | 2 | kV |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 4. DC ELECTRICAL CHARACTERISTICS FOR 2.5 V SUPPLY (Test Conditions: All parameters are measured at room temperature 25°C)

| Symbol | Description | Min | Typ | Max | Unit |
|------------------|---|-----------|-----|-----------------------|------|
| V _{IL} | Input LOW Voltage | GND - 0.3 | | 0.8 | V |
| V _{IH} | Input HIGH Voltage | 2.0 | | V _{DD} + 0.3 | V |
| I _{IL} | Input LOW Current | | | -35 | μA |
| I _{IH} | Input HIGH Current | | | 35 | μA |
| I _{XOL} | XOUT Output LOW Current (@ 0.5 V, V _{DD} = 2.5 V) | | 3.0 | | mA |
| I _{XOH} | XOUT Output HIGH Current (@ 2.5 V, V _{DD} = 2.5 V) | | 3.0 | | mA |
| V _{OL} | Output LOW Voltage (V _{DD} = 2.5 V, I _{OL} = 8.0 mA) | | | 0.6 | V |
| V _{OH} | Output HIGH Voltage (V _{DD} = 2.5 V, I _{OH} = 8.0 mA) | 1.8 | | | V |
| I _{DD} | Static Supply Current (Note 1) | | 1.0 | | mA |
| I _{CC} | Dynamic Supply Current (2.5 V, 10 MHz, and No Load) | | 2.5 | | mA |
| V _{DD} | Operating Voltage | 2.375 | 2.5 | 2.625 | V |
| t _{ON} | Powerup Time (first locked cycle after powerup) (Note 2) | | | 5.0 | mS |
| Z _{OUT} | Clock Output Impedance | | 50 | | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. XIN/CLKIN pin is pulled low.
2. V_{DD} and XIN/CLKIN input are stable.

Table 5. AC ELECTRICAL CHARACTERISTICS FOR 2.5 V SUPPLY

| Symbol | Description | Min | Typ | Max | Unit |
|--------------------------|--|-----|-----|----------------|------|
| CLKIN | Input Frequency | 6.0 | | 12 | MHz |
| ModOUT | Output Frequency | 6.0 | | 12 | MHz |
| f _d | Frequency Deviation Input Frequency = 6.0 MHz Input Frequency = 12 MHz | | | ±1.47 ±0.78 | % |
| t _{LH} (Note 3) | Output Rise Time (measured at 0.7 V to 1.7 V) | 0.7 | 1.4 | 1.7 | ns |
| t _{HL} (Note 3) | Output Fall Time (measured at 1.7 V to 0.7 V) | 0.4 | 0.9 | 1.1 | ns |
| t _{JC} | Jitter (Cycle-to-Cycle) | | | 200 | ps |
| t _D | Output Duty Cycle | 45 | 50 | 55 | % |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. t_{LH} and t_{HL} are measured at capacitive load of 15 pF.

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Table 6. DC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY (Test Conditions: All parameters are measured at room temperature 25°C)

| Symbol | Description | Min | Typ | Max | Unit |
|------------------|---|-----------|-----|-----------------------|------|
| V _{IL} | Input LOW Voltage | GND - 0.3 | | 0.8 | V |
| V _{IH} | Input HIGH Voltage | 2.0 | | V _{DD} + 0.3 | V |
| I _{IL} | Input LOW Current | | | -35 | μA |
| I _{IH} | Input HIGH Current | | | 35 | μA |
| I _{XOL} | XOUT Output LOW Current (@ 0.4 V, V _{DD} = 3.3 V) | | 3.0 | | mA |
| I _{XOH} | XOUT Output HIGH Current (@ 2.5 V, V _{DD} = 3.3 V) | | 3.0 | | mA |
| V _{OL} | Output LOW Voltage (V _{DD} = 3.3 V, I _{OL} = 8.0 mA) | | | 0.4 | V |
| V _{OH} | Output HIGH Voltage (V _{DD} = 3.3 V, I _{OH} = 8.0 mA) | 2.5 | | | V |
| I _{DD} | Static Supply Current (Note 4) | | 1.1 | | mA |
| I _{CC} | Dynamic Supply Current (3.3 V, 10 MHz, and No Load) | | 3.5 | | mA |
| V _{DD} | Operating Voltage | 2.7 | 3.3 | 3.6 | V |
| t _{ON} | Powerup Time (first locked cycle after powerup) (Note 5) | | | 5.0 | mS |
| Z _{OUT} | Clock Output Impedance | | 45 | | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. XIN/CLKIN pin is pulled low.
5. V_{DD} and XIN/CLKIN input are stable.

Table 7. AC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY

| Symbol | Description | Min | Typ | Max | Unit |
|--------------------------|--|-----|-----|----------------|------|
| CLKIN | Input Frequency | 6.0 | | 13 | MHz |
| ModOUT | Output Frequency | 6.0 | | 13 | MHz |
| f _d | Frequency Deviation Input Frequency = 6.0 MHz Input Frequency = 13 MHz | | | ±1.47 ±0.72 | % |
| t _{LH} (Note 6) | Output Rise Time (measured at 0.8 V to 2.0 V) | 0.4 | 1.2 | 1.5 | ns |
| t _{HL} (Note 6) | Output Fall Time (measured at 2.0 V to 0.8 V) | 0.4 | 1.0 | 1.2 | ns |
| t _{JC} | Jitter (Cycle-to-Cycle) | | | 200 | ps |
| t _D | Output Duty Cycle | 45 | 50 | 55 | % |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. t_{LH} and t_{HL} are measured at capacitive load of 15 pF.

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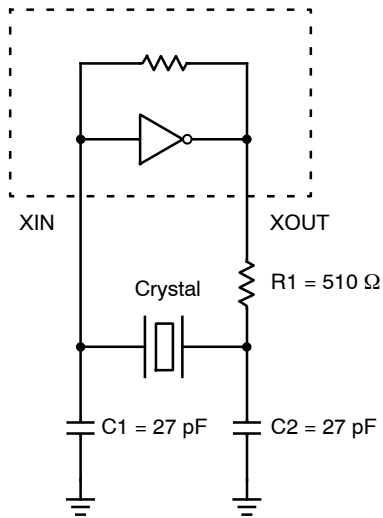


Figure 4. Typical Crystal Oscillator Circuit

Table 8. TYPICAL CRYSTAL SPECIFICATIONS

| Fundamental AT Cut Parallel Resonant Crystal | |
|--|---------------------------|
| Nominal Frequency | 8.0 MHz |
| Frequency Tolerance | ±50 ppm or better at 25°C |
| Operating Temperature Range | -25°C to +85°C |
| Storage Temperature | -40°C to +85°C |
| Load Capacitance | 18 pF |
| Shunt Capacitance | 7 pF Maximum |
| ESR | 25 Ω |

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ORDERING INFORMATION

| Device | Marking | Temperature Range | Package | Shipping [†] | Availability |
|--------------|---------|-------------------|------------------------------------|-----------------------|---|
| NB2969ASNR2 | E0C | 0°C - 70°C | TSOP-6 (TSOT-23-6) | 2500 Tape & Reel | <i>Now</i> |
| NB2969ASNR2G | E0C | 0°C - 70°C | TSOP-6 (TSOT-23-6) (Pb-Free) | 2500 Tape & Reel | <i>Contact Sales Representative</i> |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

TSOP-6 CASE 318G-02 ISSUE V

DATE 12 JUN 2012



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.01 | 0.06 | 0.10 |
| b | 0.25 | 0.38 | 0.50 |
| c | 0.10 | 0.18 | 0.26 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.50 | 2.75 | 3.00 |
| E1 | 1.30 | 1.50 | 1.70 |
| e | 0.85 | 0.95 | 1.05 |
| L | 0.20 | 0.40 | 0.60 |
| L2 | 0.25 BSC | | |
| M | 0° | - | 10° |

- | | | | | | |
|--|--|---|---|---|--|
| <p>STYLE 1: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN</p> | <p>STYLE 2: PIN 1. EMITTER 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. BASE 2 6. COLLECTOR 2</p> | <p>STYLE 3: PIN 1. ENABLE 2. N/C 3. R BOOST 4. Vz 5. V in 6. V out</p> | <p>STYLE 4: PIN 1. N/C 2. V in 3. NOT USED 4. GROUND 5. ENABLE 6. LOAD</p> | <p>STYLE 5: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2</p> | <p>STYLE 6: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR</p> |
| <p>STYLE 7: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. N/C 5. COLLECTOR 6. EMITTER</p> | <p>STYLE 8: PIN 1. Vbus 2. D(in) 3. D(in)+ 4. D(out)+ 5. D(out) 6. GND</p> | <p>STYLE 9: PIN 1. LOW VOLTAGE GATE 2. DRAIN 3. SOURCE 4. DRAIN 5. DRAIN 6. HIGH VOLTAGE GATE</p> | <p>STYLE 10: PIN 1. D(OUT)+ 2. GND 3. D(OUT)- 4. D(IN)- 5. VBUS 6. D(IN)+</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1/GATE 2</p> | <p>STYLE 12: PIN 1. I/O 2. GROUND 3. I/O 4. I/O 5. VCC 6. I/O</p> |
| <p>STYLE 13: PIN 1. GATE 1 2. SOURCE 2 3. GATE 2 4. DRAIN 2 5. SOURCE 1 6. DRAIN 1</p> | <p>STYLE 14: PIN 1. ANODE 2. SOURCE 3. GATE 4. CATHODE/DRAIN 5. CATHODE/DRAIN 6. CATHODE/DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 2. SOURCE 3. GATE 4. DRAIN 5. N/C 6. CATHODE</p> | <p>STYLE 16: PIN 1. ANODE/CATHODE 2. BASE 3. EMITTER 4. COLLECTOR 5. ANODE 6. CATHODE</p> | <p>STYLE 17: PIN 1. EMITTER 2. BASE 3. ANODE/CATHODE 4. ANODE 5. CATHODE 6. COLLECTOR</p> | |

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



- | | |
|--|---|
| <p>XXX = Specific Device Code A = Assembly Location Y = Year W = Work Week ■ = Pb-Free Package</p> | <p>XXX = Specific Device Code M = Date Code ○ = Pb-Free Package</p> |
|--|---|

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|------------------|-------------|--|
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| DESCRIPTION: | TSOP-6 | PAGE 1 OF 1 |

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