NCN2612B

6-Channel Differential 1:2 Switch for PCIe 2.0 and Display Port 1.1

The NCN2612B is a 6−Channel differential SPDT switch designed to route PCI Express Gen2 and/or DisplayPort 1.1a signals. Due to the ultra−low ON−state capacitance (2.1 pF typ) and resistance (8 Ω typ), this switch is ideal for switching high frequency signals up to a signal bit rate (BR) of 5 Gbps. This switch pinout is designed to be used in BTX form factor desktop PCs and is available in a space−saving 5x11x0.75 mm WQFN56 package. The NCN2612B uses 80% less quiescent power than other comparable PCIe switches.

Features

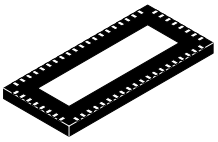
- BTX Pinout
- V_{DD} Power Supply from 3 V to 3.6 V
- Low Supply Current: 250 μA typ
- 6 Differential Channels, 2:1 MUX/DEMUX
- Compatible with Display Port 1.1a & PCIe 2.0
- Data Rate: Supports 5 Gbps
- Low R_{ON} Resistance: 8 Ω typ
- Low C_{ON} Capacitance: 2.1 pF
- Space Saving, Small WQFN−56 Package
- This is a Pb−Free Device

Typical Applications

- Notebook Computers
- Desktop Computers
- Server/Storage Networks

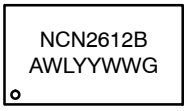
ON Semiconductor®

http://onsemi.com



WQFN56
CASE 510AK

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCN2612BMTTWG	WQFN56 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

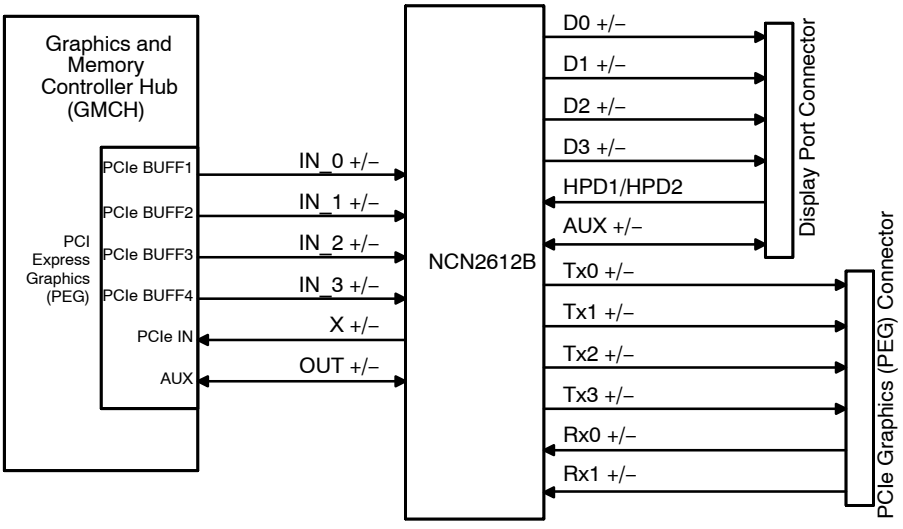


Figure 1. Application Schematic

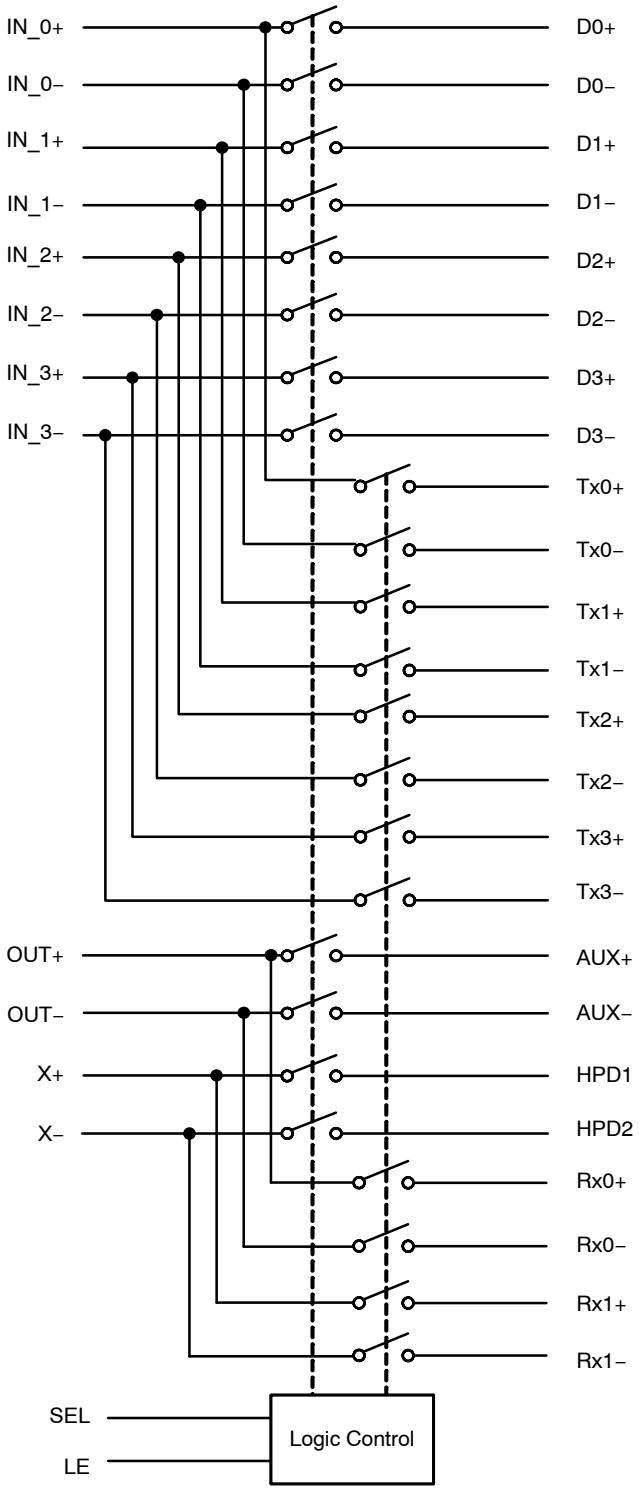


Figure 2. NCN2612B Block Diagram

TRUTH TABLE (SEL Control)

Function	SEL
PCI Express Gen2 Path is Active (Tx, Rx)	L
Digital Video Port is Active (D, HPD, AUX)	H

TRUTH TABLE (Latch Control)

LE	Internal Mux Select
L	Respond to Changes on SEL
H	Latched

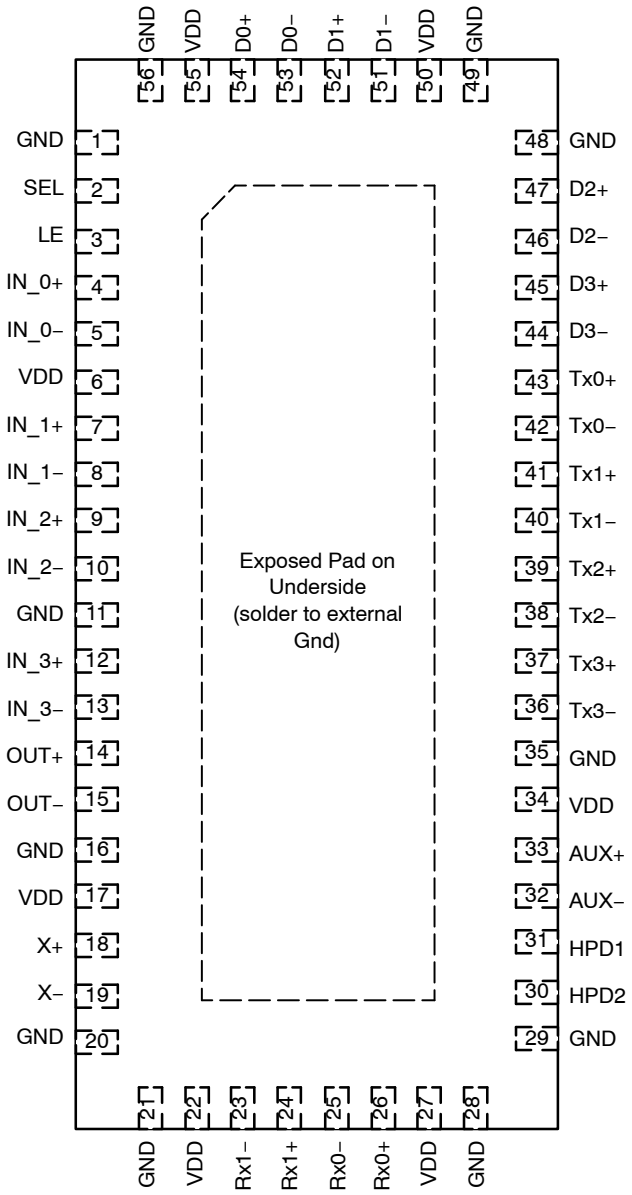


Figure 3. Pinout
(Top View)

PIN FUNCTION AND DESCRIPTION

Pin	Name	Description
6, 17, 22, 27, 34,50, 55	VDD	DC Supply, 3.3 V ±10%
1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56	GND	Power Ground.
Exposed Pad	–	The exposed pad on the backside of package is internally connected to Gnd. Externally the exposed pad should also be user−connected to GND.
2	SEL	SEL controls the mux through a flow−through latch. Do not float this pin. SEL = 0 for PCIE Mode; SEL = 1 for DP Mode
3	LE	LE controls the latch gate. Do not float this pin.
4	IN_0+	Differential input from GMCH PCIE outputs. IN_0+ makes a differential pair with IN_0−.
5	IN_0−	Differential input from GMCH PCIE outputs. IN_0− makes a differential pair with IN_0+.
7	IN_1+	Differential input from GMCH PCIE outputs. IN_1+ makes a differential pair with IN_1−.
8	IN_1−	Differential input from GMCH PCIE outputs. IN_1− makes a differential pair with IN_1+.
9	IN_2+	Differential input from GMCH PCIE outputs. IN_2+ makes a differential pair with IN_2−.
10	IN_2−	Differential input from GMCH PCIE outputs. IN_2− makes a differential pair with IN_2+.
12	IN_3+	Differential input from GMCH PCIE outputs. IN_3+ makes a differential pair with IN_3−.
13	IN_3−	Differential input from GMCH PCIE outputs. IN_3− makes a differential pair with IN_3+.
14	OUT+	Pass−through output from AUX+ input when SEL = 1. Pass−through output from Rx0+ input when SEL = 0.
15	OUT−	Pass−through output from AUX− input when SEL = 1. Pass−through output from Rx0− input when SEL = 0.
18	X+	X+ is an analog pass−through output corresponding to Rx1+.
19	X−	X− is an analog pass−through output corresponding to the Rx1− input. The path from Rx1− to X− must be matched with the path from Rx1+ to X+. X+ and X− form a differential pair when the pass−through mux mode is selected.
23	Rx1−	Differential input from PCIE connector or device. Rx1− makes a differential pair with Rx1+. Rx1− is passed through to the X− pin on the path that matches the Rx1+ to X+ pin.
24	Rx1+	Differential input from PCIE connector or device. Rx1+ makes a differential pair with Rx1−. Rx1+ is passed through to the X+ pin when SEL = 0.
25	Rx0−	Differential input from PCIE connector or device. Rx0− makes a differential pair with Rx0+. Rx0− is passed through to the OUT− pin when SEL = 0.
26	Rx0+	Differential input from PCIE connector or device. Rx0+ makes a differential pair with Rx0−. Rx0+ is passed through to the OUT+ pin when SEL = 0.
30	HPD2	Negative low frequency HPD input handshake protocol signal (normally not connected).
31	HPD1	Positive low frequency HPD input handshake protocol signal.
32	AUX−	Differential input from HDMI/DP connector. AUX− makes a differential pair with AUX+. AUX− is passed through to the OUT− pin when SEL = 1.
33	AUX+	Differential input from HDMI/DP connector. AUX+ makes a differential pair with AUX−. AUX+ is passed through to the OUT+ pin when SEL = 1.
37, 36	Tx3+, Tx3−	Analog pass−through output#2 corresponding to IN_3+ and IN_3− when SEL = 0.
39, 38	Tx2+, Tx2−	Analog pass−through output#2 corresponding to IN_2+ and IN_2− when SEL = 0.
41, 40	Tx1+, Tx1−	Analog pass−through output#2 corresponding to IN_1+ and IN_1− when SEL = 0.
43, 42	Tx0+, Tx0−	Analog pass−through output#2 corresponding to IN_0+ and IN_0− when SEL = 0.
45, 44	D3+, D3−	Analog pass−through output#1 corresponding to IN_3+ and IN_3−, when SEL = 1.
47, 46	D2+, D2−	Analog pass−through output#1 corresponding to IN_2+ and IN_2−, when SEL = 1.
52, 51	D1+, D1−	Analog pass−through output#1 corresponding to IN_1+ and IN_1−, when SEL = 1.
54, 53	D0+, D0−	Analog pass−through output#1 corresponding to IN_0+ and IN_0−, when SEL = 1.

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	−0.5 to 5.3	V_{DC}
Input/Output Voltage Range of the Switch (Tx, Rx, D, HPD, AUX, IN_, OUT, X)	V_{IS}	−0.5 to V_{DD} + 0.3	V_{DC}
Selection Pin Voltages (SEL and LE)	V_{IN}	−0.5 to V_{DD} + 0.3	V_{DC}
Continuous Current Through One Switch Channel	I_{IS}	±120	mA
Maximum Junction Temperature (Note 1)	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Thermal Resistance, Junction−to−Air (Note 2)	$R_{\theta JA}$	37	°C/W
Latch−up Current (Note 3)	I_{LU}	±100	mA
Human Body Model (HBM) ESD Rating (Note 4)	ESD HBM	7000	V
Machine Model (MM) ESD Rating (Note 4)	ESD MM	400	V
Moisture Sensitivity (Note 5)	MSL	Level 1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
2. This parameter is based on EIA/JEDEC 51−7 with a 4−layer PCB, 80 mm x 80 mm, two 1oz Cu material internal planes and top planes of 2oz Cu material.
3. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78.
4. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±7.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±400 V per JEDEC standard: JESD22−A115 for all pins.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (V_{DD} = +3.3V ±10%, T_A = −40°C to +85°C, unless otherwise noted. All Typical values are at V_{DD} = +3.3 V, T_A = +25°C, unless otherwise noted.)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
V_{DD}	Supply Voltage Range		3.0	3.3	3.6	V
I_{DD}	Power Supply Current	V_{DD} = 3.6 V, V_{IN} = GND or V_{DD}		250	350	μA
DATA SWITCH PERFORMANCE (for both PCIe and Display Port applications, unless otherwise noted)						
V_{IS}	Data Input/Output Voltage Range		0		1.2	V
R_{ON}	On Resistance (Tx, Rx)	V_{DD} = 3 V, V_{IS} = 0 V to 1.2 V, I_{IS} = 15 mA		8.0	13	Ω
R_{ON}	On Resistance (D, HPD, AUX)	V_{DD} = 3 V, V_{IS} = 0 V to 1.2 V, I_{IS} = 15 mA		9.0	13	Ω
$R_{ON(flat)}$	On Resistance Flatness	V_{DD} = 3 V, V_{IS} = 0 V to 1.2 V, I_{IS} = 15 mA (Note 6)		0.1	1.24	Ω
ΔR_{ON}	On Resistance Matching (Tx, Rx)	V_{DD} = 3 V, V_{IS} = 0 V, I_{IS} = 15 mA		0.35		Ω
ΔR_{ON}	On Resistance Matching (D, HPD, AUX)	V_{DD} = 3 V, V_{IS} = 0 V, I_{IS} = 15 mA		0.35		Ω
C_{ON}	On Capacitance	f = 1 MHz, Switch On, Open Output		2.1		pF
C_{OFF}	Off Capacitance	f = 1 MHz, Switch Off		1.6		pF
I_{ON}	On Leakage Current (IN_/ X/OUT)	V_{DD} = 3.6 V, $V_{IN\_}$ = Vx = V_{OUT} = 0 V, 1.2 V; Switch On to D/$\overline{HPD}$/AUX or Tx/Rx; outputs unconnected	−1		+1	μA
I_{OFF}	Off Leakage Current (D/Tx/HPD/Rx/AUX)	V_{DD} = 3.6 V, $V_{IN\_}$ = $V_{X\_}$ = $V_{OUT\_}$ = 0 V, 1.2 V; Switch Off; V_D = $\overline{V_{HPD}}$ = V_{AUX} or $\overline{V_D}$ = V_{HPD} = V_{AUX} set to 1.2 V, 0 V	−1		+1	μA
CONTROL LOGIC CHARACTERISTICS (SEL and LE pins)						
V_{IL}	Off voltage input		0		0.8	V
V_{IH}	High voltage input		2		V_{DD}	V
I_{IN}	Off voltage input	V_{IN} = 0 V or V_{DD}	−1		+1	μA
C_{IN}	High voltage input	f = 1 MHz		1		pF
DYNAMIC CHARACTERISTICS						
BR	Signal Data Rate			5		Gbps
D_{IL}	Differential Insertion Loss	f = 100 MHz		−0.7		dB
		f = 1.35 GHz		−1.3		
		f = 2.5 GHz		−1.9		
		f = 3.0 GHz		−1.9		
D_{ISO}	Differential Off Isolation	f = 100 MHz		−54		dB
		f = 1.35 GHz		−30		
		f = 2.5 GHz		−24		
		f = 3.0 GHz		−22		
		f = 5.0 GHz		−17		
D_{CTK}	Differential Crosstalk	f = 100 MHz		−50		dB
		f = 1.35 GHz		−32		
		f = 2.5 GHz		−27		
		f = 3.0 GHz		−25		
		f = 5.0 GHz		−25		
D_{RL}	Differential Return Loss	f = 100 MHz		−20		dB
		f = 1.35 GHz		−14		
		f = 2.5 GHz		−10		
		f = 3.0 GHz		−6		

6. Guaranteed by characterization and/or design.

SWITCHING CHARACTERISTICS (V_{DD} = +3.3 V, T_A = 25°C, unless otherwise specified)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
t_{b-b}	Bit−to−bit skew	Within the same differential pair		7		ps
t_{ch-ch}	Channel−to−channel skew	Maximum skew between all channels		55		ps

SELECTION PINS SWITCHING CHARACTERISTICS (V_{DD} = +3.3 V, T_A = 25°C, unless otherwise specified)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
T_{SELON}	SEL to Switch turn ON time	V_{IS} = 1 V, R_L = 50 Ω, V_{LE} = V_{DD}, C_L = 100 pF		9.5		ns
T_{SELOFF}	SEL to Switch turn OFF time	V_{IS} = 1 V, R_L = 50 Ω, V_{LE} = V_{DD}, C_L = 100pF		5		ns
T_{SET}	LE setup time SEL to LE	V_{IS} = 1 V, R_L = 50 Ω, V_{LE} = V_{DD}, C_L = 100 pF		1		ns
T_{HOLD}	LE hold time LE to SEL	V_{IS} = 1 V, R_L = 50 Ω, V_{LE} = V_{DD}, C_L = 100 pF		1		ns

TYPICAL OPERATING CHARACTERISTICS

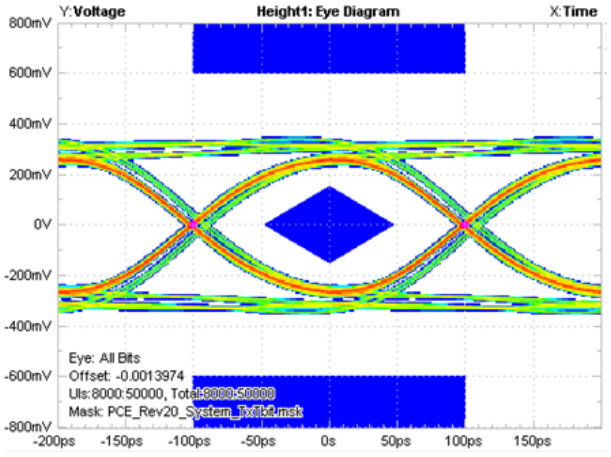


Figure 4. Eye Diagram for PCI Express at 5 Gbps, 800 mVpp Differential Swing (Minimum Case)

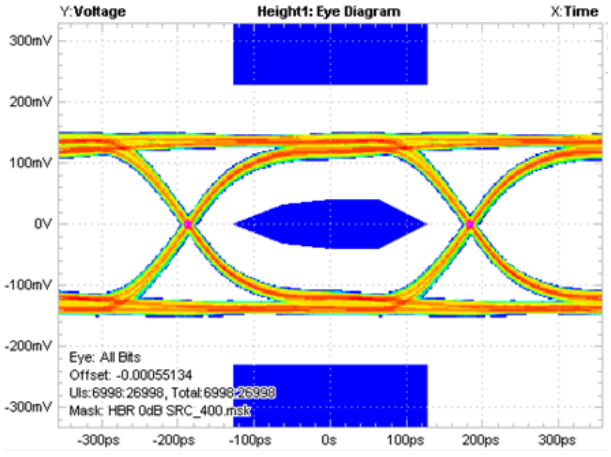


Figure 5. Eye Diagram for DisplayPort at 2.7 Gbps, 340 mVpp Differential Swing (Minimum Case)

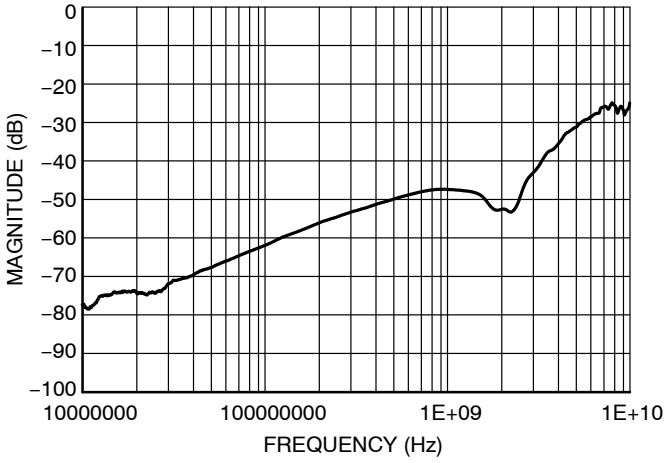


Figure 6. Differential Crosstalk

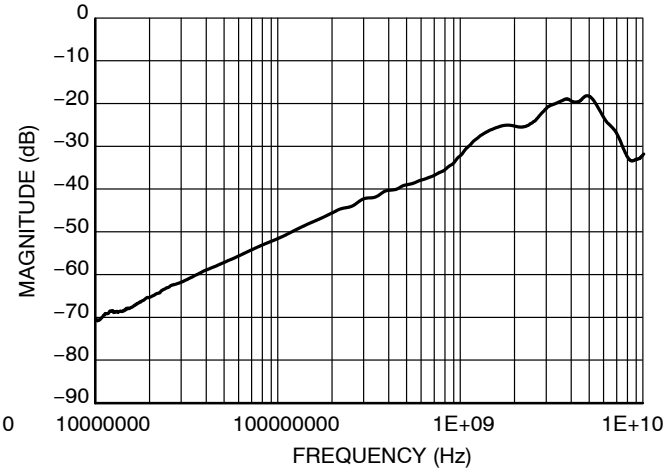


Figure 7. Differential Off Isolation

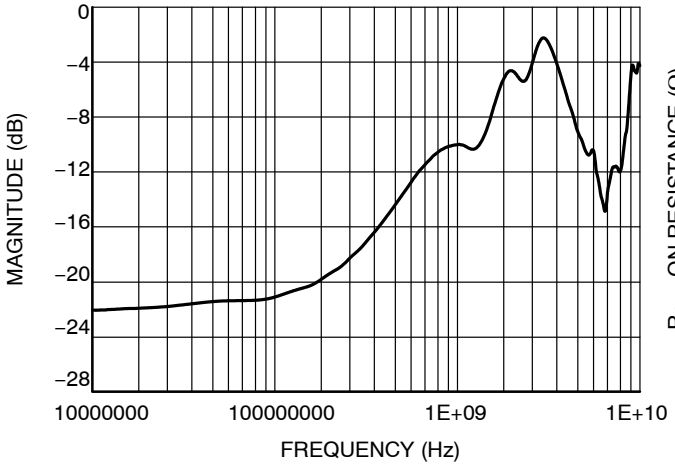


Figure 8. Differential Return Loss

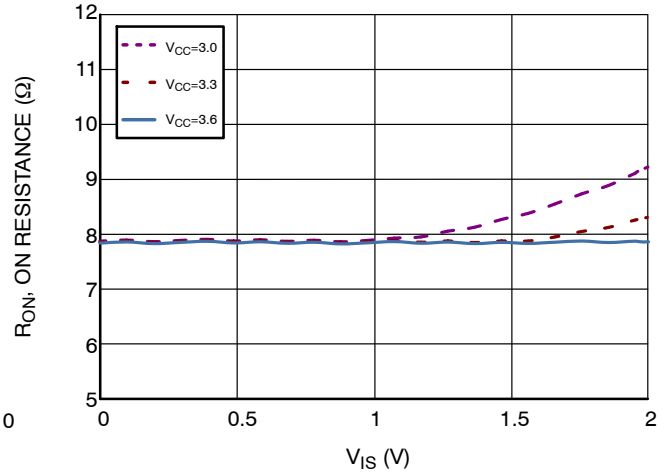


Figure 9. R_{ON} vs. V_{IS}

PARAMETER MEASUREMENT INFORMATION

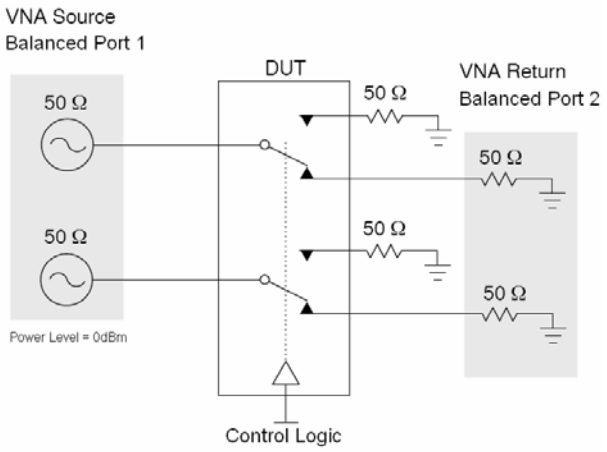


Figure 10. Differential Insertion Loss (S_{DD21}) and Differential Return Loss (S_{DD11})

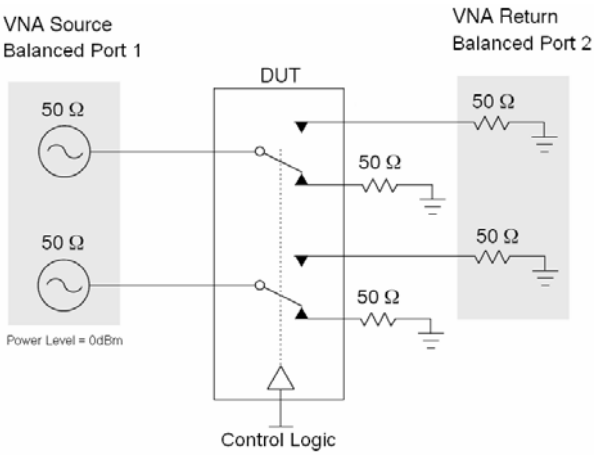


Figure 11. Differential Off Isolation (S_{DD21})

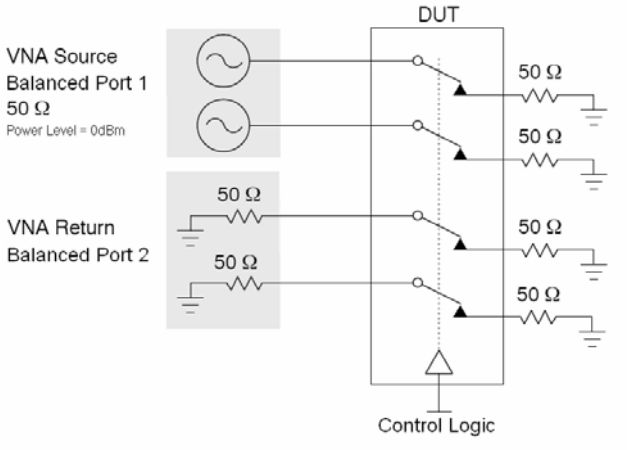
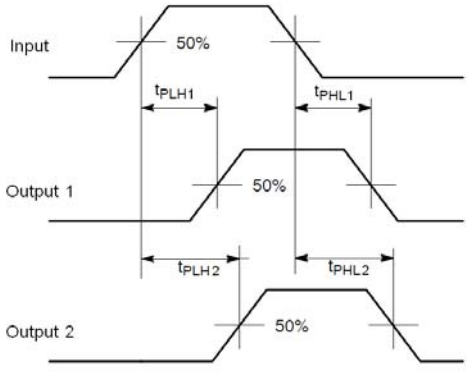
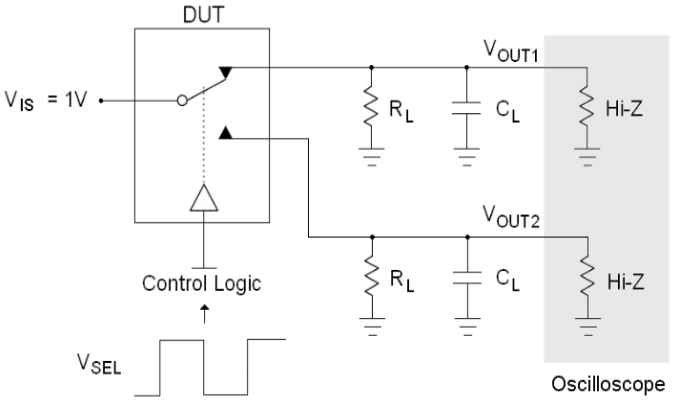


Figure 12. Differential Crosstalk (S_{DD21})



t_{skew} = $|t_{PLH1}-t_{PLH2}|$ or $|t_{PHL1}-t_{PHL2}|$

Figure 13. Bit−to−Bit and Channel−to−Channel Skew



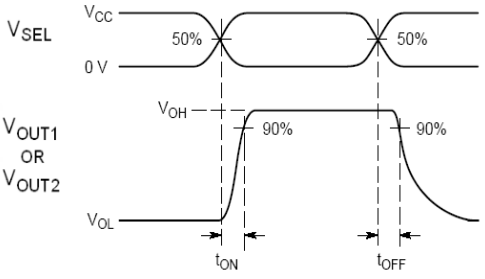


Figure 14. t_{ON} and t_{OFF}

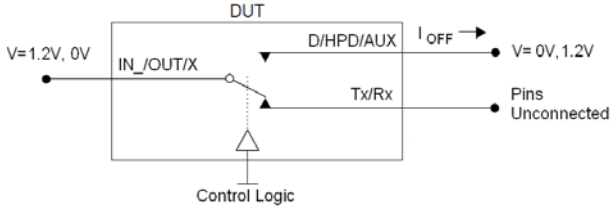


Figure 15. Off State Leakage

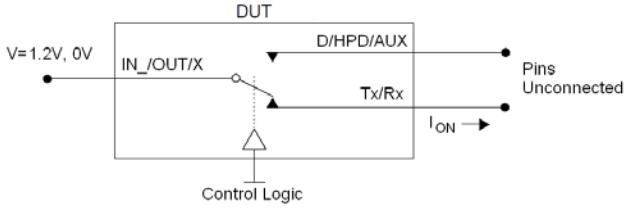


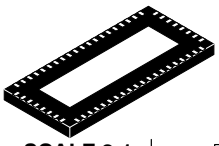
Figure 16. On State Leakage

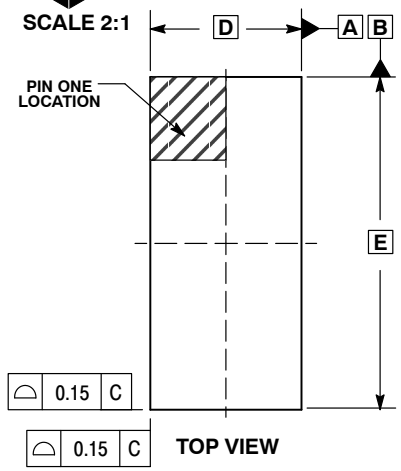
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

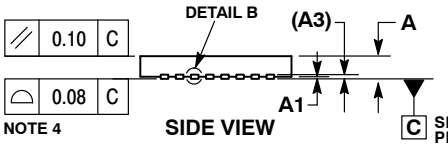
ON Semiconductor®

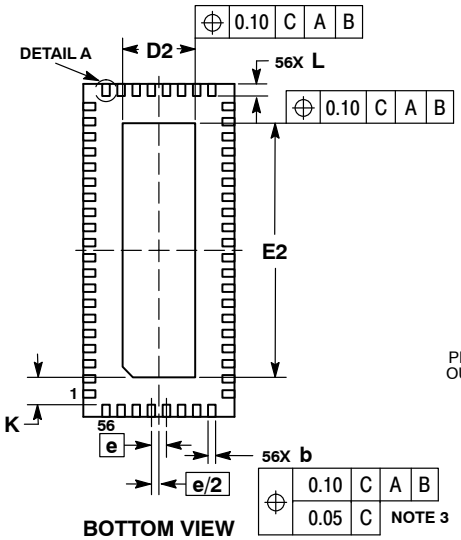
WQFN56 5x11, 0.5P
CASE 510AK−01
ISSUE A

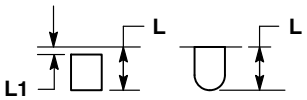
DATE 02 MAR 2010



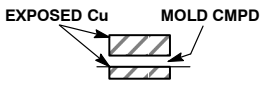








DETAIL A
ALTERNATE CONSTRUCTIONS

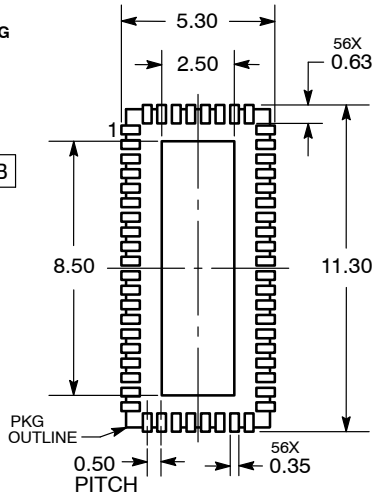


DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

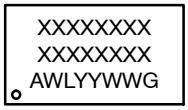
	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	−−−	0.05
A3	0.20 REF	
b	0.20	0.30
D	5.00 BSC	
D2	2.30	2.50
E	11.00 BSC	
E2	8.30	8.50
e	0.50 BSC	
K	0.20 MIN	
L	0.30	0.50
L1	−−−	0.15

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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DESCRIPTION:	**WQFN56 5x11, 0.5P**	**PAGE 1 OF 1**

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