# MC74VHCT139A

## Dual 2-to-4 Decoder/ Demultiplexer

The MC74VHCT139A is an advanced high speed CMOS 2−to−4 decoder/demultiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL devices while maintaining CMOS low power dissipation.

When the device is enabled ($\overline{E}$ = low), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device output is compatible with TTL−type input thresholds and the output has a full 5.0 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic−level translator from 3.0 V CMOS logic to 5.0 V CMOS logic, or from 1.8 V CMOS logic to 3.0 V CMOS logic while operating at the high−voltage power supply

The MC74VHCT139A input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74VHCT139A to be used to interface 5.0 V circuits to 3.0 V circuits. The output structures also provide protection when $V_{CC}$ = 0 V. These input and output structures help prevent device destruction caused by supply voltage−input/output voltage mismatch, battery backup, hot insertion, etc.
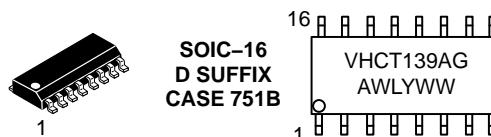
### Features

- High Speed: $t_{PD}$ = 5.0 ns (Typ) at $V_{CC}$ = 5.0 V
- Low Power Dissipation: $I_{CC}$ = 4 μA (Max) at $T_A$ = 25°C
- TTL−Compatible Inputs: $V_{IL}$ = 0.8 V; $V_{IH}$ = 2.0 V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP}$ = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
    - Human Body Model > 2000 V;
    - Machine Model > 200 V
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant

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### MARKING DIAGRAMS

**SOIC−16**
**D SUFFIX**
**CASE 751B**

```
16
VHCT139AG
AWLYWW
1
```

**TSSOP−16**
**DT SUFFIX**
**CASE 948F**

```
16
VHCT
139A
ALYW■
1
```

| A | = Assembly Location |
| WL, L | = Wafer Lot |
| Y | = Year |
| WW, W | = Work Week |
| G or ■ | = Pb−Free Package |

(Note: Microdot may be in either location)

### FUNCTION TABLE

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| $\overline{E}$ | A1 | A0 | $\overline{Y0}$ | $\overline{Y1}$ | $\overline{Y2}$ | $\overline{Y3}$ |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.
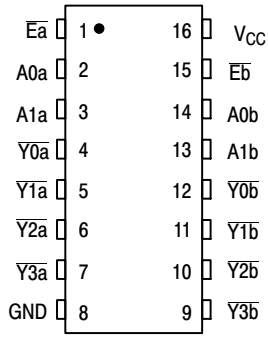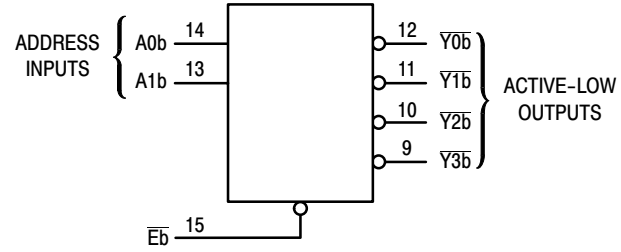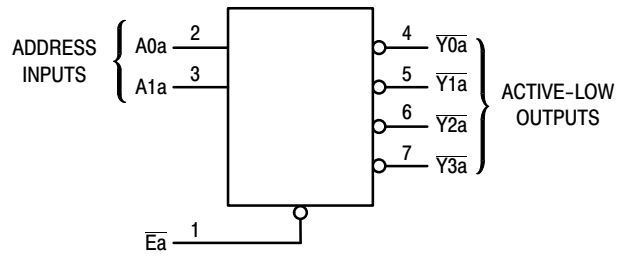
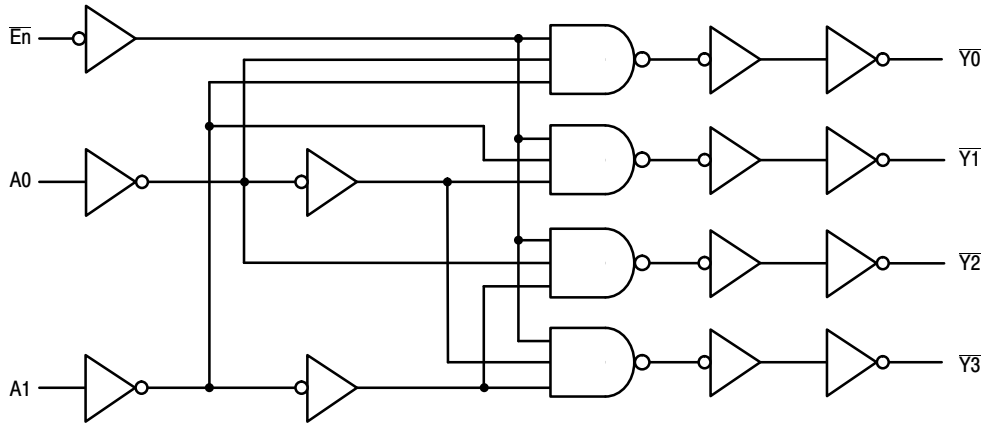# MC74VHCT139A



**Figure 1. Pin Assignment**



**Figure 2. Logic Diagram**
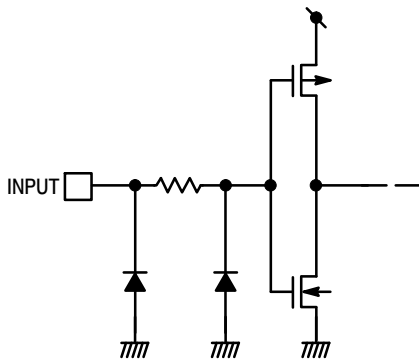


**Figure 3. Expanded Logic Diagram**
(1/2 of Device)



**Figure 4. Input Equivalent Circuit**
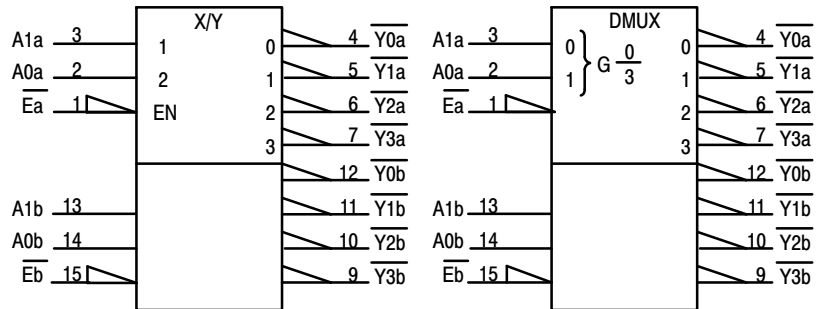


**Figure 5. IEC Logic Diagram**

# MC74VHCT139A

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| V$_{CC}$ | Positive DC Supply Voltage | | −0.5 to +7.0 | V |
| V$_{IN}$ | Digital Input Voltage | | −0.5 to +7.0 | V |
| V$_{OUT}$ | DC Output Voltage | Output in 3−State<br>High or Low State | −0.5 to +7.0<br>−0.5 to V$_{CC}$ +0.5 | V |
| I$_{IK}$ | Input Diode Current | | −20 | mA |
| I$_{OK}$ | Output Diode Current | | ± 20 | mA |
| I$_{OUT}$ | DC Output Current, per Pin | | ± 25 | mA |
| I$_{CC}$ | DC Supply Current, V$_{CC}$ and GND Pins | | ± 75 | mA |
| P$_D$ | Power Dissipation in Still Air | SOIC<br>TSSOP | 200<br>180 | mW |
| T$_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| V$_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 1)<br>Machine Model (Note 2)<br>Charged Device Model (Note 3) | >2000<br>>200<br>>2000 | V |
| I$_{LATCHUP}$ | Latchup Performance | Above V$_{CC}$ and Below GND at 125°C (Note 4) | ± 300 | mA |
| θ$_{JA}$ | Thermal Resistance, Junction−to−Ambient | SOIC<br>TSSOP | 143<br>164 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | | Min | Max | Unit |
|---|---|---|---|---|---|
| V$_{CC}$ | DC Supply Voltage | | 4.5 | 5.5 | V |
| V$_{IN}$ | DC Input Voltage | | 0 | 5.5 | V |
| V$_{OUT}$ | DC Output Voltage  Output in 3−State<br>High or Low State | | 0<br>0 | 5.5<br>V$_{CC}$ | V |
| T$_A$ | Operating Temperature Range, all Package Types | | −55 | 125 | °C |
| t$_r$, t$_f$ | Input Rise or Fall Time | V$_{CC}$ = 5.0 V ± 0.5 V | 0 | 20 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DEVICE JUNCTION TEMPERATURE VERSUS TIME
## TO 0.1% BOND FAILURES

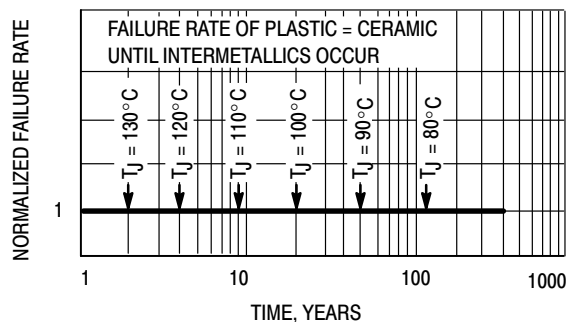| Junction<br>Temperature °C | Time, Hours | Time, Years |
|---|---|---|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |



**Figure 6. Failure Rate vs. Time Junction Temperature**

# MC74VHCT139A

## DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | $V_{CC}$ (V) | $T_A = 25°C$ Min | Typ | Max | $T_A ≤ 85°C$ Min | Max | $T_A = -55$ to $125°C$ Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High–Level Input Voltage | | 4.5 to 5.5 | 2 | | | 2 | | 2 | | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | | 4.5 to 5.5 | | | 0.8 | | 0.8 | | 0.8 | V |
| $V_{OH}$ | Maximum High–Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -50$ μA | 4.5 | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -8$ mA | 4.5 | 3.94 | | | 3.8 | | 3.66 | | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50$ μA | 4.5 | | 0 | 0.1 | | 0.1 | | 0.1 | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = 8$ mA | 4.5 | | | 0.36 | | 0.44 | | 0.52 | |
| $I_{IN}$ | Input Leakage Current | $V_{IN} = 5.5$ V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND | 5.5 | | | 4.0 | | 40.0 | | 40.0 | μA |
| $I_{CCT}$ | Additional Quiescent Supply Current (per Pin) | Any one input: $V_{IN} = 3.4$ V All other inputs: $V_{IN} = V_{CC}$ or GND | 5.5 | | | 1.35 | | 1.5 | | 1.5 | μA |
| $I_{OPD}$ | Output Leakage Current | $V_{OUT} = 5.5$ V | 0 | | | 0.5 | | 5 | | 5 | μA |

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

| Symbol | Parameter | Test Conditions | | $T_A = 25°C$ Min | Typ | Max | $T_A ≤ 85°C$ Min | Max | $T_A = -55$ to $125°C$ Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, A to Y | $V_{CC} = 3.3 ± 0.3$ V | $C_L = 15$ pF $C_L = 50$ pF | | 7.2 9.7 | 11.0 14.5 | 1.0 1.0 | 13.0 16.5 | 1.0 1.0 | 13.0 16.5 | ns |
| | | $V_{CC} = 5.0 ± 0.5$ V | $C_L = 15$ pF $C_L = 50$ pF | | 5.0 6.5 | 7.2 9.2 | 1.0 1.0 | 8.5 10.5 | 1.0 1.0 | 8.5 10.5 | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, $\overline{E}$ to Y | $V_{CC} = 3.3 ± 0.3$ V | $C_L = 15$ pF $C_L = 50$ pF | | 6.4 8.9 | 9.2 12.7 | 1.0 1.0 | 11.0 14.5 | 1.0 1.0 | 11.0 14.5 | ns |
| | | $V_{CC} = 5.0 ± 0.5$ V | $C_L = 15$ pF $C_L = 50$ pF | | 4.4 5.9 | 6.3 8.3 | 1.0 1.0 | 7.5 9.5 | 1.0 1.0 | 7.5 9.5 | |
| $C_{IN}$ | Maximum Input Capacitance | | | | 4 | 10 | | 10 | | 10 | pF |

| | | **Typical @ 25°C, $V_{CC} = 5.0$V** | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | 26 | pF |

5. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/2$ (per decoder). $C_{PD}$ is used to determine the no–load dynamic power consumption; $P_D = C_{PD} • V_{CC}^2 • f_{in} + I_{CC} • V_{CC}$.
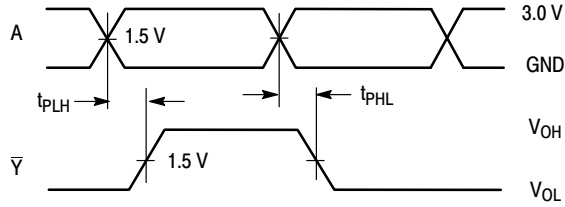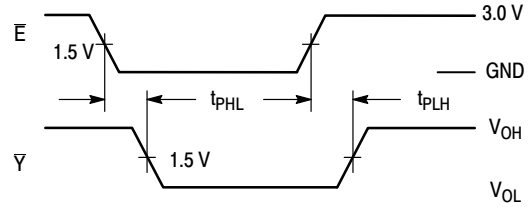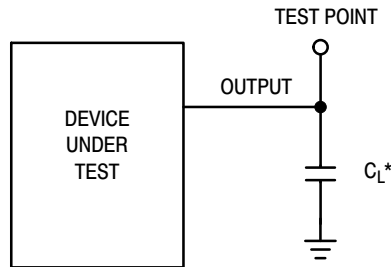
# MC74VHCT139A



Figure 7. Switching Waveform



Figure 8. Switching Waveform



*Includes all probe and jig capacitance

Figure 9. Test Circuit

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74VHCT139ADG | SOIC–16 (Pb–Free) | 48 Units / Rail |
| MC74VHCT139ADR2G | SOIC–16 (Pb–Free) | 2500 Tape & Reel |
| MC74VHCT139ADTG | TSSOP–16 (Pb–Free) | 96 Units / Rail |
| MC74VHCT139ADTRG | TSSOP–16 (Pb–Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

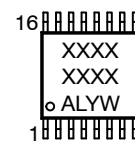**SOIC−16**
CASE 751B−05
ISSUE K

DATE 29 DEC 2006

SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N−CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P−CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P−CH
9. SOURCE P−CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N−CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N−CH

## SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

| DOCUMENT NUMBER: | 98ASB42566B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| DESCRIPTION: | SOIC−16 | | PAGE 1 OF 1 |

**TSSOP−16**
CASE 948F−01
ISSUE B

DATE 19 OCT 2006

16

1

**SCALE 2:1**

16X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

⬠ | 0.15 (0.006) | T | U Ⓢ

**2X L/2**

**L**

PIN 1
IDENT.

⬠ | 0.15 (0.006) | T | U Ⓢ

**A**
**−V−**

**B**
**−U−**

**K**
**K1**

**J1**

**J**

**SECTION N−N**

**N**

0.25 (0.010)

**M**

**N**

**F**

**DETAIL E**

**C**

⬠ | 0.10 (0.004)
**−T−** SEATING
PLANE

**D**

**G**

**H**

**DETAIL E**

**−W−**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

**SOLDERING FOOTPRINT**

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS
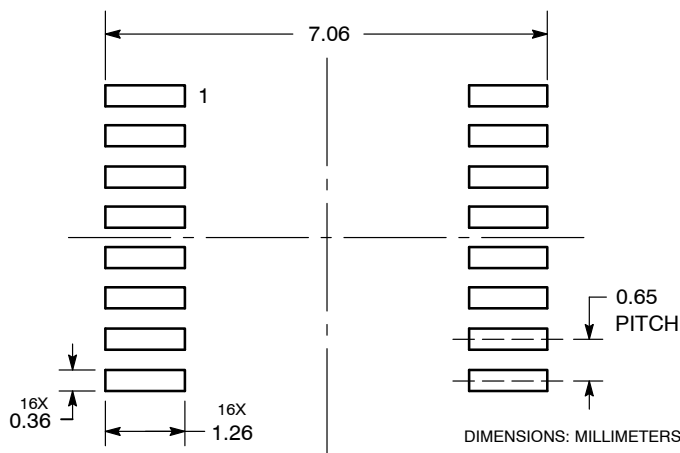
**GENERIC
MARKING DIAGRAM***

16

XXXX
XXXX
ALYW

1

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

| **DOCUMENT NUMBER:** | **98ASH70247A** | |
|---|---|---|
| **DESCRIPTION:** | **TSSOP−16** | **PAGE 1 OF 1** |

## PUBLICATION ORDERING INFORMATION

◊