MJW21193 (PNP)
MJW21194 (NPN)

Silicon Power Transistors

The MJW21193 and MJW21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

Features

- Total Harmonic Distortion Characterized
- High DC Current Gain
- Excellent Gain Linearity
- High SOA
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current − Continuous	I_C	16	Adc
Collector Current − Peak (Note 1)	I_{CM}	30	Adc
Base Current − Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.7	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	40	°C/W

ON Semiconductor®

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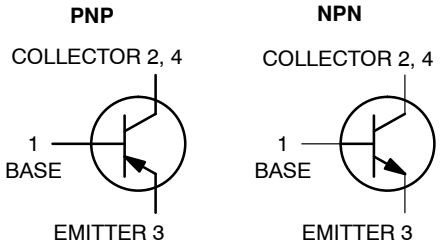
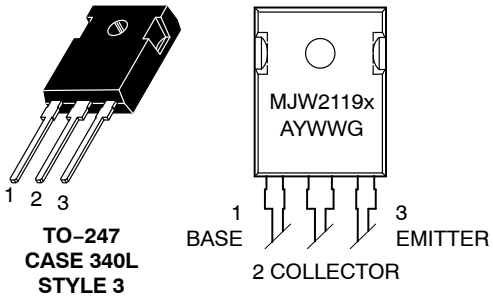
16 AMPERES
COMPLEMENTARY SILICON
POWER TRANSISTORS
250 VOLTS, 200 WATTS



MARKING DIAGRAM



TO−247
CASE 340L
STYLE 3

x = 3 or 4
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJW21193G	TO−247 (Pb−Free)	30 Units/Rail
MJW21194G	TO−247 (Pb−Free)	30 Units/Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	–	–	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	–	–	100	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	–	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non−repetitive)		4.0	–	–	
(V_{CE} = 80 Vdc, t = 1 s (non−repetitive)		2.25	–	–	
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				
(I_C = 8 Adc, V_{CE} = 5 Vdc)		20	–	80	
(I_C = 16 Adc, I_B = 5 Adc)		8	–	–	
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	–	–	2.2	Vdc
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)		–	–	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)		–	–	4	
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output	T_{HD}				%
V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched		–	0.8	–	
(Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched		–	0.08	–	
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	–	500	pF

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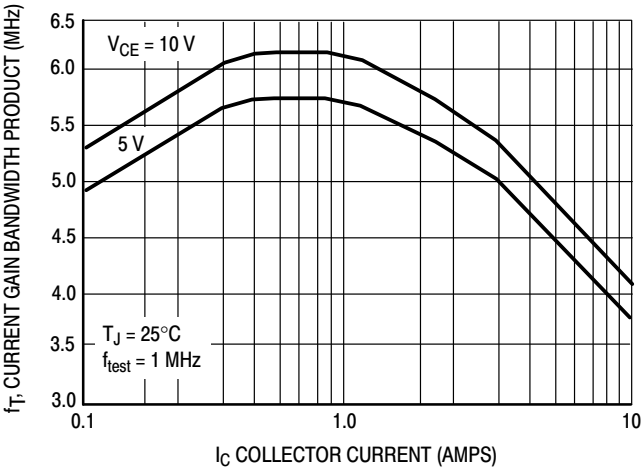

Figure 1. Typical Current Gain Bandwidth Product

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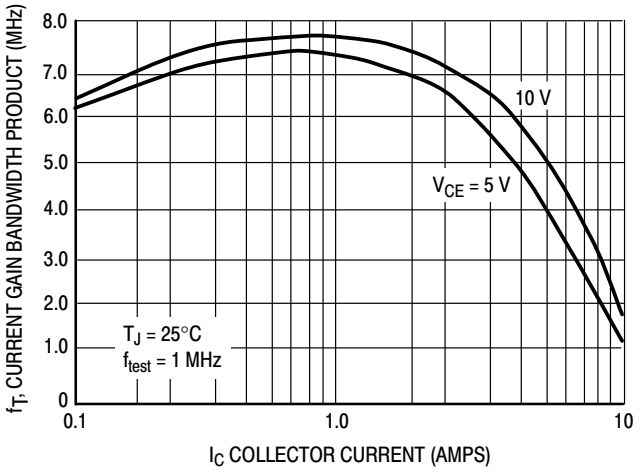

Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJW21193

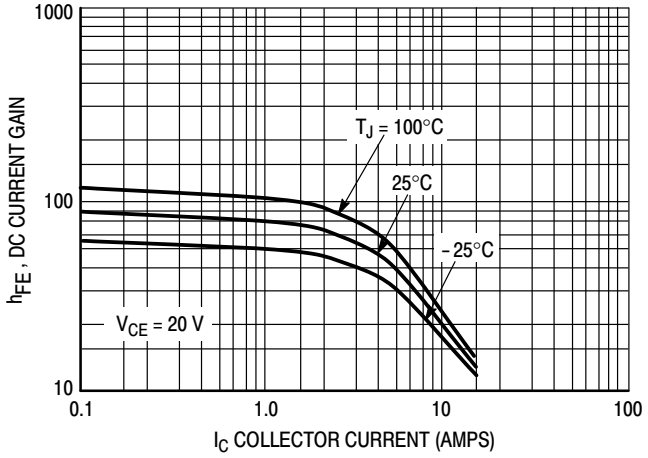

Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJW21194

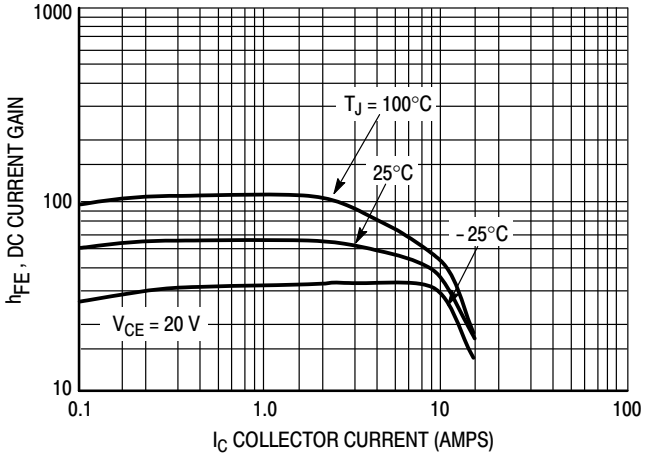

Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJW21193

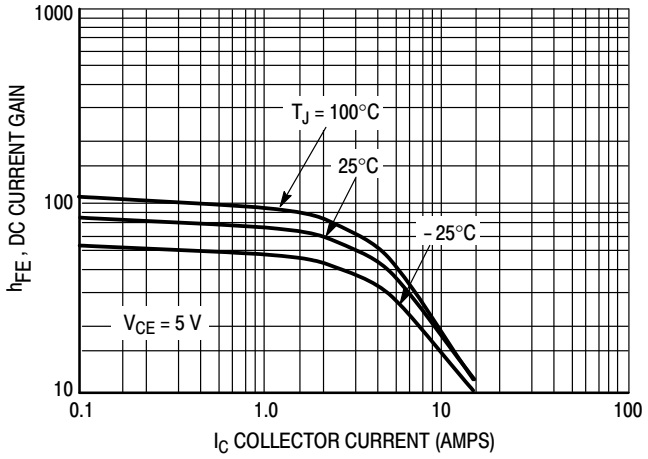

Figure 5. DC Current Gain, V_{CE} = 5 V

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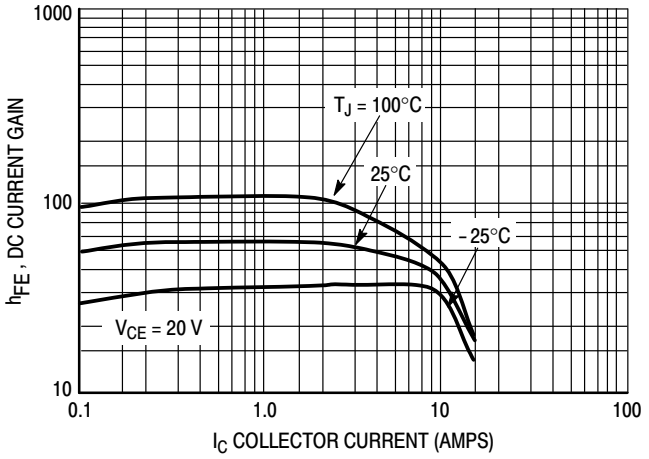

Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJW21193

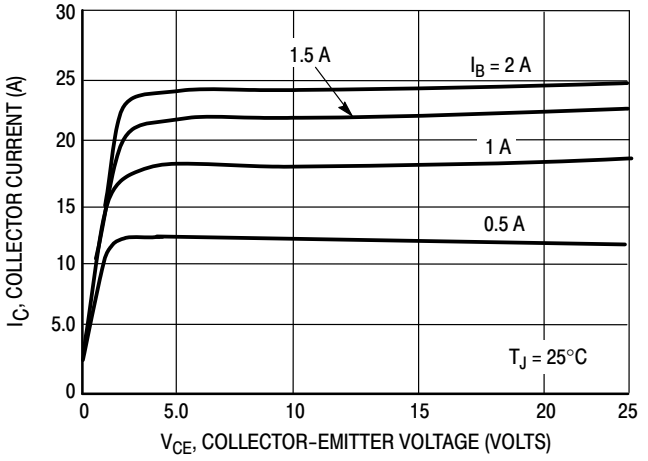

Figure 7. Typical Output Characteristics

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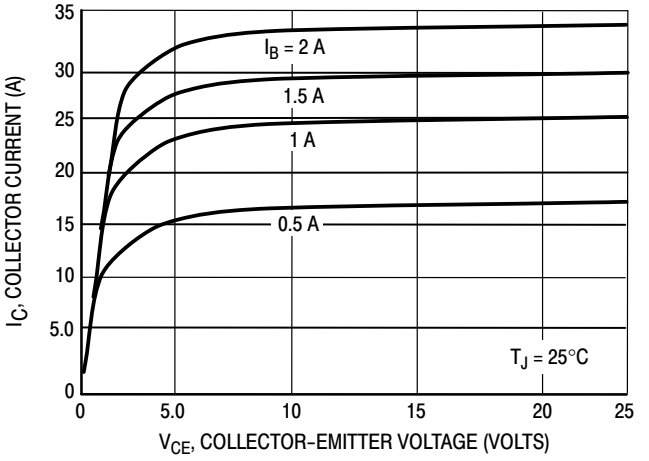

Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJW21193

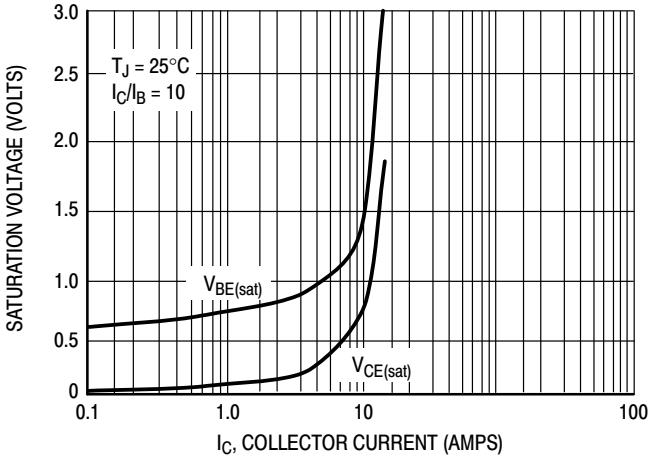

Figure 9. Typical Saturation Voltages

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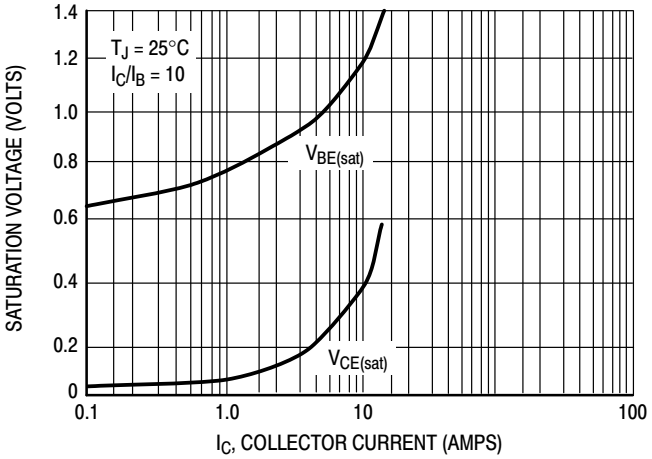

Figure 10. Typical Saturation Voltages

PNP MJW21193

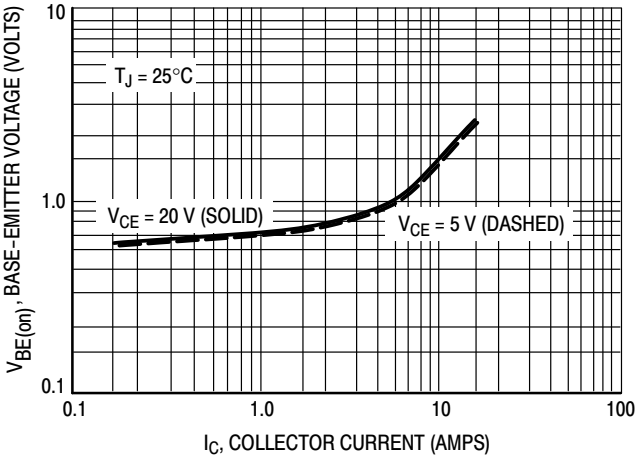

Figure 11. Typical Base−Emitter Voltage

NPN MJW21194

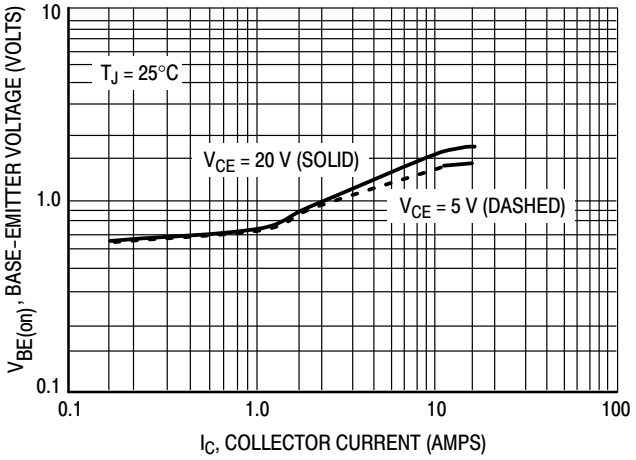

Figure 12. Typical Base−Emitter Voltage

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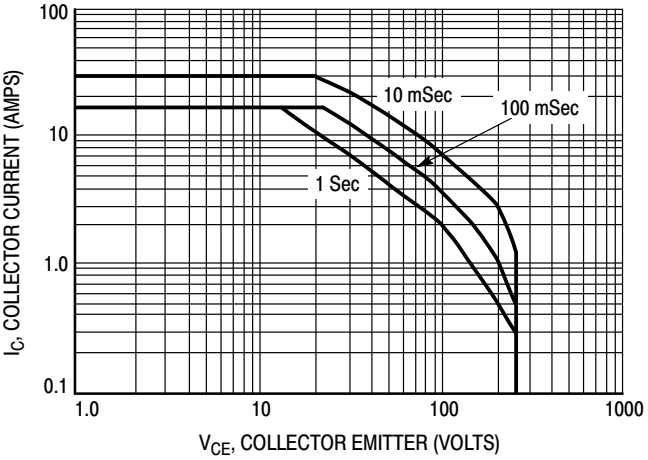

Figure 13. Active Region Safe Operating Area

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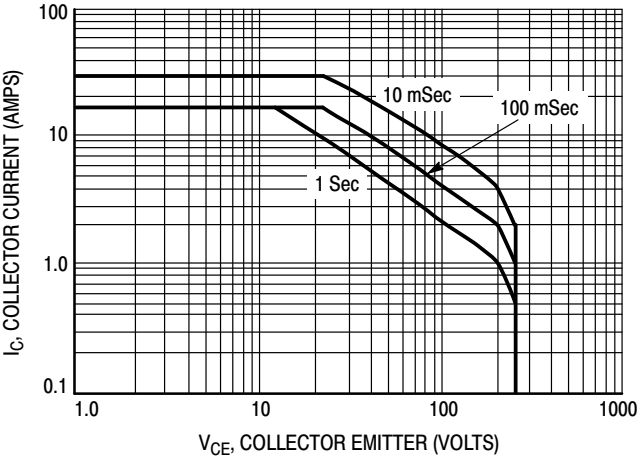


Figure 14. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

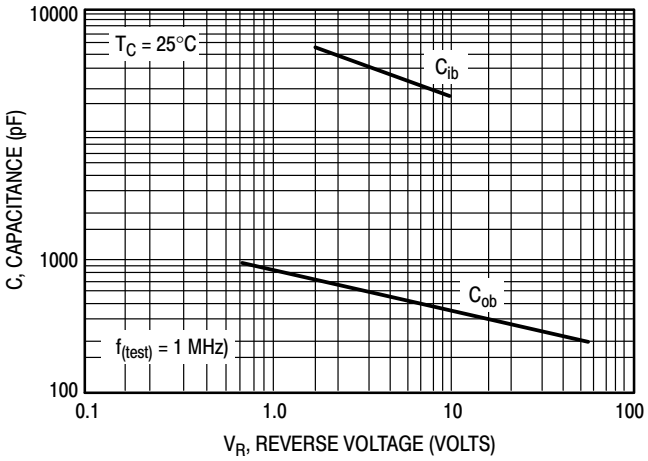


Figure 15. MJW21193 Typical Capacitance

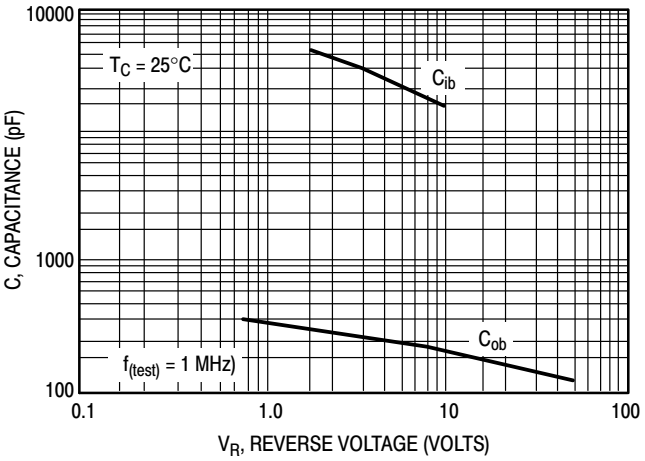


Figure 16. MJW21194 Typical Capacitance

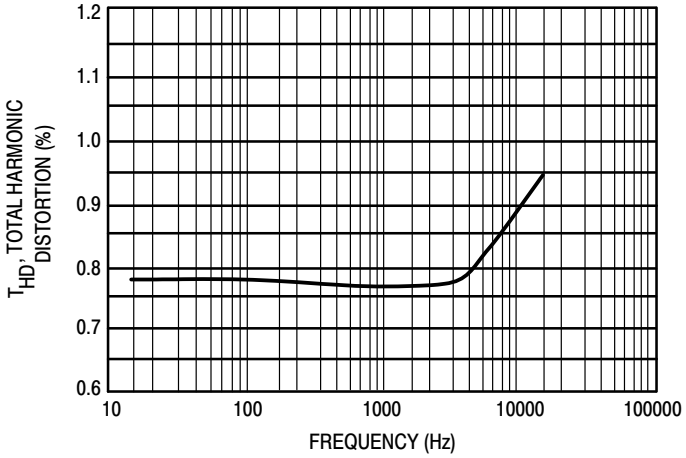


Figure 17. Typical Total Harmonic Distortion

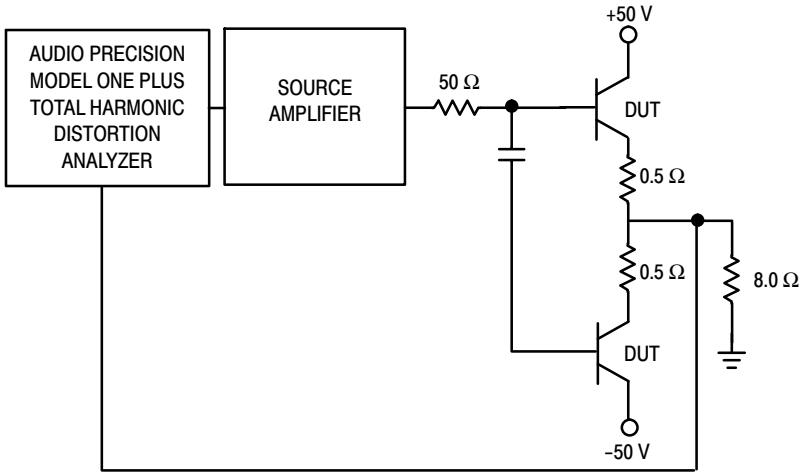


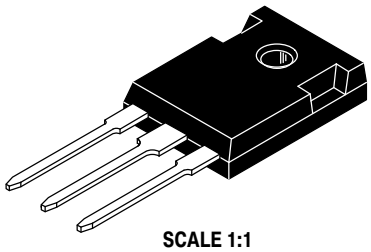
Figure 18. Total Harmonic Distortion Test Circuit

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

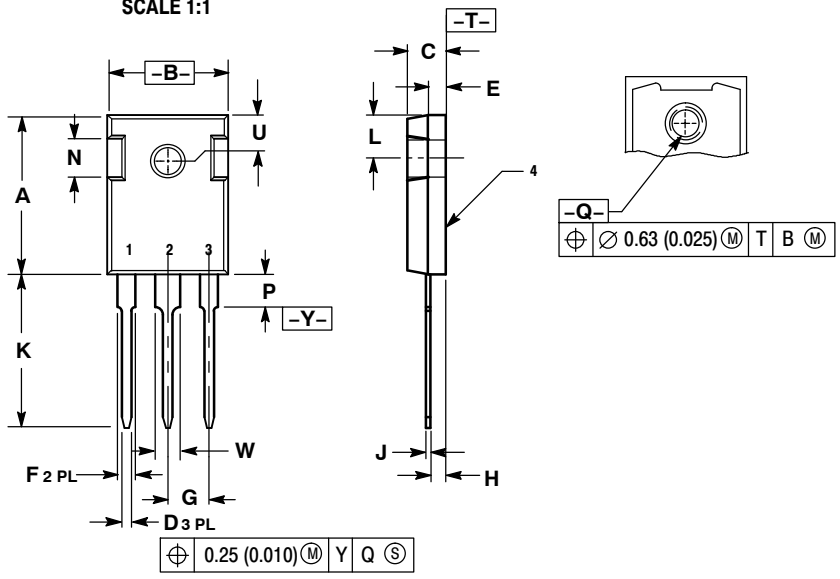
ON Semiconductor®

TO−247
CASE 340L−02
ISSUE F

DATE 26 OCT 2011



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	8.30
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)

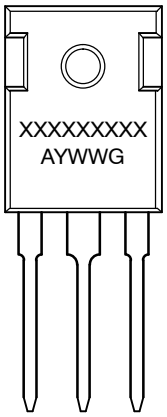
STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASB15080C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO−247	PAGE 1 OF 2

ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80–21.46/0.819–0.845. DIM K WAS 19.81–20.32/0.780–0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

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