# NCP1336A/B

# Quasi-Resonant Current Mode Controller for High Power Universal Off-Line Supplies

The NCP1336 hosts a high−performance circuitry aimed to powering quasi−resonant converters. Capitalizing on a novel valley−lockout system, the controller shifts gears and reduces the switching frequency as the power loading becomes lighter. This results in a stable operation despite switching events always occurring in the drain−source valley. This system works down to the 4th valley and toggles to a variable frequency mode beyond, ensuring an excellent standby power performance.

The controller takes benefit of a high−voltage start−up current source to provide a quick and lossless power−on sequence. To improve the safety in overload situations, the controller includes an Over Power Protection circuit which clamps the delivered power at high−line. Safety−wise, an adjustable timer relies on the feedback voltage to detect a fault. On version B, this fault triggers a triple−hiccup on the VCC pin which naturally reduces the average input power drawn by the converter. On version A, when a fault is detected, the controller is latched−off.

Particularly well suited for adapter applications, the controller features two latch inputs: one dedicated to Over Temperature protection (OTP) which offers an easy means to connect a pull−down temperature sensor like an NTC, and a second one more classical that can be used to perform an accurate Over Voltage Protection.

Finally, a brownout pin which stops the circuit operation in presence of a low mains condition is included.

### Features

- Quasi−Resonant Peak Current−Mode Control Operation
- Valley Switching Operation with Valley−Lockout for Noise−Immune Operation
- Internal 5 ms Soft−Start
- Loss−Free Adjustable Over Power Protection
- Auto−Recovery or Latched Internal Output Short− Circuit Protection
- Adjustable Timer for Improved Short−Circuit Protection
- Overvoltage and Overtemperature Protection Inputs
- Brownout Input
- −500 mA/+800 mA Peak Current Source/Sink Capability
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- 3 µs Blanking Delay to Ignore Leakage Ringing at Turn−Off
- Extremely Low No−Load and Standby Power
- SO14 Package
- These are Pb−Free Devices
- This Device uses Halogen−Free Molding Compound

### Typical Applications

- High Power ac−dc Converters for TVs, Set−Top Boxes etc
- Offline Adapters for Notebooks

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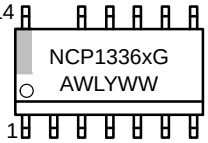
**QUASI−RESONANT PWM CONTROLLER FOR HIGH POWER AC−DC WALL ADAPTERS**

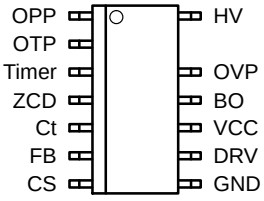

**SO−14**
**CASE 751AN**
**SUFFIX O**

**MARKING DIAGRAM**




| | |
|---|---|
| A | = Assembly Location |
| x | = A or B |
| WL | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

**PIN CONNECTIONS**




(Top View)

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 25 of this data sheet.

## PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Function | Pin Description |
|---|---|---|---|
| 1 | OPP | Adjust the Over Power Protection | A negative voltage applied to this pin reduces the internal maximum peak current setpoint. Connecting it to an auxiliary winding through a resistor divider thus performs Over Power compensation. If grounded, OPP is null. |
| 2 | OTP | Over−Temperature Protection | Connect an NTC between this pin and GND pin. Pin 2 features an internal current source that biases the NTC. When the NTC pulls the pin down, the circuit permanently latches−off. |
| 3 | Timer | Timer | Wiring a capacitor to ground helps selecting the timer duration. |
| 4 | ZCD | Zero Crossing Detection | Connected to the auxiliary winding, this pin detects the core reset event. |
| 5 | Ct | Timing Capacitor | A capacitor connected to this pin acts as the timing capacitor in foldback mode. |
| 6 | FB | Feedback Pin | Hooking an optocoupler collector to this pin will allow regulation. |
| 7 | CS | Current Sense | This pin monitors the primary peak current. |
| 8 | GND | − | This pin is the controller ground. |
| 9 | DRV | Driver Output | This pin is the driver's output to an external MOSFET. |
| 10 | VCC | Supplies the Controller | This pin is connected to an external auxiliary voltage. |
| 11 | BO | Brownout | This pin is the brownout input. |
| 12 | OVP | Over−Voltage Protection | By pulling this pin high, the controller can be permanently latched−off. |
| 13 | NC | − | This pin is omitted for improved creepage. |
| 14 | HV | High−Voltage Input | Connected to the bulk capacitor, this pin powers the internal current source to deliver a startup current. |

## OVERCURRENT PROTECTION ON NCP1336 VERSIONS

| | Auto−Recovery Overcurrent protection | Latched Overcurrent protection |
|---|---|---|
| NCP1336 / A | | X |
| NCP1336 / B | X | |

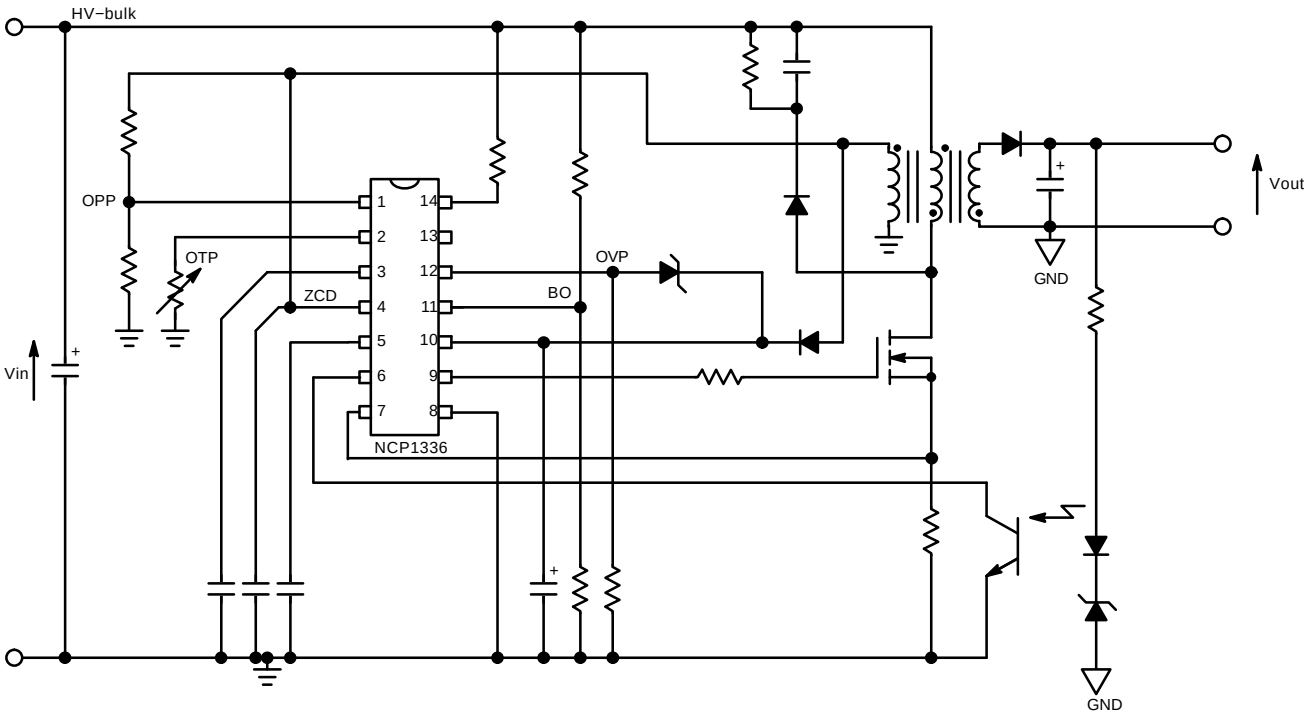



**Figure 1. Typical Application Example**

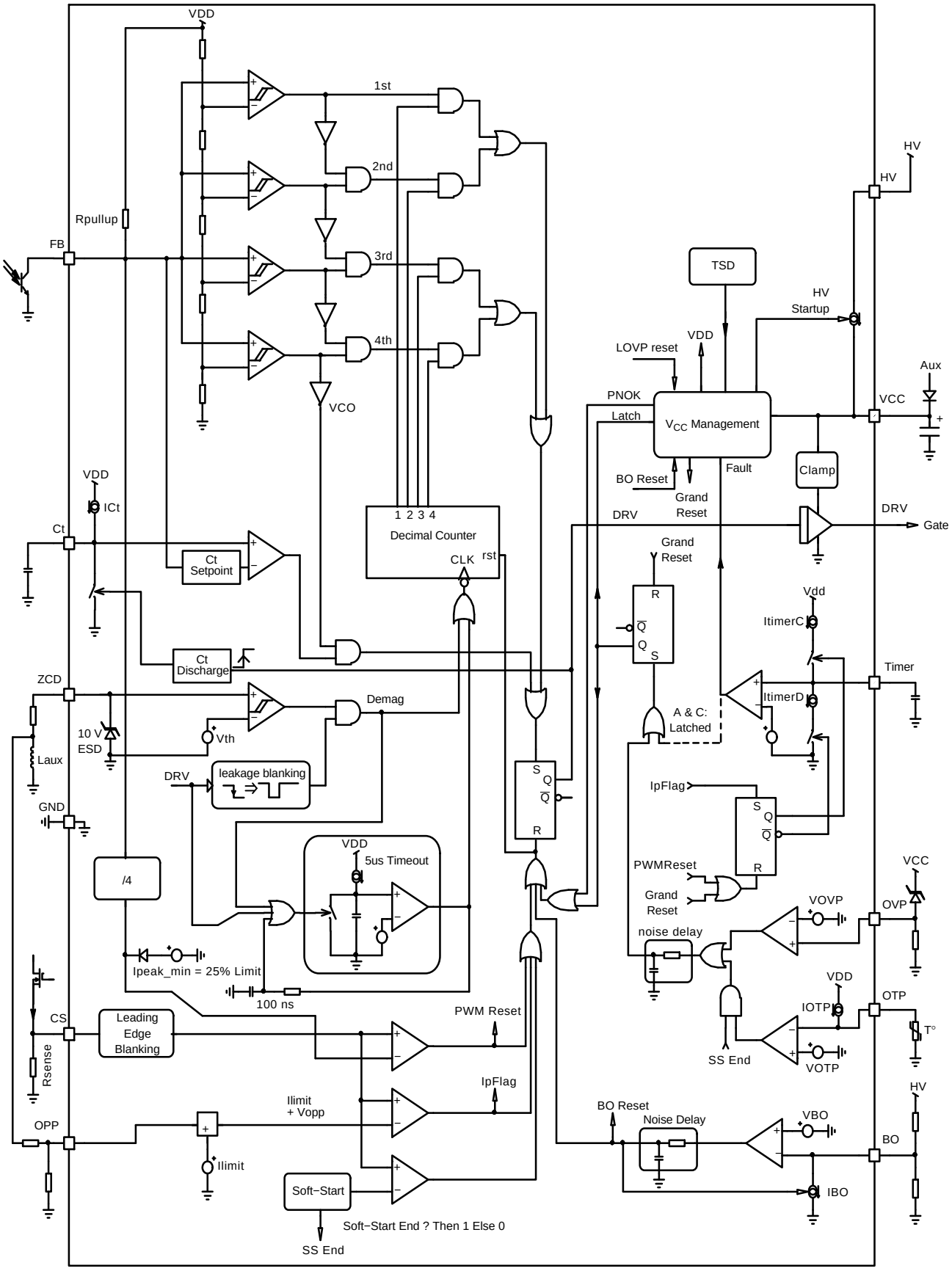



**Figure 2. Internal Circuit Architecture**

**MAXIMUM RATINGS TABLE**

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{CCmax}$<br>$I_{CCmax}$ | Maximum Power Supply voltage, $V_{CC}$ pin, continuous voltage<br>Maximum current for VCC Pin | −0.3 to 28<br>±30 | V<br>mA |
| $V_{HVmax}$<br>$I_{HVmax}$ | High voltage pin (pin 14) voltage range<br>Pin 14 current range | −0.3 to 500<br>±20 | V<br>mA |
| $V_{max}$<br>$I_{max}$ | Maximum voltage on low power pins (except pin 4, pin 9, pin 10 and pin 14)<br>Current range for low power pins (except pin 4, pin 9, pin 10 and pin 14) | −0.3 to 10<br>±10 | V<br>mA |
| $V_{ZDC,dc}$<br>$I_{ZDC,dc}$ | Maximum continuous voltage on pin 4<br>Maximum continuous current on pin 4 | −0.3 to 10<br>±10 | V<br>mA |
| $V_{ZDC,pulse}$<br>$I_{ZDC,pulse}$ | Maximum positive pulsed voltage (pulse duration below 100 μs) on pin 4<br>Maximum positive pulsed current (pulse duration below 100 μs) on pin 4 | +12<br>+3 | V<br>mA |
| $V_{OPPmax}$<br>$I_{OPPneg}$ | Recommended maximum operating voltage on pin OPP (pin 1)<br>Maximum negative current into OPP pin (pin 1) | −300<br>2 | mV<br>mA |
| $V_{DRV(MAX)}$ | Maximum DRV pin voltage when DRV is in High state | $V_{CC}$ + 1.0 | V |
| $R_{\theta JA}$ | Thermal Resistance Junction−to−Air | 120 | °C/W |
| $TJ_{MAX}$ | Maximum Junction Temperature | 150 | °C |
| | Storage Temperature Range | −60 to +150 | °C |
| | ESD Capability, HBM model (All pins except HV) (Note 1) | 2 | kV |
| | ESD Capability, Machine Model (All pins except DRV) (Note 1) | 200 | V |
| | ESD Capability, Machine Model (DRV pin) (Note 1) | 160 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection rated using the following tests: Human Body Model 2000 V per JEDEC standard JESD22, Method A114E. Machine Model Method 200 V per JEDEC standard JESD22, Method A115A.
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

## ELECTRICAL CHARACTERISTICS

(For typical values $T_J$ = 25°C, for min/max values $T_J$ = −40°C to +125°C, Max $T_J$ = 150°C, $V_{CC}$ = 12 V unless otherwise noted)

| Symbol | Rating | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **SUPPLY SECTION** | | | | | |
| $VCC_{on}$ | $V_{CC}$ increasing level at which the current source turns−off | 14 | 15 | 16 | V |
| $VCC_{min}$ | $V_{CC}$ level below which output pulses are stopped | 8 | 9 | 10 | V |
| $VCC_{reset}$ | Internal latch reset level | − | 5.5 | − | V |
| $I_{CC1}$ | Internal IC consumption, no output load on DRV pin (Fsw = 10 kHz) | − | 1.4 | 2.0 | mA |
| $ICC1_{light}$ | $I_{CC1}$ for a Feedback Voltage Equal to $VH_{VCO}$ (internal bias reduction), with $C_T$ = 220 pF (corresponding to an Fsw of about 20 kHz) | | 1.8 | | mA |
| ICC2 | Internal IC consumption, 1 nF output load on pin 9, Fsw = 65 kHz | − | 2.5 | 3.0 | mA |
| ICC3 | Internal IC consumption, hiccup phase ($VCC_{min}$ < $V_{CC}$ < $VCC_{on}$) | − | 0.45 | 0.6 | mA |
| **INTERNAL STARTUP CURRENT SOURCE ($T_J$ > 0°C)** (HV Pin Biased to 60 Vdc) | | | | | |
| IC2 | High−voltage current source, $V_{CC}$ = 10 V (Note 3) | 3 | 6 | 9 | mA |
| IC1 | High−voltage current source, $V_{CC}$ = 0 | 150 | 300 | 550 | μA |
| $V_{Th}$ | $V_{CC}$ transition level for IC1 to IC2 toggling point ($I_{HV}$ = 2.5 mA) | 0.3 | 0.7 | 0.9 | V |
| $I_{leak}$ | Leakage current for the high voltage source, $V_{HV(pin)}$ = 500 Vdc | 1 | 12 | 30 | μA |
| **DRIVE OUTPUT** | | | | | |
| $T_r$ | Output voltage rise−time @ $C_L$ = 1 nF, 10%−90% of a 12 V output signal | − | 40 | 75 | ns |
| $T_f$ | Output voltage fall−time @ $C_L$ = 1 nF, 10%−90% of a 12 V output signal | − | 25 | 60 | ns |
| $I_{source}$ | Source current capability at $V_{DRV}$ = 2 V | − | 500 | − | mA |
| $I_{sink}$ | Sink current capability at $V_{DRV}$ = 10 V | − | 800 | − | mA |
| $VDRV_{low}$ | DRV pin level at $V_{CC}$ close to $VCC_{min}$ with a 33 kΩ resistor to GND and a 1 nF capacitor to GND | 7.6 | − | − | V |
| $VDRV_{high}$ | DRV pin level at $V_{CC}$ = 28 V with a 1 nF capacitor to GND (Note 3) | − | − | 17 | V |
| **DEMAGNETIZATION INPUT** | | | | | |
| $V_{th}$ | Input threshold voltage ($V_{ZCD(pin)}$ decreasing) | 35 | 55 | 90 | mV |
| $V_H$ | Hysteresis ($V_{ZCD(pin)}$ increasing) | 15 | 35 | 55 | mV |
| $VC_H$<br>$VC_L$ | Input clamp voltage<br>High state ($I_{ZCD(pin)}$ = 3.0 mA)<br>Low state ($I_{ZCD(pin)}$ = −2.0 mA) | <br>8<br>−0.9 | <br>10<br>−0.7 | <br>12<br>0 | <br>V<br>V |
| $T_{dem}$ | Demag propagation delay ($V_{ZCD(pin)}$ decreasing from 4 V to −0.3 V) | − | 150 | 250 | ns |
| $C_{par}$ | Internal input capacitance at $V_{ZCD(pin)}$ = 1 V | − | 10 | − | pF |
| $T_{blank}$ | Blanking Delay after $t_{ON}$ | 2 | 3 | 4 | μs |
| $T_{out}$ | Timeout after last demag transition | 4 | 5.25 | 6.5 | μs |
| **CURRENT COMPARATOR** | | | | | |
| $I_{IB}$ | Input Bias Current @ 1 V input level on CS pin | − | 0.02 | − | μA |
| $I_{Limit1}$ | Maximum internal current setpoint – $T_J$ = 25°C – OPP pin grounded | 0.76 | 0.8 | 0.84 | V |
| $I_{Limit2}$ | Maximum internal current setpoint – $T_J$ from −40°C to 125°C – OPP pin grounded | 0.744 | 0.8 | 0.856 | V |
| Ipeak_VCO | Percentage of maximum peak current level at which VCO takes over (Note 4) | 22 | 25 | 28 | % |
| $T_{DEL}$ | Propagation delay from current detection to gate OFF state | − | 100 | 160 | ns |
| $T_{LEB}$ | Leading Edge Blanking Duration<br>$T_J$ = −5°C to +125°C<br>$T_J$ = −40°C to +125°C | <br>240<br>240 | <br>295<br>295 | <br>350<br>360 | ns |

3. Minimum value for $T_J$ = 125°C.
4. The peak current setpoint goes down as the load decreases. It is frozen below Ipeak_VCO (Ipeak = cst)
5. If negative voltage in excess to −300 mV is applied to OPP pin, the current setpoint decrease is no longer guaranteed to be linear.
6. NTC on OTP pin with R = 8.8 kΩ at 110°C.

## ELECTRICAL CHARACTERISTICS

(For typical values $T_J$ = 25°C, for min/max values $T_J$ = −40°C to +125°C, Max $T_J$ = 150°C, $V_{CC}$ = 12 V unless otherwise noted)

| Symbol | Rating | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CURRENT COMPARATOR** | | | | | |
| $OPP_{max}$ | Setpoint decrease for $V_{OPP}$ = −300 mV (Note 5) | 35 | 37.5 | 40 | % |
| $OPP_S$ | Setpoint decrease for OPP pin shorted to ground | − | 0 | − | % |
| **TIMING CAPACITOR** | | | | | |
| $VCT_{max}$ | Maximum voltage on Ct capacitor, $V_{FB} < VFB_T$ | 5 | 5.5 | − | V |
| $I_{CT}$ | Source current (Ct pin grounded) $T_J$ = −5°C to +125°C<br>$T_J$ = −40°C to +125°C | 18<br>17.42 | 20<br>20 | 22<br>22 | μA |
| $VCT_{min}$ | Minimum voltage on Ct, discharge switch activated | − | − | 90 | mV |
| Ct | Recommended timing capacitor value | − | 220 | − | pF |
| **FEEDBACK SECTION** | | | | | |
| $R_{pullup}$ | Internal pullup resistor $T_J$ = −5°C to +125°C<br>$T_J$ = −40°C to +125°C | 16<br>15.5 | 18<br>18 | 24<br>24 | kΩ |
| $I_{ratio}$ | FB pin to current setpoint division ratio | 3.75 | 4 | 4.25 | |
| $VFB_T$ | FB pin threshold under which the Ct capacitor is clamped to $VCT_{MAX}$ | 0.26 | 0.3 | 0.34 | V |
| $VH_{2D}$ | FB voltage where 1st valley ends and 2nd valley starts ($V_{FB}$ decreasing) | 1.316 | 1.4 | 1.484 | V |
| $VH_{3D}$ | FB voltage where 2nd valley ends and 3rd valley starts ($V_{FB}$ decreasing) | 1.128 | 1.2 | 1.272 | V |
| $VH_{4D}$ | FB voltage where 3rd valley ends and 4th valley starts ($V_{FB}$ decreasing) | 0.846 | 0.9 | 0.954 | V |
| $VH_{VCOD}$ | FB voltage where 4th valley ends and VCO starts ($V_{FB}$ decreasing) | 0.752 | 0.8 | 0.848 | V |
| $VH_{VCOI}$ | FB voltage where VCO ends and 4th valley starts ($V_{FB}$ increasing) | 1.316 | 1.4 | 1.484 | V |
| $VH_{4I}$ | FB voltage where 4th ends and 3rd valley starts ($V_{FB}$ increasing) | 1.504 | 1.6 | 1.696 | V |
| $VH_{3I}$ | FB voltage where 3rd ends and 2nd valley starts ($V_{FB}$ increasing) | 1.692 | 1.8 | 1.908 | V |
| $VH_{2I}$ | FB voltage where 2nd ends and 1st valley starts ($V_{FB}$ increasing) | 1.88 | 2 | 2.12 | V |
| **PROTECTIONS** | | | | | |
| $V_{OVP}$ | OVP level | 2.79 | 3 | 3.21 | V |
| $Tlatch_{del}$ | Delay before latch confirmation (noise immunity) | 15 | 20 | 25 | μs |
| Ilatch | Internal source current for OTP (Note 6) $T_J$ = −5°C to +125°C<br>$T_J$ = −40°C to +125°C | 85<br>82 | 93<br>93 | 97<br>98 | μA |
| $Ilatch_{110}$ | Internal source current for OTP @ 110°C (Note 6) | − | 91 | − | μA |
| $V_{OTP}$ | Fault detection level for OTP (Note 6) | 0.765 | 0.8 | 0.82 | V |
| VtimFault | Timer Level Completion | 4.65 | 5 | 5.35 | V |
| ItimerC | Timer capacitor charging current $T_J$ = −5°C to +125°C<br>$T_J$ = −40°C to +125°C | 8.5<br>8.25 | 10<br>10 | 11.5<br>11.5 | μA |
| ItimerD | Timer capacitor discharging current | 8.5 | 10 | 11.5 | μA |
| TimerL | Timer length, Ctimer = 0.1 μF typical | − | 50 | − | ms |
| TSS | Soft−start duration | − | 5 | − | ms |
| TSD | Temperature shutdown | 140 | − | − | °C |
| $TSD_{hys}$ | Temperature shutdown hysteresis | − | 40 | − | °C |

3. Minimum value for $T_J$ = 125°C.
4. The peak current setpoint goes down as the load decreases. It is frozen below Ipeak_VCO (Ipeak = cst)
5. If negative voltage in excess to −300 mV is applied to OPP pin, the current setpoint decrease is no longer guaranteed to be linear.
6. NTC on OTP pin with R = 8.8 kΩ at 110°C.

## ELECTRICAL CHARACTERISTICS

(For typical values $T_J$ = 25°C, for min/max values $T_J$ = −40°C to +125°C, Max $T_J$ = 150°C, $V_{CC}$ = 12 V unless otherwise noted)

| Symbol | Rating | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **BROWNOUT PROTECTION** | | | | | |
| VBO | Brownout level | 0.744 | 0.8 | 0.856 | V |
| IBO | Hysteresis Current, $V_{BO(pin)}$ < VBO $T_J$ = −5°C to +125°C<br>$T_J$ = −40°C to +125°C | 9<br>8.65 | 10<br>10 | 11<br>11 | μA |
| $TBO_{del}$ | Delay before BO confirmation (noise immunity) | 11 | 17 | 23 | μs |
| $IBO_{bias}$ | Brownout input bias current | − | 0.02 | − | μA |

3. Minimum value for $T_J$ = 125°C.
4. The peak current setpoint goes down as the load decreases. It is frozen below Ipeak_VCO (Ipeak = cst)
5. If negative voltage in excess to −300 mV is applied to OPP pin, the current setpoint decrease is no longer guaranteed to be linear.
6. NTC on OTP pin with R = 8.8 kΩ at 110°C.

## APPLICATION INFORMATION

**NCP1336** implements a standard current−mode architecture operating in quasi−resonant mode. Thanks to a novel circuitry, the controller prevents valley−jumping instability and steadily locks out in selected valley as the power demand goes down. Once the fourth valley is reached, the controller continues to reduce the frequency further down, offering excellent efficiency over a wide operating range. Thanks to a fault timer combined to an OPP circuitry, the controller is able to efficiently limit the output power at high−line.

- ***Quasi−Resonance Current−mode operation***: implementing quasi−resonance operation in peak current−mode control, the NCP1336 optimizes the efficiency by switching in the valley of the MOSFET drain−source voltage. Thanks to a novel circuitry, the controller locks−out in a selected valley and remains locked until the output loading significantly changes. This behavior is obtained by monitoring the feedback voltage. When the load becomes lighter, the feedback setpoint changes and the controller jumps into the next valley. It can go down to the $4^{th}$ valley if necessary. Beyond this point, the controller reduces its switching frequency by freezing the peak current setpoint. During quasi−resonance operation, in case of very damped valleys, a 5 μs timer adds the missing valleys.
- ***Frequency reduction in light−load conditions***: when the $4^{th}$ valley is left, the controller reduces the switching frequency which naturally improves the standby power by a reduction of all switching losses.
- ***Overpower protection (OPP)***: a negative voltage applied on OPP pin is directly added to the internal peak current setpoint. If this voltage is created from an auxiliary winding with flyback polarity, a direct image of the input voltage is subtracted from the internal clamp, thus reducing the peak current at high line. If the OPP pin is connected to ground no compensation is performed.
- ***Internal high−voltage startup switch***: reaching a low no−load standby power represents a difficult exercise when the controller requires an external, lossy, resistor connected to the bulk capacitor. Thanks to an internal logic, the controller disables the high−voltage current source after startup which no longer hampers the consumption in no−load situations.
- ***Internal soft−start***: a soft−start precludes the main power switch from being stressed upon start−up. Its duration is fixed and equal to 5 ms.
- ***OTP input***: thanks to an internal current source, the controller allows the direct connection of an NTC to ground. As soon as the pin is brought below VOTP by the NTC, the circuit permanently latches−off. During soft−start, the OTP comparator is masked to allow the voltage on pin OTP to rise above VOTP.
- ***OVP input***: thanks to an internal bias resistor to ground, the controller allows the direct connection of a zener diode (or a resistor divider for improved accuracy) to a monitored voltage. As soon as the pin is brought above VOVP, the controller latches−off.
- ***Short−circuit protection***: short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (where the auxiliary winding level does not properly collapse in presence of an output short). Here, when the internal 0.8 V maximum peak current limit is activated, the timer capacitor is charged. If the fault disappears, the timer capacitor is discharged by a current equal to the charging current. If the timer reaches completion while the error flag is still present, the controller stops the pulses and goes into a latch−off phase, operating in a low−frequency burst−mode via a *triple* hiccup operation. To limit the fault output power, a divide−by−three circuitry is installed on the $V_{CC}$ pin and requires *3 times* a start−up sequence before attempting to restart on version B. As soon as the fault disappears, the SMPS resumes operation. The latch−off phase can also be initiated, more classically, when $V_{CC}$ drops below $VCC_{min}$. On version A, the fault is latched.
- ***Brownout***: the NCP1336 includes a brownout circuit which safely stops the controller in case the input voltage is too low. Restart occurs via a complete startup sequence (latch reset and soft−start).

## APPLICATION INFORMATION

The NCP1336 has two operating modes: quasi resonant operation and VCO operation.

The operating mode is fixed by the FB voltage:

- Quasi−resonant operation occurs for FB voltage higher than 0.8 V (FB decreasing) or higher than 1.6 V (FB increasing) which correspond to high output power and medium output power.
  During quasi−resonant operation, the operating valley (1st, 2nd, 3rd or 4th) is fixed by the FB voltage which is compared internally to several voltage references corresponding to the different valleys. There is a wide hysteresis on each valley, allowing the controller to adjust the output power by the current−mode control without jumping between valleys. The peak current is variable and is set by the FB voltage divided by 4.
- VCO operation occurs for FB voltage lower than 0.8 V (FB decreasing) or lower than 1.6 V (FB increasing). This corresponds to low output power.
  During VCO operation, the peak current is fixed to 25% of its maximum value and the frequency is variable. The frequency is set by the end of charge of Ct capacitor. This capacitor is charged with a constant current source and the capacitor voltage is compared to an internal threshold fixed by FB voltage. When this capacitor voltage reaches the threshold the capacitor is rapidly discharged down to 0 V and a new period start.

### Startup

NCP1336 includes a high voltage startup circuitry that derives current from the bulk line to charge the $V_{CC}$ capacitor. When the power supply is first connected to the mains outlet, the internal current source is biased and charges up the $V_{CC}$ capacitor. When the voltage on this $V_{CC}$ capacitor reaches the $VCC_{on}$ level, the current source turns off, reducing the amount of power being dissipated. At this time, the controller is only supplied by the $V_{CC}$ capacitor, and the auxiliary supply should take over before $V_{CC}$ collapses below $VCC_{min}$. Figure 3 shows the internal arrangement of this structure:

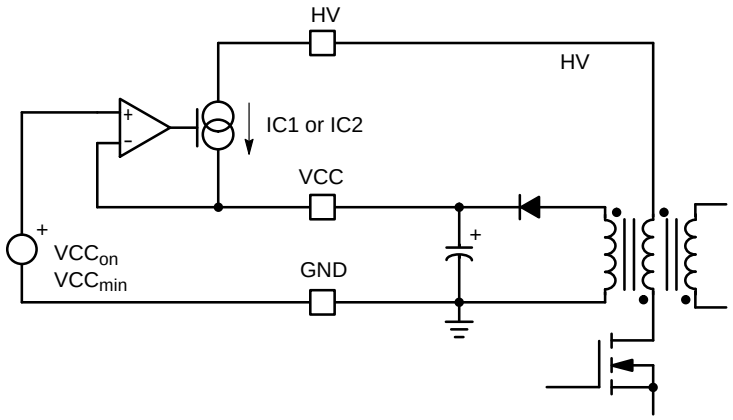



**Figure 3. Startup Circuitry: The Current Source Brings $V_{CC}$ Above 15 V and Turns Off**

In some fault situations, a short−circuit can purposely occur between $V_{CC}$ and GND. In high line conditions ($V_{HV}$ = 370 Vdc) the current delivered by the startup device will seriously increase the junction temperature. For instance, since IC2 equals 3 mA (the min corresponds to the highest $T_J$), the device would dissipate 370 V x 3 mA = 1.11 W. To avoid this situation, the controller includes a novel circuitry made of two startup levels, IC1 and IC2. At power−up, as long as $V_{CC}$ is below a certain level (0.7 V typ.), the source delivers IC1 (around 300 μA typical), then, when $V_{CC}$ reaches 0.7 V, the source smoothly transitions to IC2 and delivers its nominal value. As a result, in case of short−circuit between $V_{CC}$ and GND, the power dissipation will drop to 370 V x 300 μA = 111 mW. Figure 4 portrays this particular behavior:

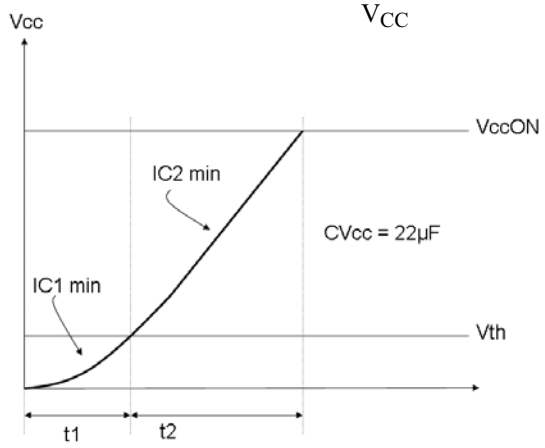



**Figure 4. The Dual Level Startup Current Source**

The first startup period is calculated by the formula, CV = It which implies a 22 μF x 0.9 V / 150 μA = 132 ms startup time for the first sequence. The second sequence is obtained by changing I to 3 mA (worst case calculation) with ΔV = 15 V − 0.9 V = 14.1 V, which finally leads to a second startup time of 22 μF x 14.1 V / 3 mA = 103 ms. The total startup time becomes 103 ms + 132 ms = 235 ms. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.

As soon as $V_{CC}$ reaches $VCC_{on}$, drive pulses are delivered on pin 9 and the auxiliary winding increases the voltage on the $V_{CC}$ pin. At the same time, the controller smoothly ramps up the peak current to $I_{max}$ (0.8 V / $R_{sense}$) which is reached after a typical 5 ms soft−start period. As soon as the CS voltage reaches 0.8 V = $I_{Limit1}$, the internal error flag IpFlag is asserted. When the error flag is asserted, the current source on pin 3 is activated and charges up the capacitor connected to this pin. If the error flag is still asserted when the timer capacitor has reached the threshold level VtimFault, then the controller assumes that the power supply has really undergone a fault condition and immediately stops all pulses to enter a safe burst operation. Figure 5 depicts the $V_{CC}$ evolution during a proper startup sequence, showing the state of the error flag:

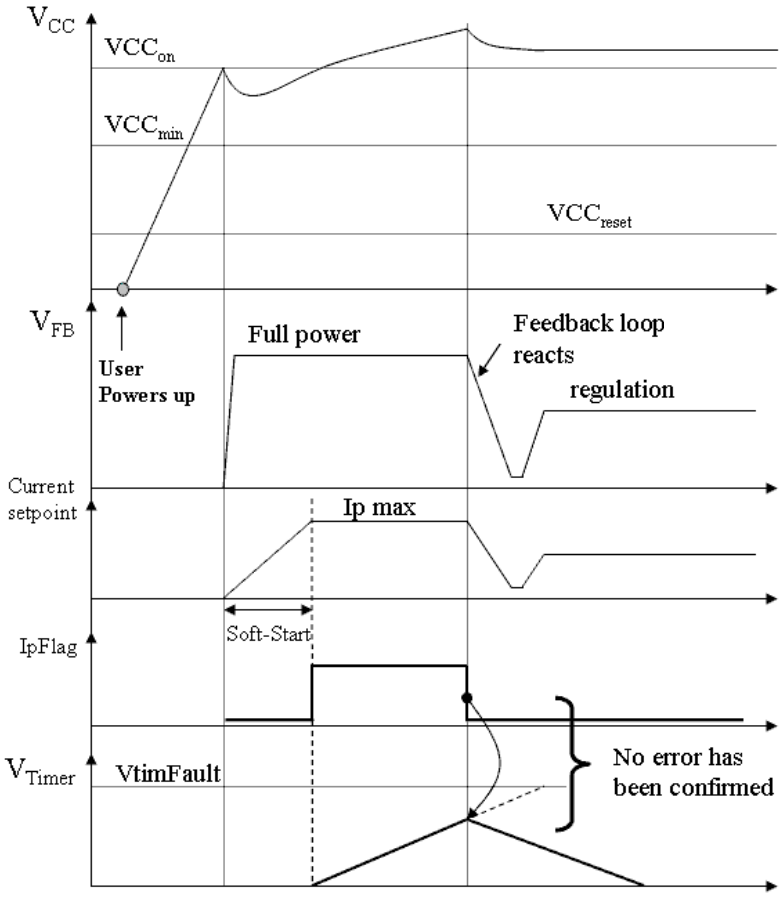



**Figure 5. An error flag gets asserted as soon as the current setpoint reaches its upper limit (0.8 V/$R_{sense}$). Here the timer lasts 50 ms, a 100 nF capacitor being connected to pin 3.**

### NCP1336 Operation

The valley detection is done by monitoring the voltage of the auxiliary winding of the transformer. The typical detection level is fixed at 55 mV. When a valley is detected, the decimal counter is incremented. The operating valley (1st, 2nd, 3rd or 4th) is determined by the FB voltage. As FB voltage decreases or increases, the valley comparators toggle one after another to select the proper valley. The activation of an “n” valley comparator disables the “n+1” or “n−1” valley comparator (depending if FB increases or decreases) and enables the corresponding “n” output of the decimal counter. Figure 6 shows the internal arrangement of the valley selection circuitry.

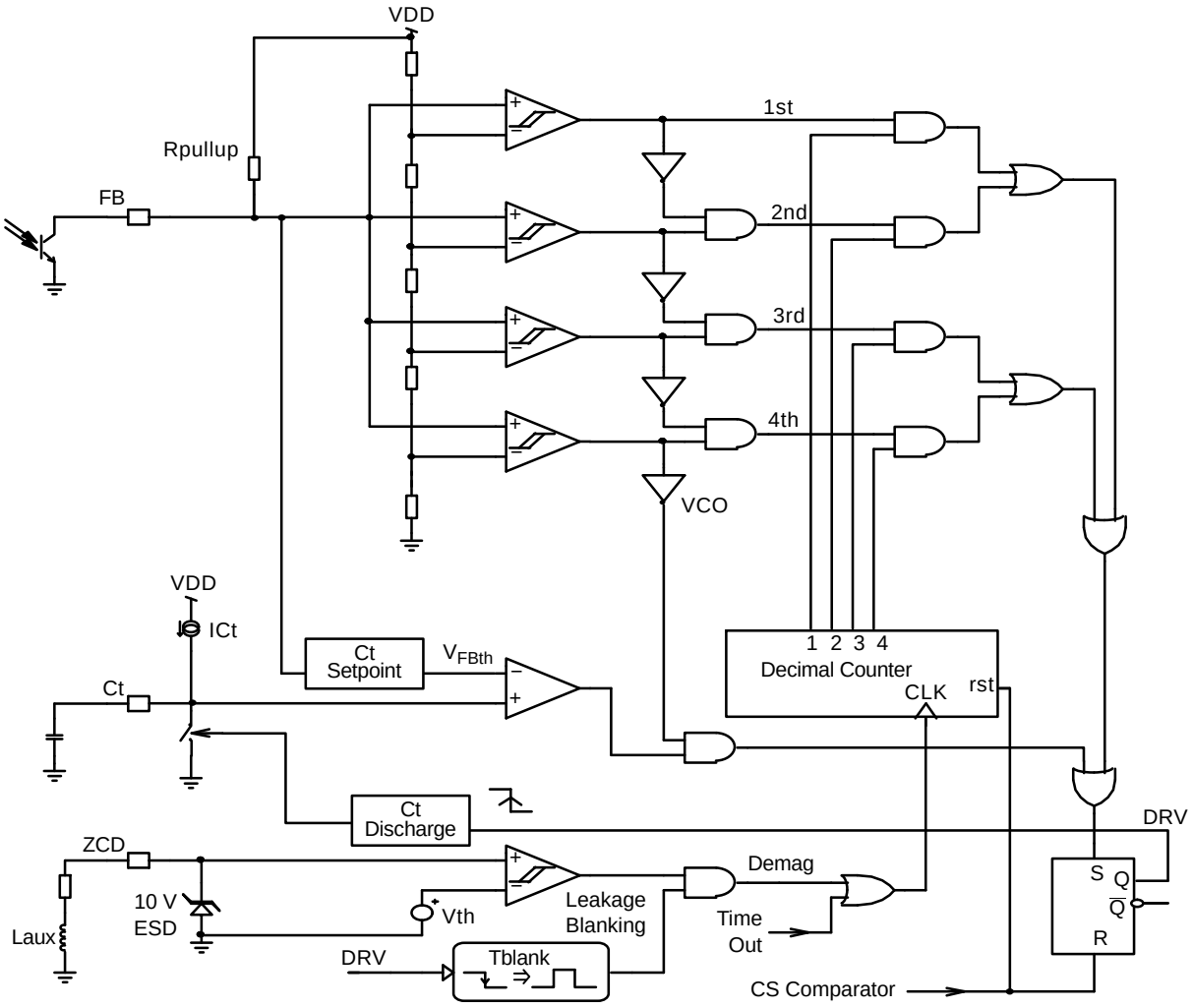



**Figure 6. Valley Selection and VCO Internal Schematic**

When an “n” valley is asserted by the valley selection circuitry, the controller is locked in this valley until the FB voltage decreases of 0.6 V (“n+1” valley activates) or increases of 0.8 V (“n−1” valley activates). The peak current adjusts to deliver the necessary output power (See Figure 7 and Figure 8). Each comparator has a hysteresis of 600 mV that helps to stabilize the valley selection in case of oscillations on FB voltage.

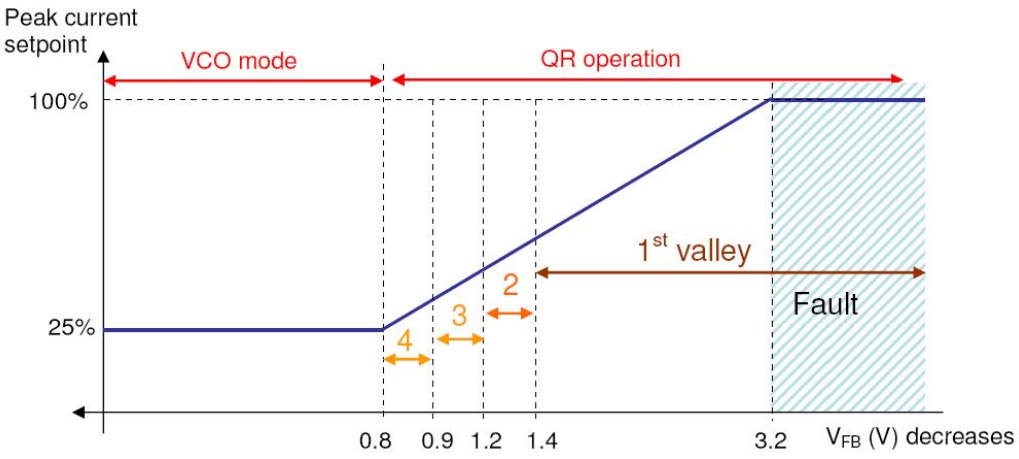



**Figure 7. Peak Current Setpoint and Selected Valley vs. FB Voltage when FB Voltage Decreases**

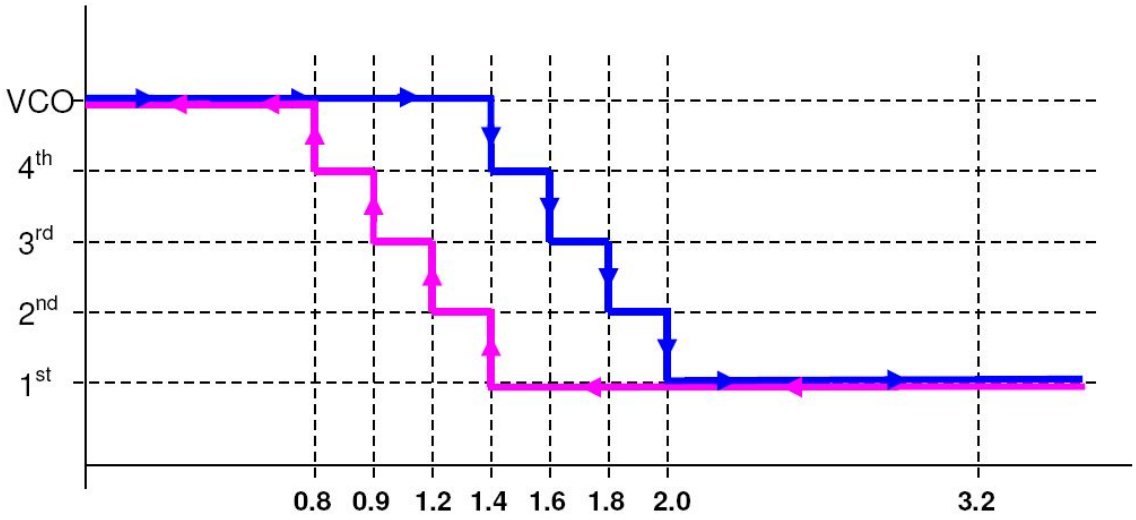



**Figure 8. Selected Valley According to FB State**

As the output load decreases (FB voltage decreases), the valleys are incremented from the first to the fourth. When the fourth valley is reached, if FB voltage further decreases below 0.8 V, the controller enters VCO mode as in NCP1351.

During VCO operation, the peak current is frozen to 25% of maximum peak current: the switching frequency expands to deliver the necessary output power. This allows achieving very low standby power consumption.

Figure 9 shows a simulation case where the output current of a 19 V / 60 W adapter decreases from 2.5 A to 0.5 A. No instability is seen during the valley transitions (Figures 10, 11, 12 and 13.)

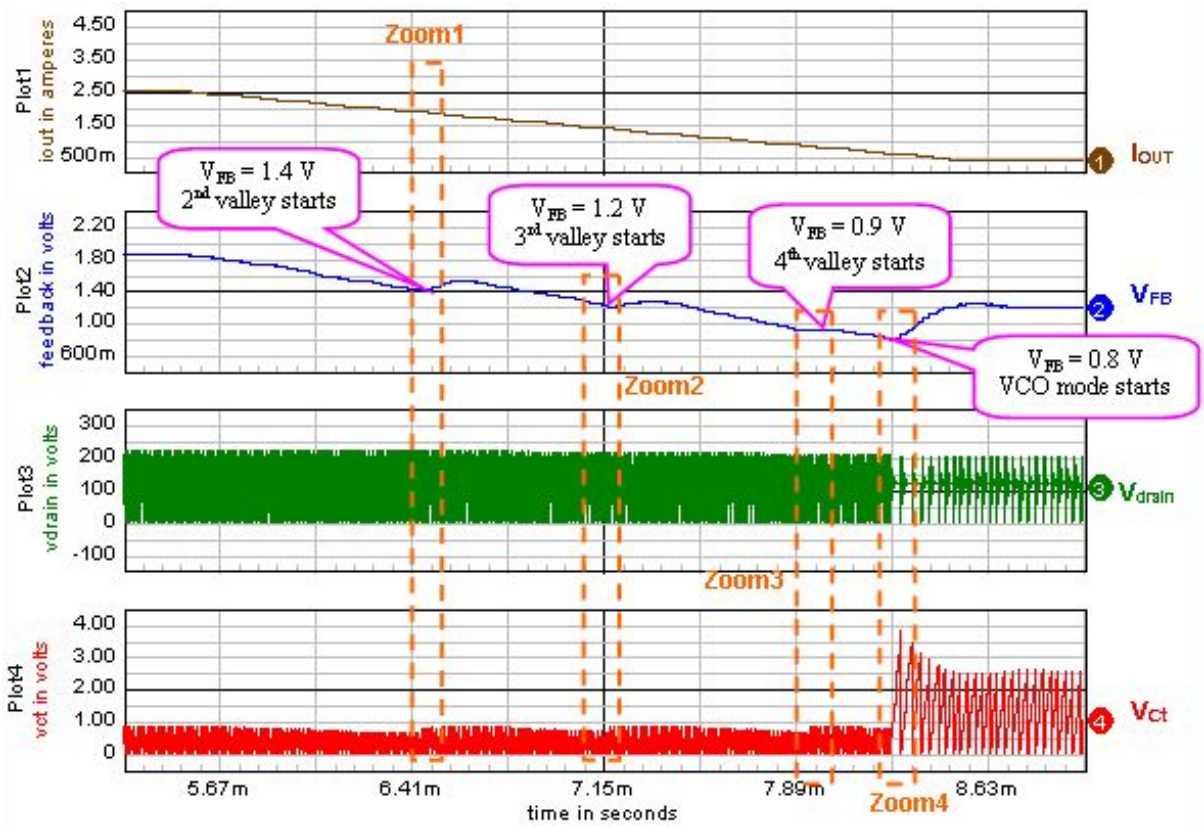



**Figure 9. Output Load Decreases from 2.5 A to 0.5 A at $V_{IN}$ = 120 Vdc for a 19 V / 60 W Adapter**

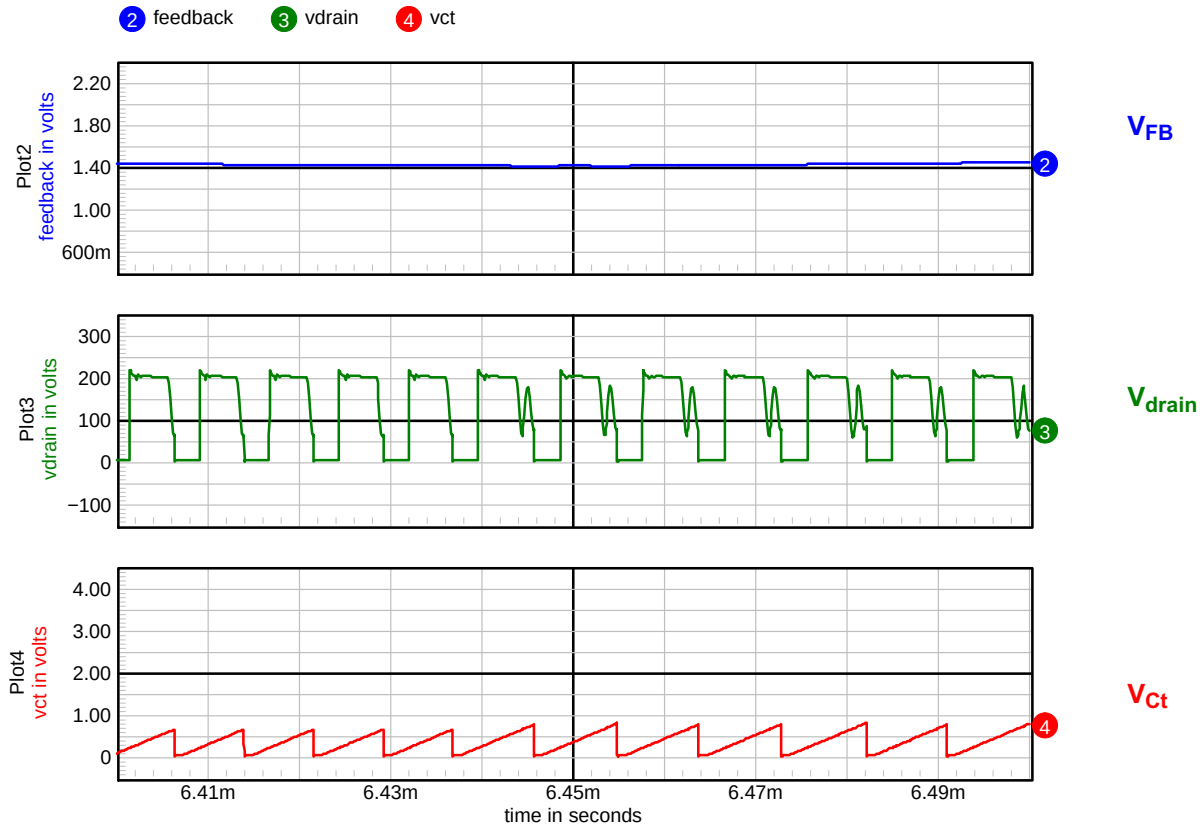



**Figure 10. Zoom 1: 1st to 2nd Valley Transition**

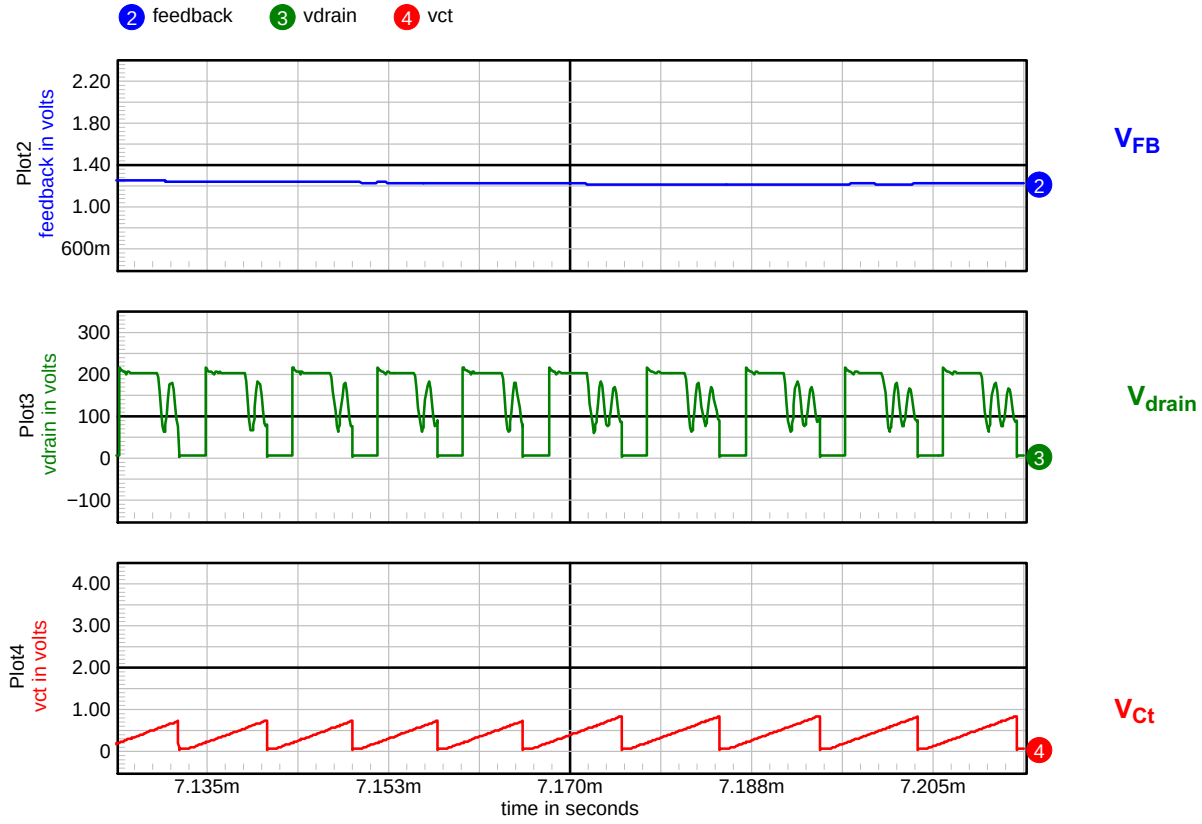



**Figure 11. Zoom 2: 2nd to 3rd Valley Transition**

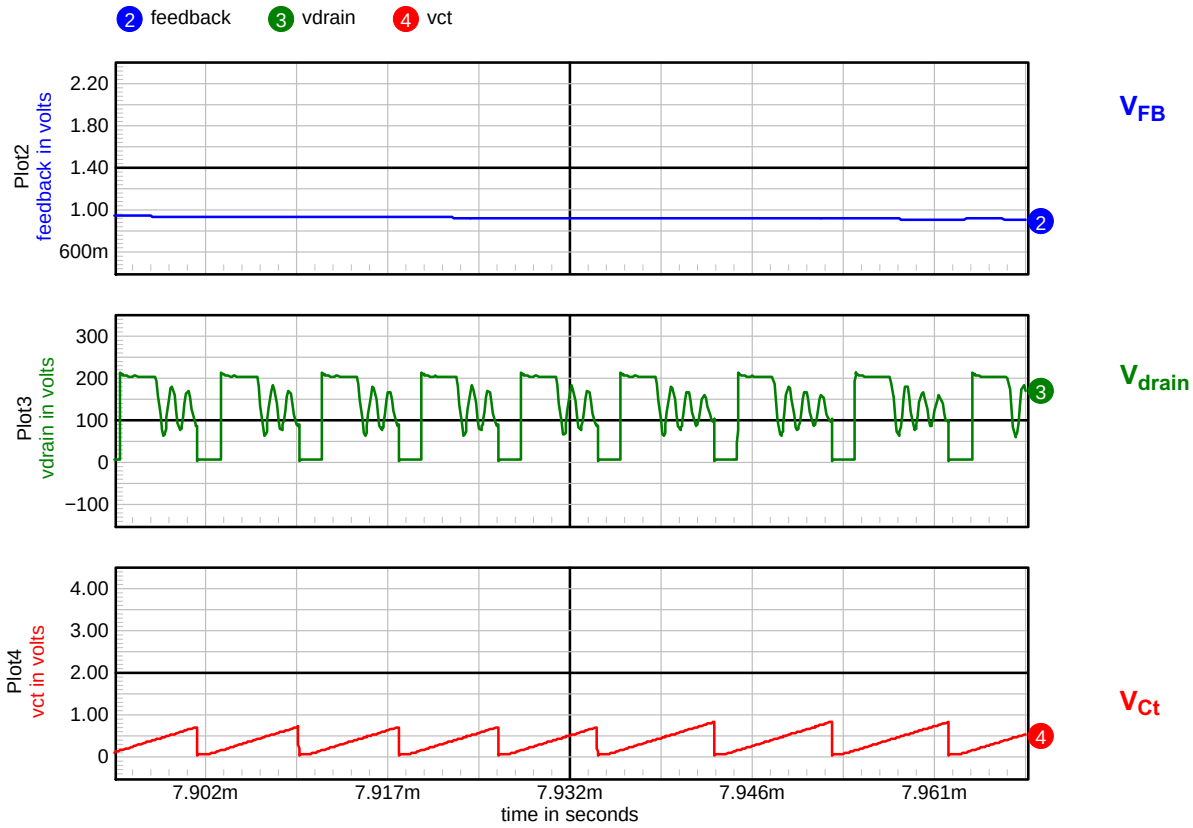



**Figure 12. Zoom 3: 3rd to 4th Valley Transition**

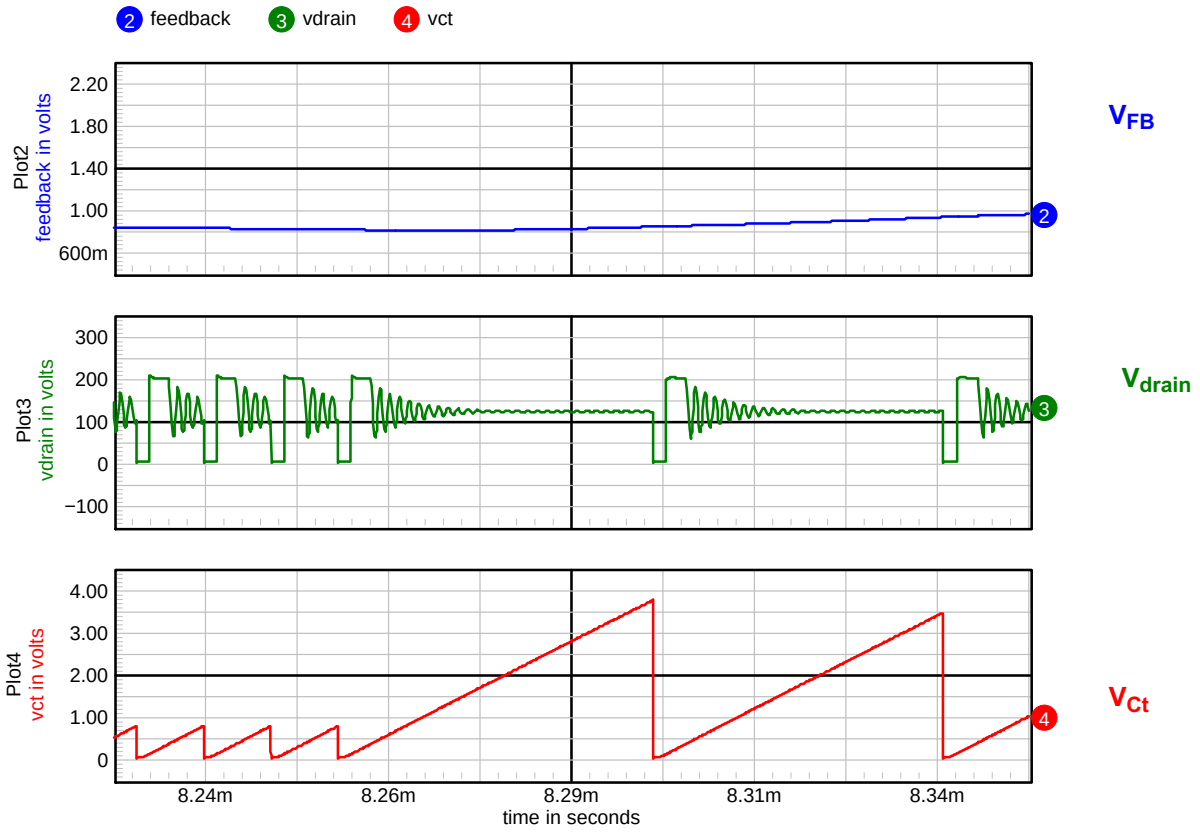



**Figure 13. Zoom 4: 4th Valley to VCO Mode Transistion**

**Time Out**

In case of extremely damped free oscillations, the ZCD comparator can be unable to detect the valleys. Consequently, the decimal counter clock is in low state and the drive pulses stops. To avoid such situation, NCP1336 integrates a Time Out function that acts as a clock for the decimal counter. The controller thus continues its normal operation. To avoid having a too big step in frequency, the time out duration is set to 5.25 μs. Figures 15 and 16 detail the time out operation.

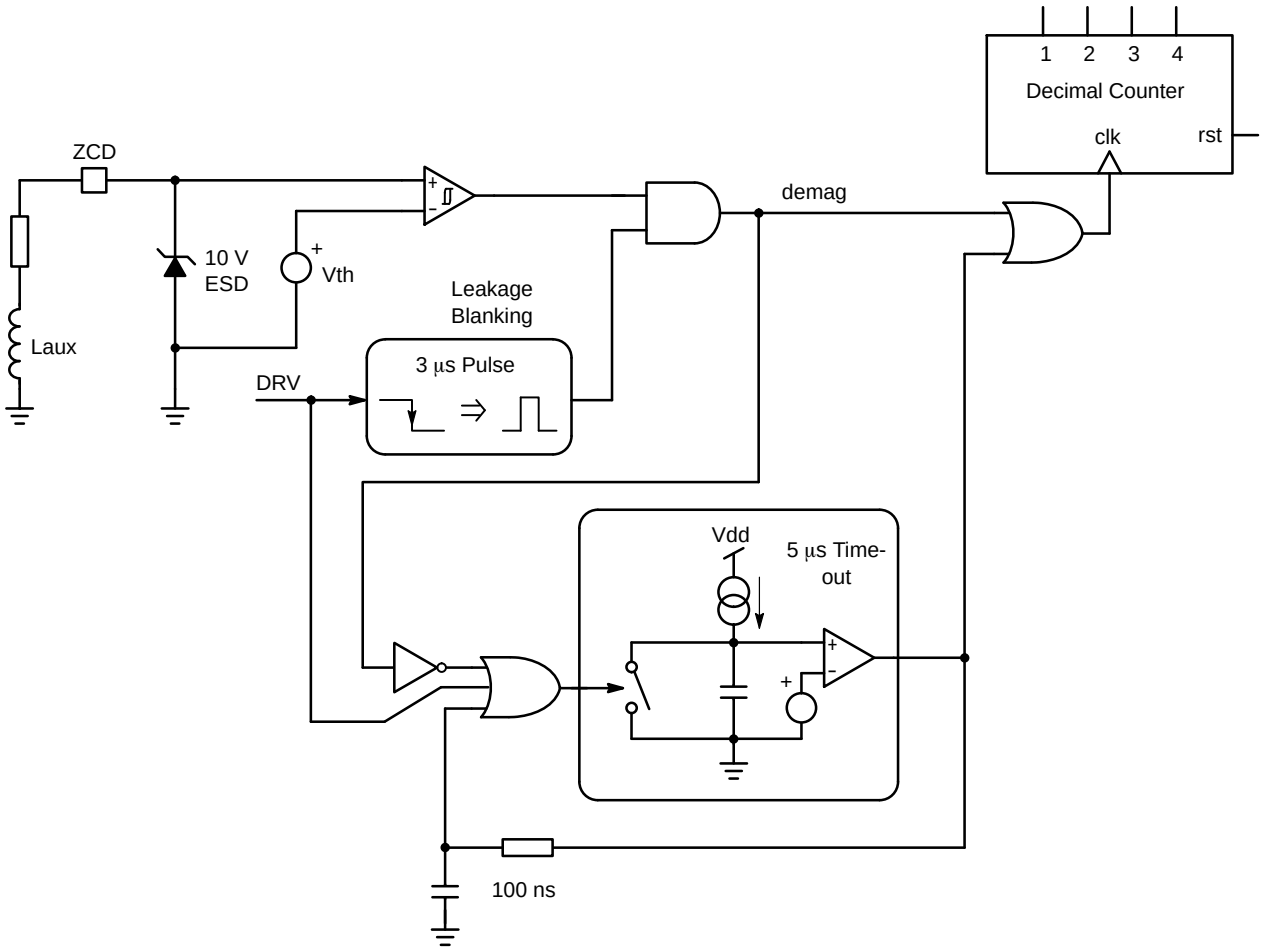



**Figure 14. Time Out Circuit**

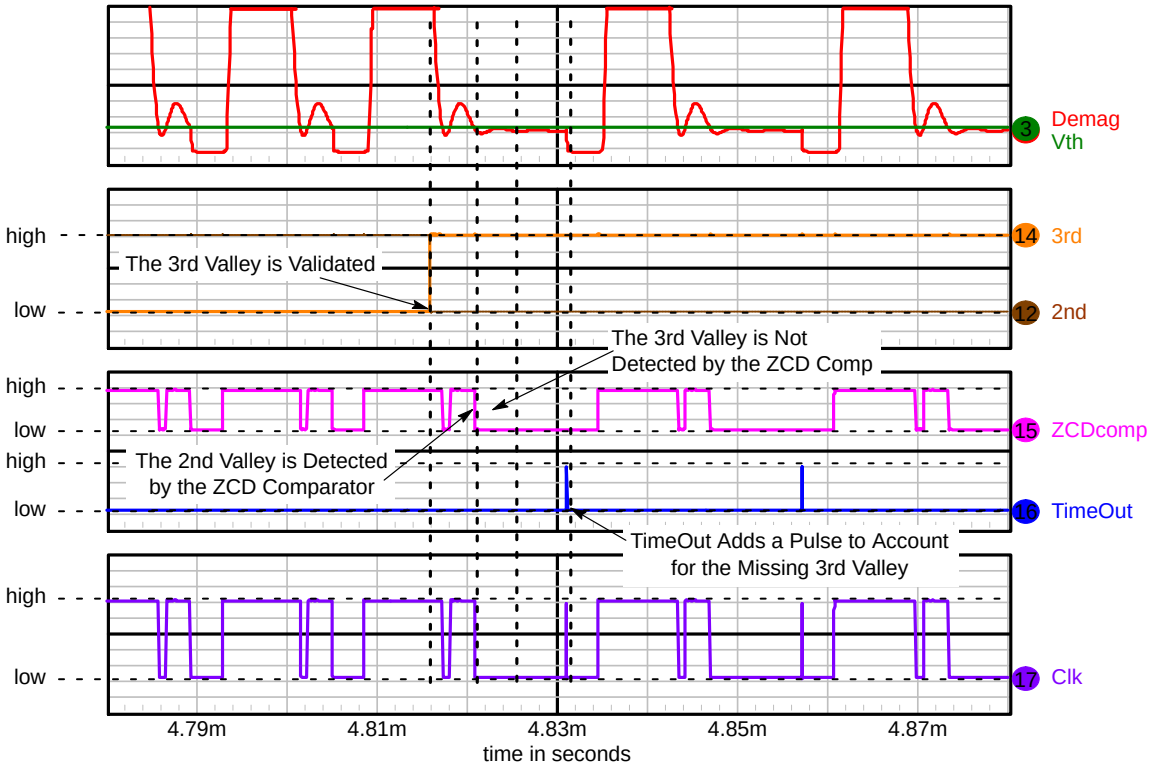



**Figure 15. Time Out Operation Chronogram**

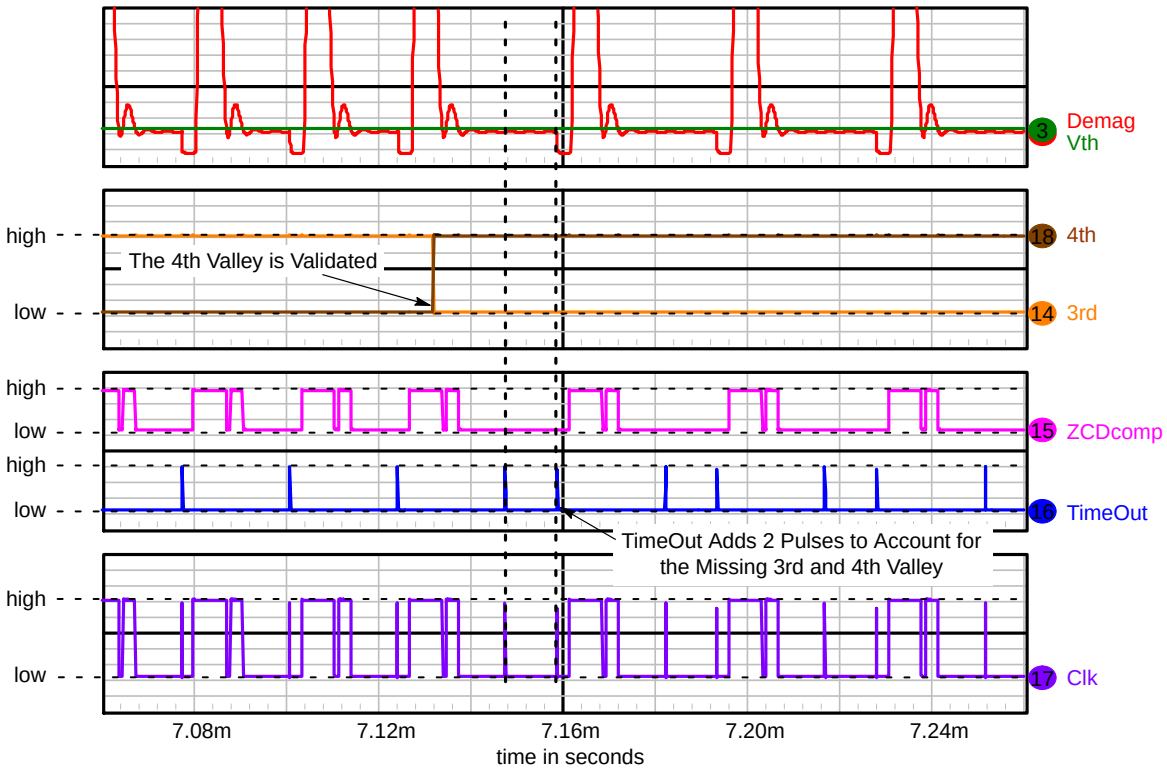



**Figure 16. Time Out Operation Chronogram continued**

### VCO Mode

VCO operation occurs for FB voltage lower than 0.8 V (FB decreasing), or lower than 1.6 V (FB increasing). This corresponds to low output power.

During VCO operation, the peak current is fixed to 25% of its maximum value and the frequency is variable and expands as the output power decreases.

The frequency is set by the end of charge of Ct capacitor. This capacitor is charged with a constant current source and the capacitor voltage is compared to an internal threshold fixed by FB voltage (see Figure 6). When this capacitor voltage reaches the threshold, the capacitor is rapidly discharged down to 0 V and a new period start. The internal threshold is inversely proportional to the FB voltage. The relationship between $V_{FBth}$ and $V_{FB}$ is: $V_{FBth} = 6.5 - (10/3)\ V_{FB}$. When $V_{FB}$ is lower than 0.3 V, Ct voltage is clamped to $VCT_{max} = 5.5$ V. Figure 17 shows the VCO mode at works**.**

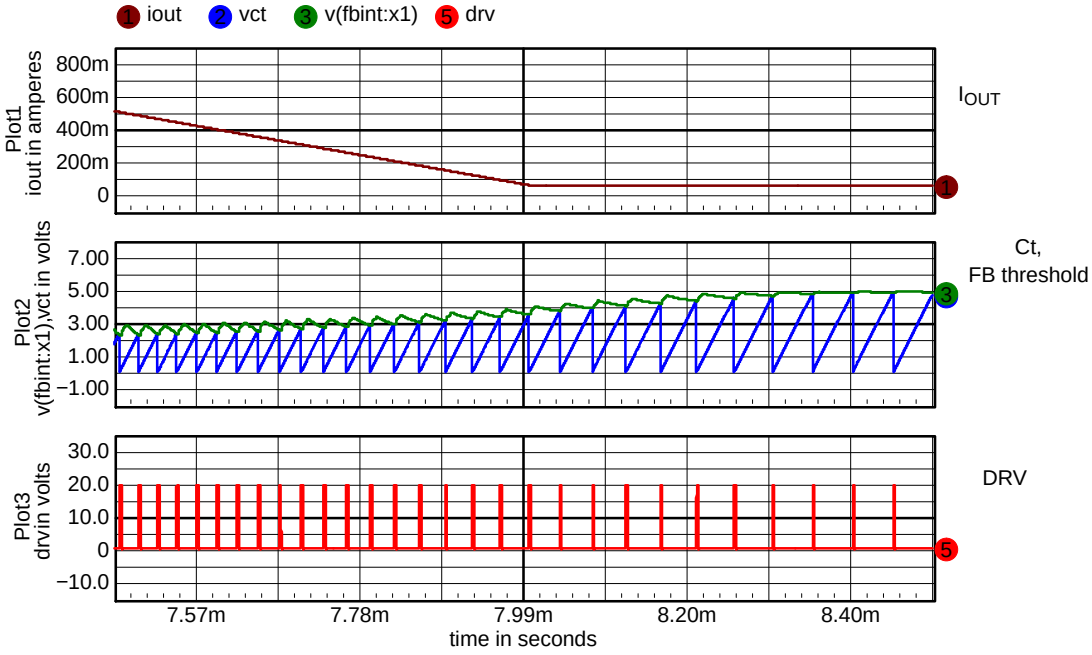



**Figure 17. In VCO Mode, as the Power Output Decreases the Frequency Expands**

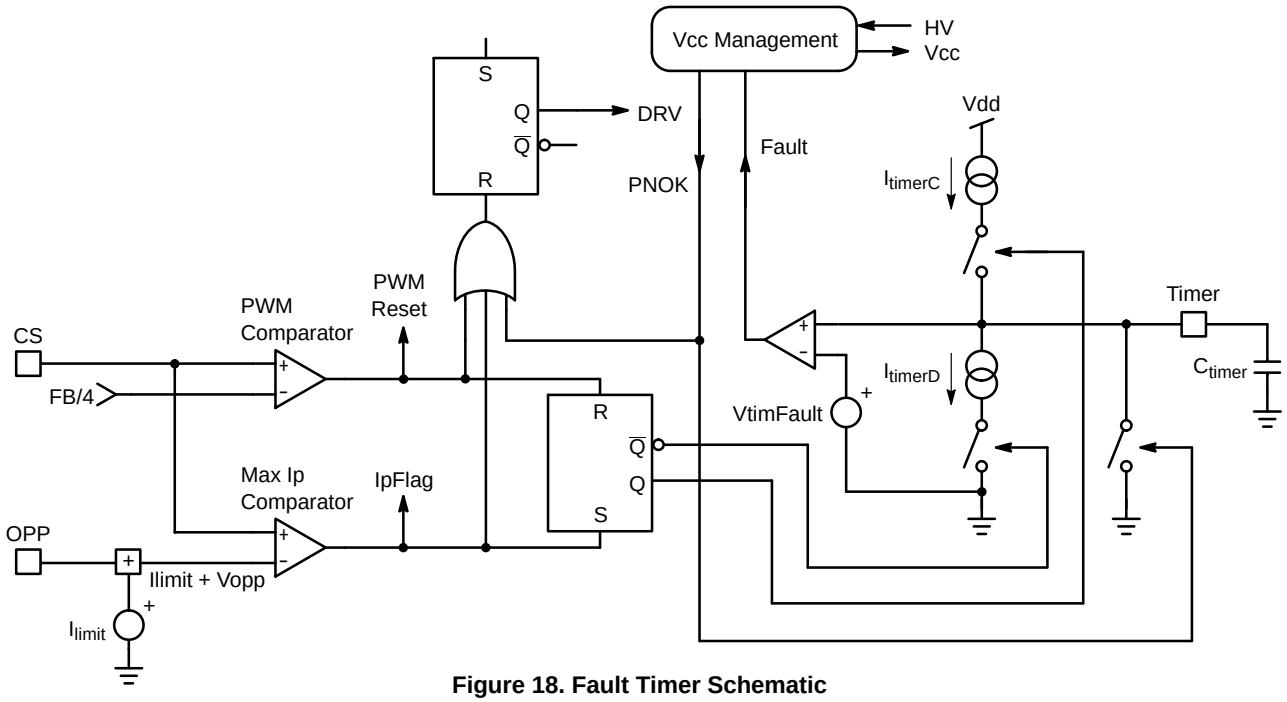



**Figure 18. Fault Timer Schematic**

### Short−circuit or Overload Mode

Figure 18 shows the implementation of the fault timer.

When the current in the MOSFET is higher than, “Max (0.8 V / $R_{sense}$) Ip” comparator trips and the timer capacitor is charged by ItimerC current source. When the current comes back within safe limits, “Max Ip” comparator becomes silent and the PWM comparator triggers the discharge of the timer capacitor.

If “IpFlag” and PWMreset occur at the same time, the PWMreset signal is the strongest and the capacitor is discharged.

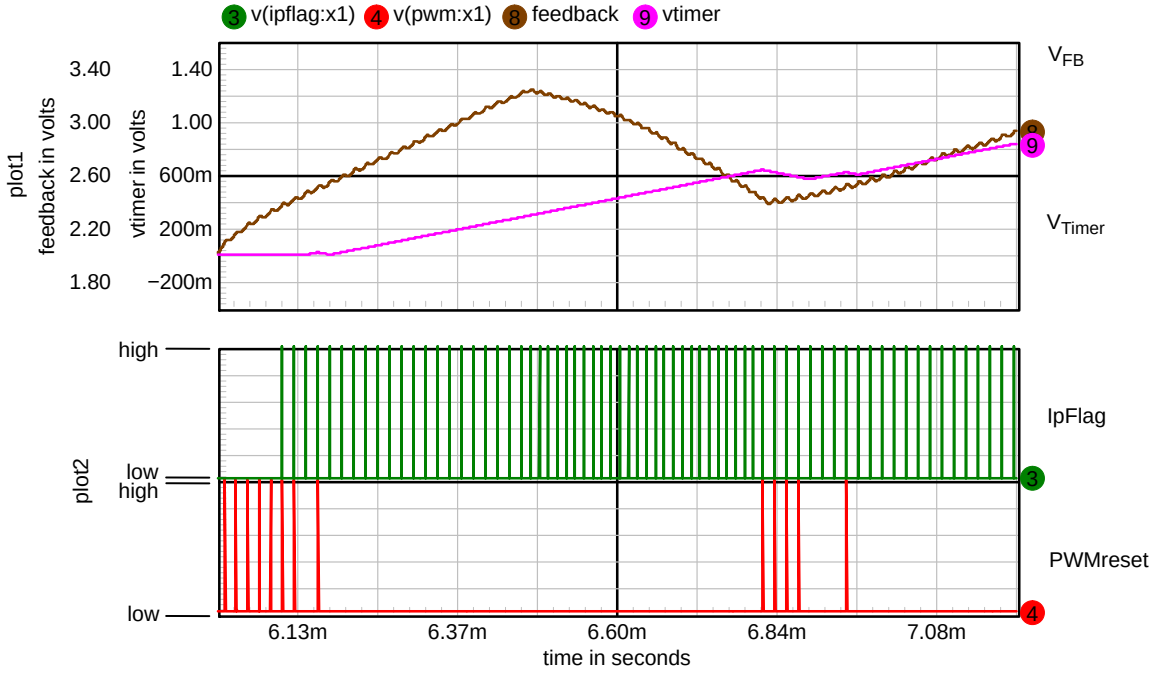



**Figure 19. Timer Operating Chronograms**

There can be various events that force a fault on the primary side controller. We can split them in different situation, each having a particular configuration:

1. The converter regulates but the auxiliary winding collapses: this is a typical situation linked to the usage of a constant−current / constant−voltage (CC−CV) type of controller. If the output current increases, the voltage feedback loop gives up and the current loop takes over. It means that $V_{OUT}$ goes low but the feedback loop is still closed because of the output current monitoring. Therefore, seen from the primary side, there is no fault. However, there are numerous charger applications where the output voltage shall not go below a certain limit, even if the current is controlled. To cope with this situation, the controller features a precise under−voltage lockout comparator biased to a $VCC_{min}$ level. When this level is crossed, whatever the other pin conditions, pulses are stopped and the controller enters the safe hiccup mode, trying to re−start. Figure 20 shows how the converter will behave in this situation. If the fault goes away, the SMPS resumes operation.
2. In the second case, the converter operates in regulation, but the output is severely overloaded. However, due to the bad coupling between the power and the auxiliary windings, the controller $V_{CC}$ does not go low. The peak current is pushed to the maximum, the error flag IpFlag is consequently asserted and the timer starts to count. Upon completion, all pulses are stopped and triple−startup hiccup mode is entered for version B. If the fault goes away, the SMPS resumes operation (Figure 21). For version A, when the timer finishes counting, the pulses stop and the circuit stays latched until the user cycles down the power supply (Figure 22).
3. Another case exists where the short−circuit makes the auxiliary level go below $VCC_{min}$. In that case, the timer length is truncated and all pulses are stopped. The triple hiccup fault mode is entered and the SMPS tries to re−start. When the fault is removed, the SMPS resumes operation.

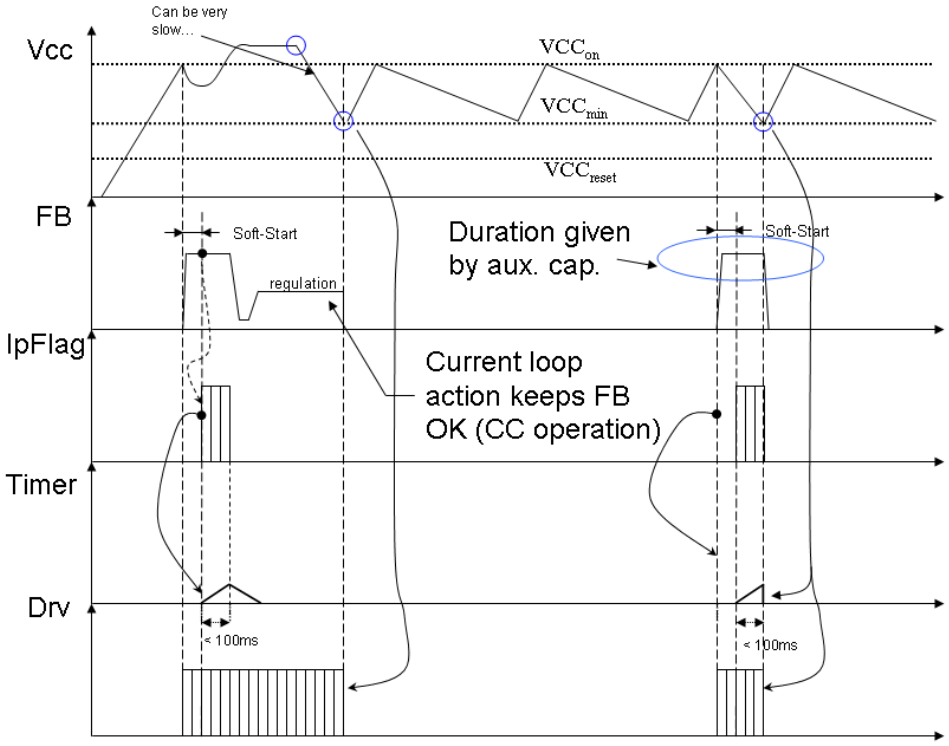



**Figure 20. First Fault Mode Case, the Auxiliary Winding Collapses but Feedback is Still There**

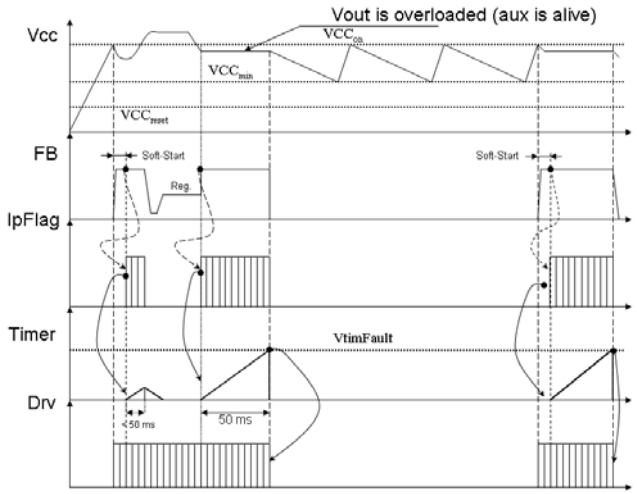



**Figure 21. Short−Circuit Case Where Vaux Does NOT Collapse on Version B**

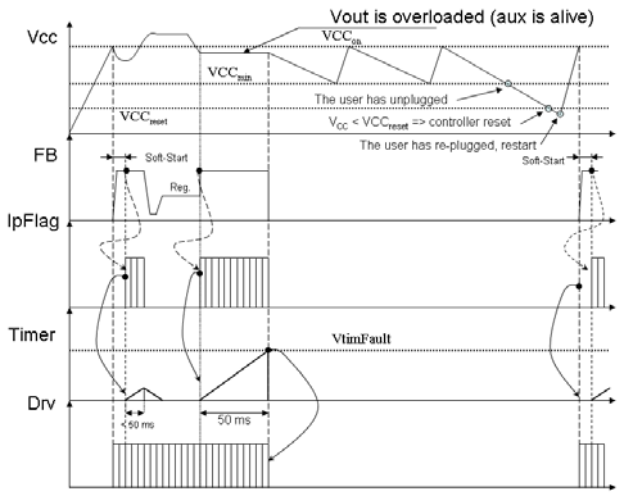



**Figure 22. Short−Circuit Case Where Vaux Does NOT Collapse on Version A**

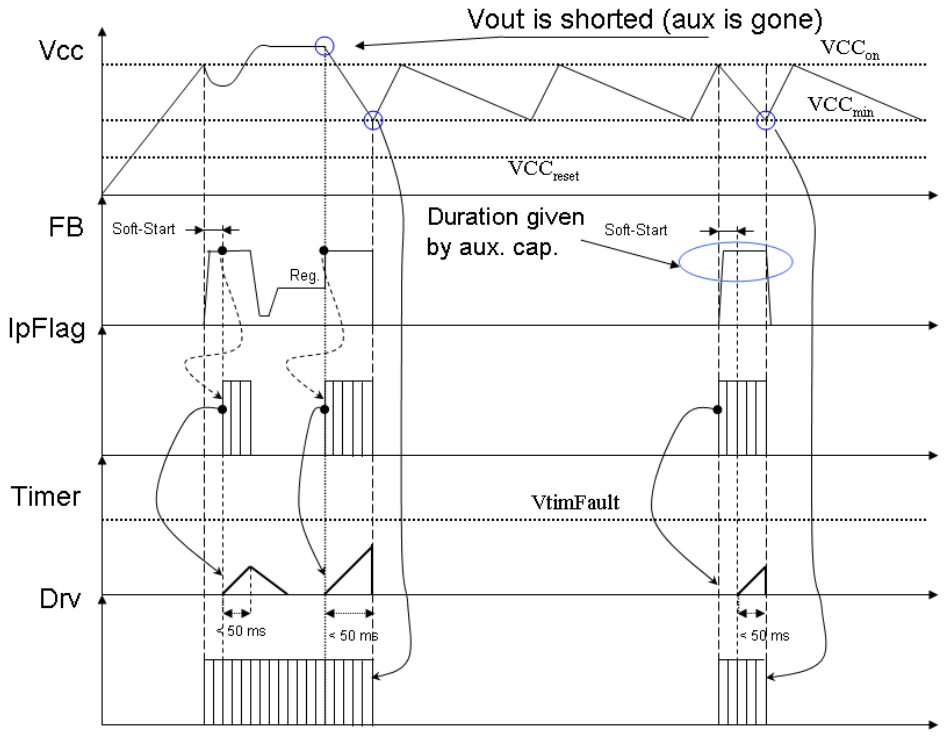



**Figure 23. This Case is Similar to a Short−Circuit Where $V_{aux}$ Does Collapse**

The recurrence in hiccup mode can easily be adjusted by either reducing the timer or increasing the $V_{CC}$ capacitor. Figure 24 details the various time portion a hiccup is made of:

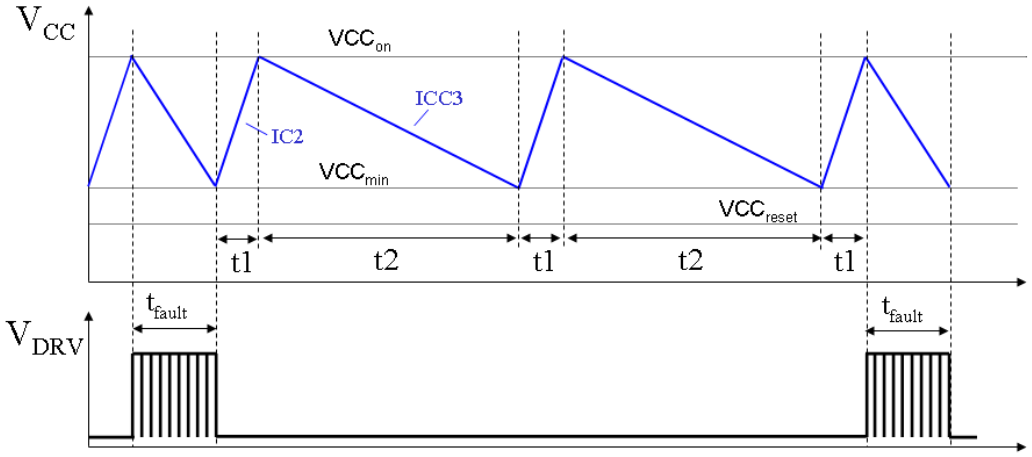



**Figure 24. The Burst Period is Ensured by the $V_{CC}$ Capacitor Charge / Discharge Cycle**

If by design we have selected a 22 μF $V_{CC}$ capacitor, it becomes easy to evaluate the burst period and its duty−cycle. This can be done by properly identifying all time events on Figure 8 and applying the classical formula:

$$t = \frac{C\Delta V}{I}$$

- $t_1$: I = 3 mA, ΔV= 15 V − 9 V = 6 V → $t_1$ = 44 ms
- $t_2$: I = ICC3 = 600 μA, ΔV= 15 V − 9 V = 6 V → $t_2$ = 220 ms

The total period duration is thus the sum of all these events which leads to $t_{hiccup}$ = 572 ms. If $t_{fault}$ = 50 ms, then our burst duty−cycle equals 50 ms / (572 ms + 50 ms) ≈ 8%, which is good. Should the user like to further decrease or, to the contrary, increase this duty−cycle, changing the $V_{CC}$ capacitor is an easy job.

### Over Voltage / Over Temperature Protection

The OTP and OVP pins feature circuitries to protect the circuit against high temperature and high voltage (see Figure 25).

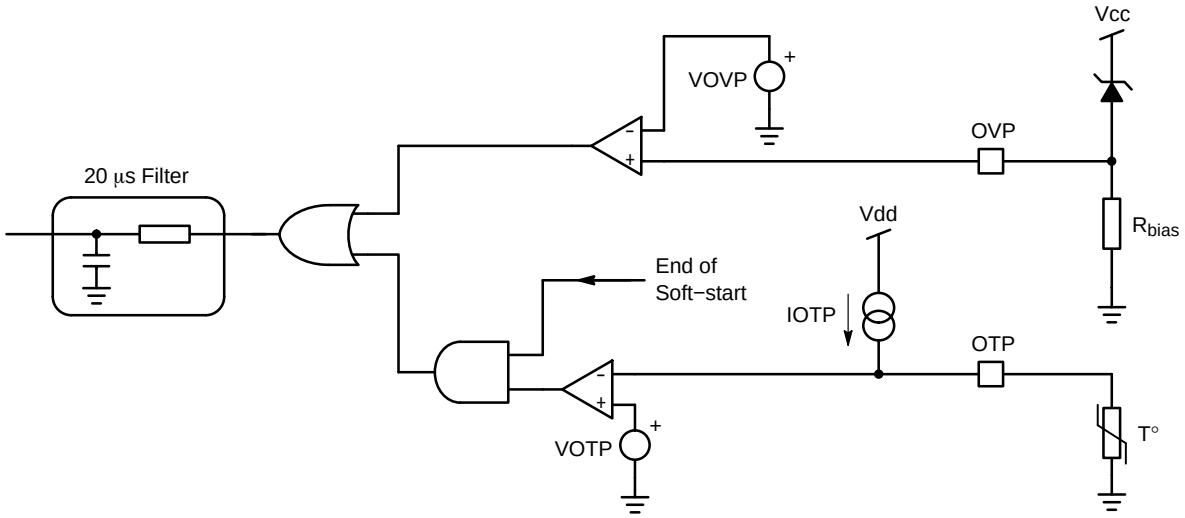



**Figure 25. Pin Latch Circuitry**

### OTP

A current flows out of the OTP pin into the NTC resistor, thus imposing a voltage on the OTP pin. When the temperature increases, the NTC's resistance reduces (For example, at 110°C, $R_{NTC}$ = 8.8 k instead of 470 k at 25°C) and the voltage on the OTP pin decreases until it reaches $V_{OTP}$: the comparator trips and latches−off the controller. To reset the controller, the user must unplug and re−plug the power supply.

During start−up and soft−start, the output of the OTP comparator is masked to allow for the voltage on the OTP pin to grow if a capacitor is installed across the NTC for filtering purposes.

### OVP

When $V_{CC}$ increases (OVP), a current starts to flow in the zener (which much be biased externally), and the voltage on the OVP pin starts to increase. When this voltage reaches $V_{OVP}$, the circuit immediately stops pulsing and stays latched until the user cycles down the power supply. The reset occurs if $V_{CC}$ drops below 5 V (or brownout is detected).

Figures 26 and 27 details the operating diagrams in case of an over temperature and an overvoltage event.

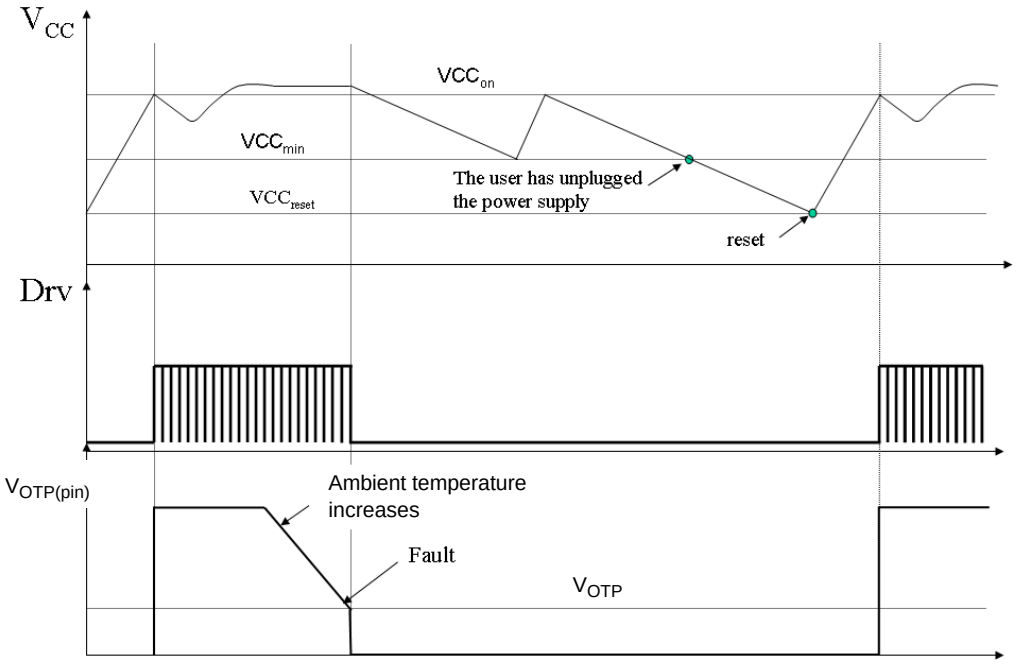



**Figure 26. Operating Diagrams in Case of an Over Temperature**

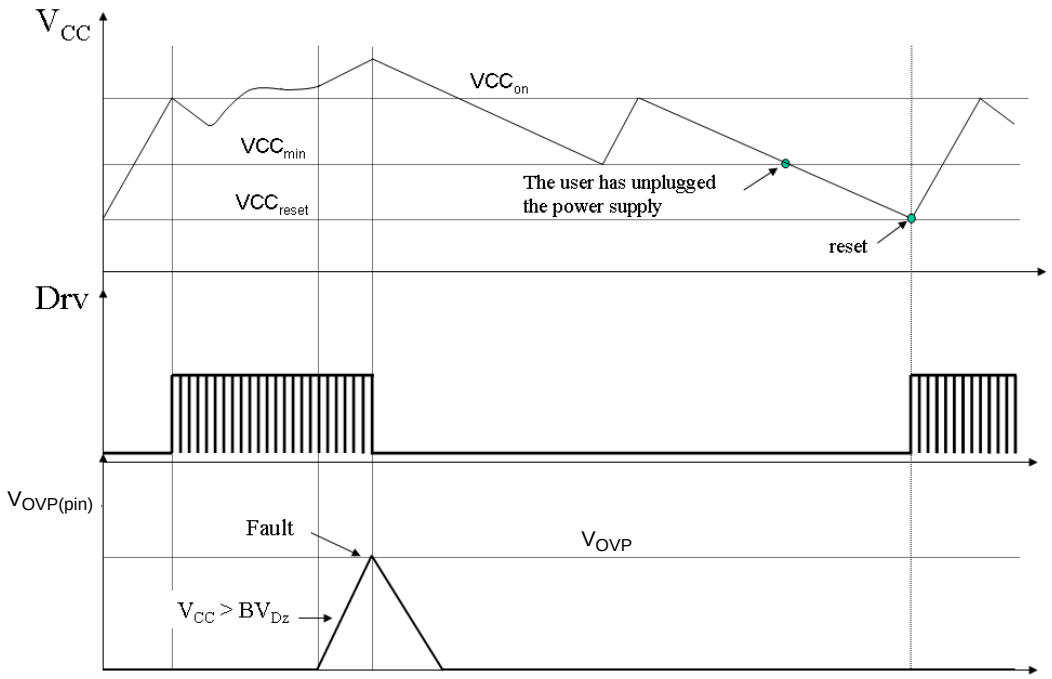



**Figure 27. Operating Diagrams in Case of an Over Voltage**

### Over Power Protection

The implementation of over power compensation in NCP1336 is described by Figure 28. A negative voltage applied on the OPP pin directly affects the precise maximum peak current reference.

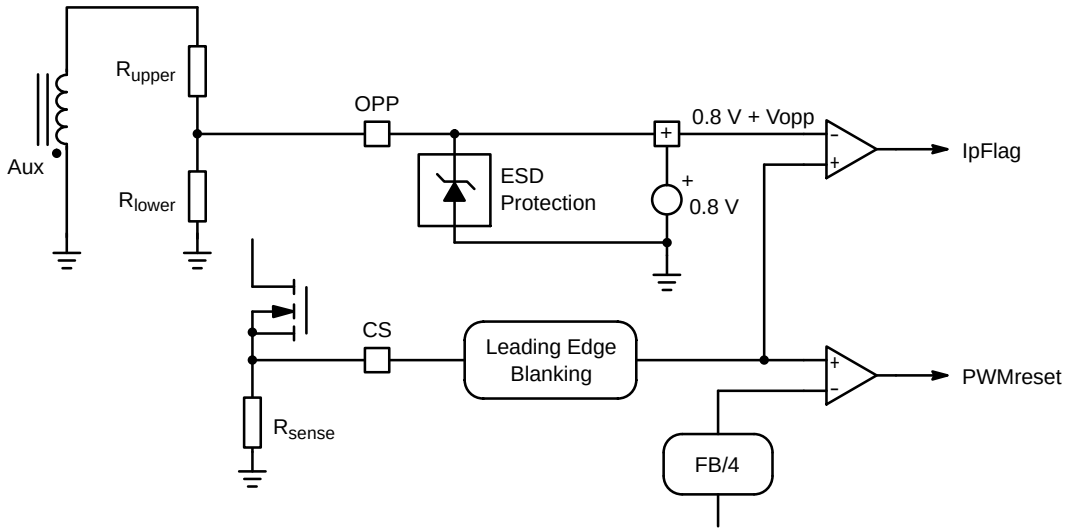



**Figure 28. The Internal OPP Circuitry Implemented on NCP1336**

By connecting the OPP pin through a resistor divider to an auxiliary winding with flyback polarity, where a negative voltage proportional to the input voltage appears during the on−time, the maximum peak current setpoint is simply decreased according to $V_{IN}$, following Figure 29.

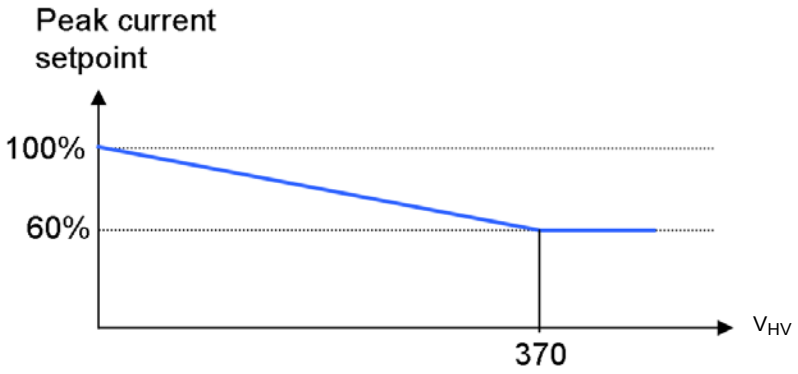



**Figure 29. Peak Current Setpoint Variation vs. OPP Pin Voltage**

By adding a zener diode in series with the resistor divider, the user has the choice to adjust the level at which the OPP is applied to the power chip.

### Design Example

Let us assume we need a current setpoint reduction of 25% at 370 Vdc, which corresponds to a sense voltage of 600 mV. We thus need to apply 600 mV − 800 mV = −200 mV on OPP pin to perform the expected compensation.

Knowing that the voltage that appears on the auxiliary winding during the on−time is $-N_{p,aux}\ V_{IN}$, with $N_{p,aux}$ the auxiliary to primary turn ratio of the transformer ($N_{p,aux} = N_{aux}/N_p$), we can simply calculate the ratio of the resistor divider:

$$\frac{R_{upper}}{R_{lower}} = -\frac{N_{p,aux}V_{IN} - V_{OPP}}{V_{OPP}}$$

Assuming the turn ratio of the transformer is $N_{p,aux} = 0.25$, we obtain:

$$\frac{R_{upper}}{R_{lower}} = -\frac{0.25 \times 370 - (-0.2)}{-0.2} = 461.5$$

With $R_{upper}$ = 470 kΩ and $R_{lower}$ = 1 kΩ for instance, the OPP function is performed with negligible power wasted in the resistor divider.

### Brownout

The NCP1336 features a brownout pin to protect the power supply against low input voltage condition. This pin permanently monitors a fraction of the bulk voltage through a voltage divider. When this image of bulk voltage is below the VBO threshold, the controller stops switching. When the bulk voltage comes back within safe limits, the circuit goes through a new startup sequence including soft−start and restarts switching (Figure 30). The hysteresis on brownout pin is implemented with a low side current source sinking 10 μA when the brownout comparator is low ($V_{bulk} < V_{bulkON}$).

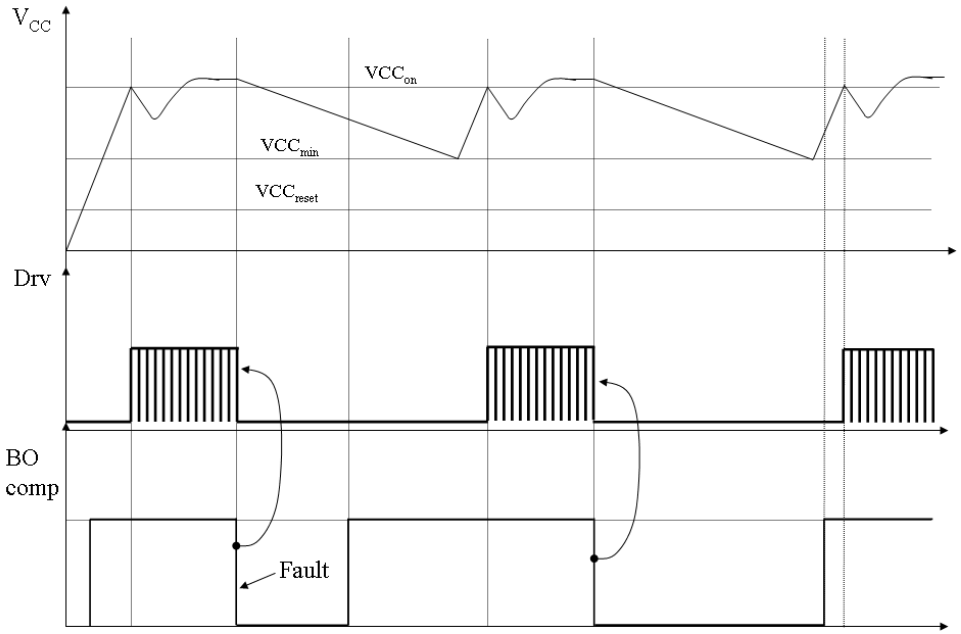



**Figure 30. Brownout Operating Chronograms**

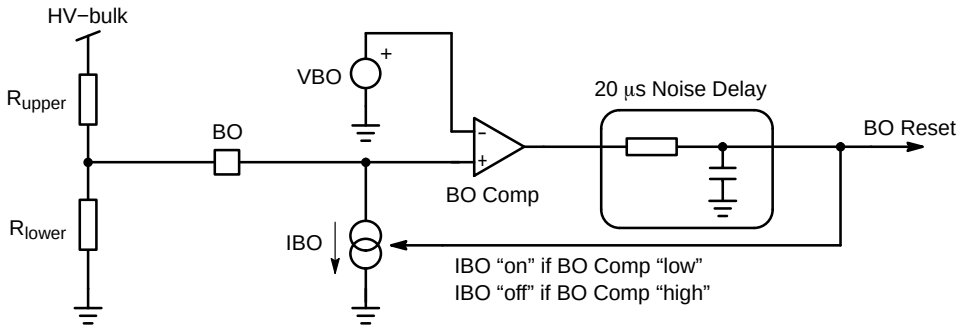



**Figure 31. Brownout Circuitry**

The following equations show how to calculate the resistors for BO pin.

First of all, select the bulk voltage value at which the controller must start switching ($V_{bulkON}$) and the bulk voltage for shutdown ($V_{bulkOFF}$). Then use the following equation to calculate $R_{upper}$ and $R_{lower}$.

$$R_{lower} = \frac{VBO(V_{bulkON} - V_{bulkOFF})}{I_{BO}(V_{bulkOFF} - VBO)}$$

$$R_{upper} = \frac{R_{lower}(V_{bulkOFF} - V_{BO})}{VBO}$$

**Design Example**

$V_{BO}$ = 0.8 V

$I_{BO}$ = 10 μA

We select: $V_{bulkON}$ = 120 V, $V_{bulkOFF}$ = 60 V

$$R_{lower} = \frac{VBO \cdot (V_{bulkON} - V_{bulkOFF})}{I_{BO} \cdot (V_{bulkOFF} - VBO)} = \frac{0.8\ V \cdot (120\ V - 60\ V)}{10\ \mu A \cdot (60\ V - 0.8\ V)} = 81.1\ k\Omega$$

$$R_{upper} = \frac{R_{lower} \cdot (V_{bulkOFF} - V_{BO})}{V_{BO}} = \frac{81.1\ k\Omega \cdot (60\ V - 0.8\ V)}{0.8\ V} = 6\ M\Omega$$

**ORDERING INFORMATION**

| Device | Package Type | Shipping† |
|---|---|---|
| NCP1336ADR2G | SO−14 Less Pin 13 (Pb−Free) | 2500 / Tape & Reel |
| NCP1336BDR2G | SO−14 Less Pin 13 (Pb−Free) | 2500 / Tape & Reel |

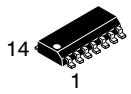
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

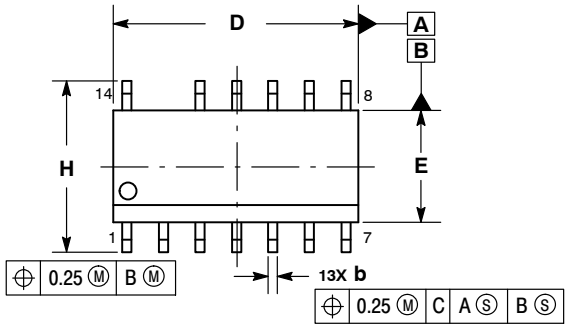
ON Semiconductor®

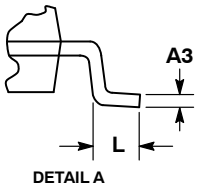
**SOIC−14 NB, LESS PIN 13**
CASE 751AN−01
ISSUE A

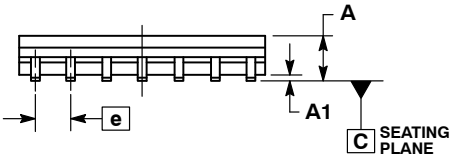
DATE 28 JAN 2008

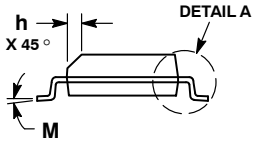



**SCALE 1:1**



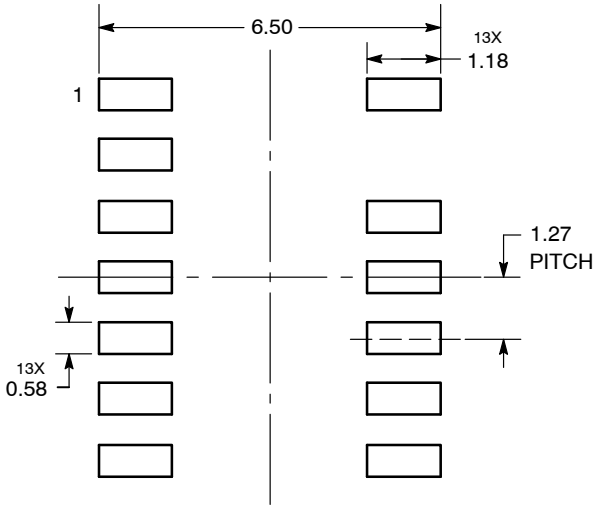




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| A3 | 0.19 | 0.25 |
| b | 0.35 | 0.49 |
| D | 8.55 | 8.75 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.25 |
| M | 0 ° | 7 ° |

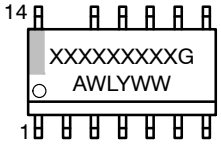
### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | |
|---|---|---|
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