BUV21

SWITCHMODE™ Series NPN Silicon Power Transistor

This device is designed for high speed, high current, high power applications.

Features

- High DC Current Gain:
  h_{FE} min = 20 at I_C = 12 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$
  max = 0.6 V at I_C = 8 A
- Very Fast Switching Times:
  TF max = 0.4 μs at I_C = 25 A
- These are Pb−Free Devices*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(SUS)}$	200	Vdc
Collector−Base Voltage	V_{CBO}	250	Vdc
Emitter−Base Voltage	V_{EBO}	7	Vdc
Collector−Emitter Voltage (V_{BE} = −1.5 V)	V_{CEX}	250	Vdc
Collector−Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	240	Vdc
Collector−Current − Continuous − Peak (PW ≤ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base−Current Continuous	I_B	8	Adc
Total Device Dissipation @ T_C = 25°C	P_D	250	W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	0.7	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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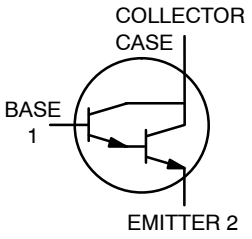
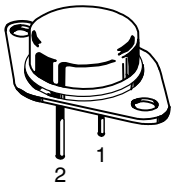
40 AMPERES NPN SILICON POWER METAL TRANSISTOR 200 VOLTS − 250 WATTS

NPN





TO−204AE (TO−3)
CASE 197A
STYLE 1

MARKING DIAGRAM

BUV21	= Device Code
G	= Pb−Free Package
A	= Assembly Location
Y	= Year
WW	= Work Week
MEX	= Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
BUV21G	TO−204 (Pb−Free)	100 Units / Tray

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (Note 1)				
Collector−Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: (V_{CE} = 250 V, V_{BE} = −1.5 V)(T_C = 25°C unless otherwise noted) (V_{CE} = 250 V, V_{BE} = −1.5 V, T_C = 125°C)	I_{CEX}		 3.0 12.0	mAdc
Collector−Emitter Cutoff Current (V_{CE} = 160 V)	I_{CEO}		3.0	mAdc
Emitter−Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter−Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	 12 0.15		Adc
ON CHARACTERISTICS (Note 1)				
DC Current Gain (I_C = 12 A, V_{CE} = 2 V) (I_C = 25 A, V_{CE} = 4 V)	h_{FE}	 20 10	 60	
Collector−Emitter Saturation Voltage (I_C = 12 A, I_B = 1.2 A) (I_C = 25 A, I_B = 3 A)	$V_{CE(sat)}$		 0.6 1.5	Vdc
Base−Emitter Saturation Voltage (I_C = 25 A, I_B = 3 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)				
Turn-on Time	(I_C = 25 A, I_{B1} = I_{B2} = 3 A, V_{CC} = 100 V, R_C = 4 Ω)	t_{on}	1.0	μs
Storage Time		t_s	1.8	
Fall Time		t_f	0.4	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

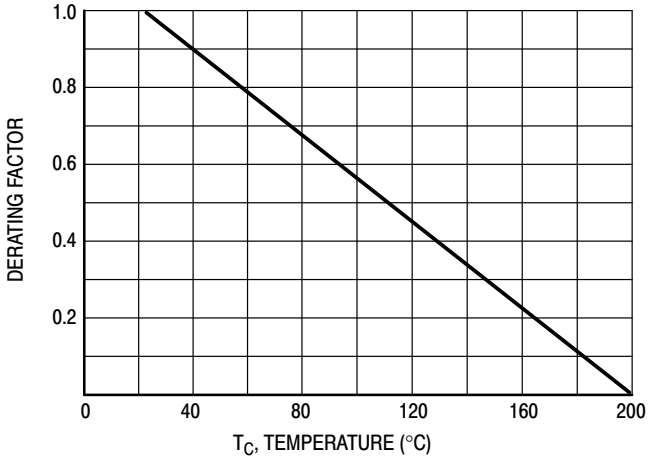


Figure 1. Power Derating

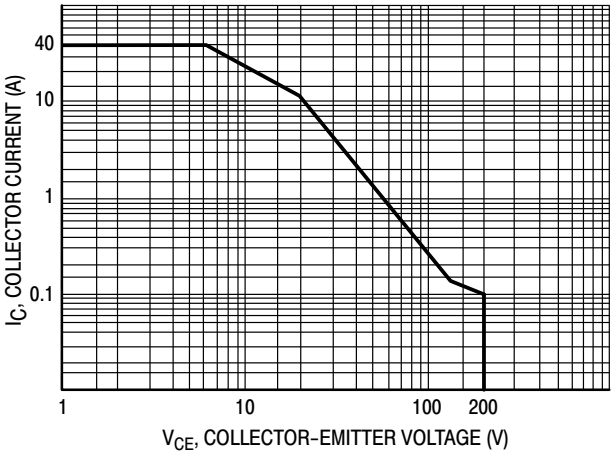


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25°C$, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

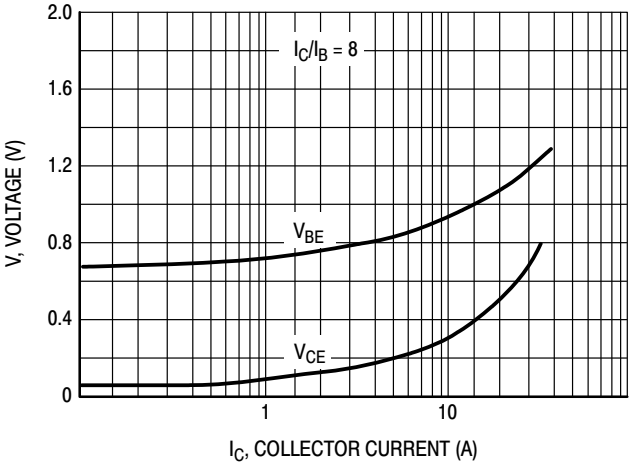


Figure 3. “On” Voltages

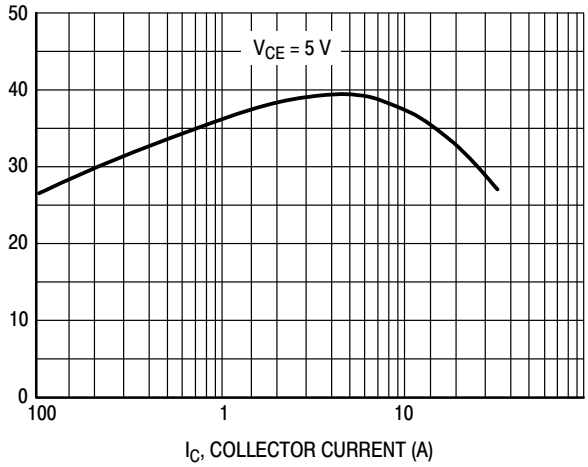


Figure 4. DC Current Gain

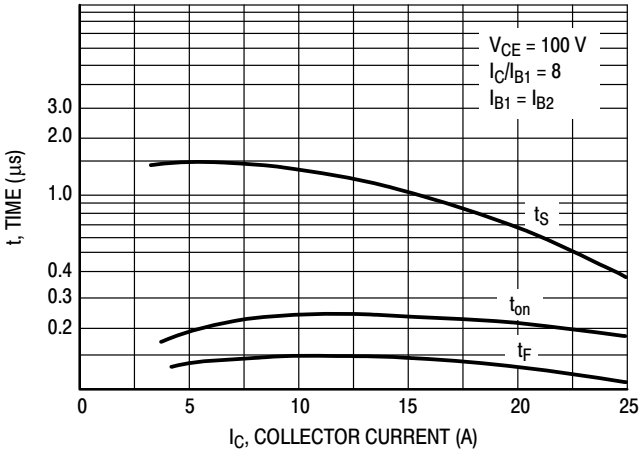
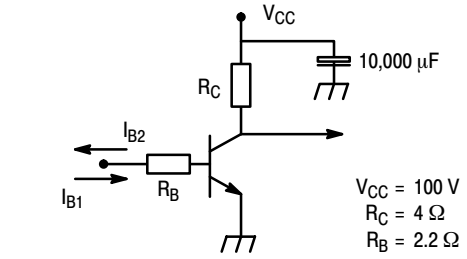


Figure 5. Resistive Switching Performance



$R_C - R_B$: Non inductive resistances

Figure 6. Switching Times Test Circuit

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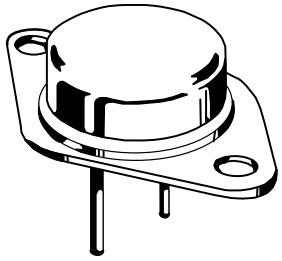
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

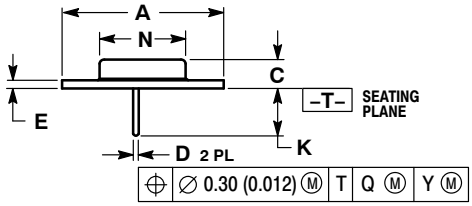
ON Semiconductor®

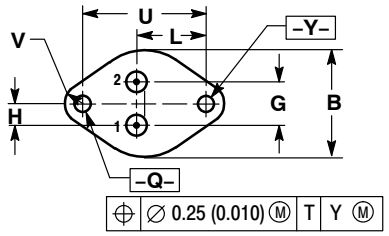


SCALE 1:1

TO–204 (TO–3)
CASE 197A–05
ISSUE K

DATE 21 FEB 2000





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

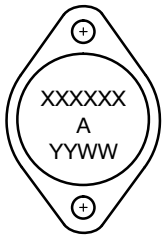
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. ANODE = 1
2. ANODE = 2
CASE: CATHODES

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Locationa
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking.

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STATUS:	**ON SEMICONDUCTOR STANDARD**		
NEW STANDARD:			
DESCRIPTION:	**TO–204 (TO–3)**		**PAGE 1 OF 2**

ISSUE	REVISION	DATE
K	LEGALLY CHANGED TO ON	21 FEB 2000

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