MJ802

High-Power NPN Silicon Transistor

This transistor is for use as an output device in complementary audio amplifiers to 100−Watts music power per channel.

Features

- High DC Current Gain − h_{FE} = 25−100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the PNP MJ4502
- Pb−Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CER}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Collector−Emitter Voltage	V_{CEO}	90	Vdc
Emitter−Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	0.875	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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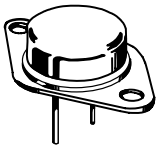
30 AMPERE
POWER TRANSISTOR
NPN SILICON
100 VOLTS − 200 WATTS



TO−204AA (TO−3)
CASE 1−07
STYLE 1

MARKING DIAGRAM

MJ802 = Device Code
G = Pb−Free Package
A = Assembly Location
YY = Year
WW = Work Week
MEX = Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
MJ802	TO−204	100 Units / Tray
MJ802G	TO−204 (Pb−Free)	100 Units / Tray

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (I_C = 200 mAdc, R_{BE} = 100 Ω)	BV_{CER}	100	−	Vdc
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	−	Vdc
Collector−Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 – –	 1.0 5.0	mAdc
Emitter−Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	−	1.0	mAdc
ON CHARACTERISTICS(1)				
DC Current Gain (Note 1) (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	−
Base−Emitter “On” Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	−	1.3	Vdc
Collector−Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	−	0.8	Vdc
Base−Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	−	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	−	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

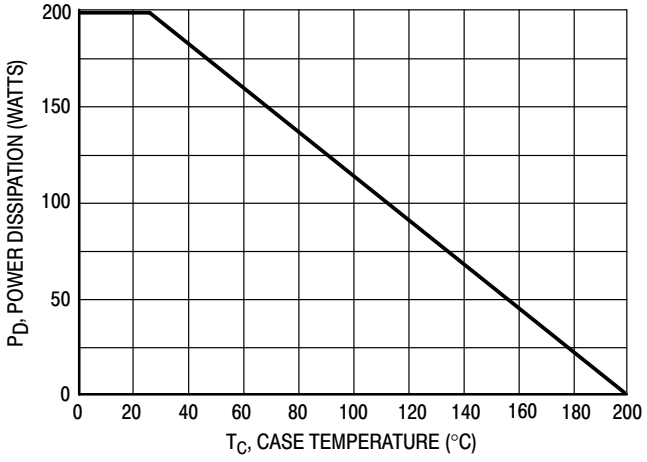


Figure 1. Power−Temperature Derating Curve

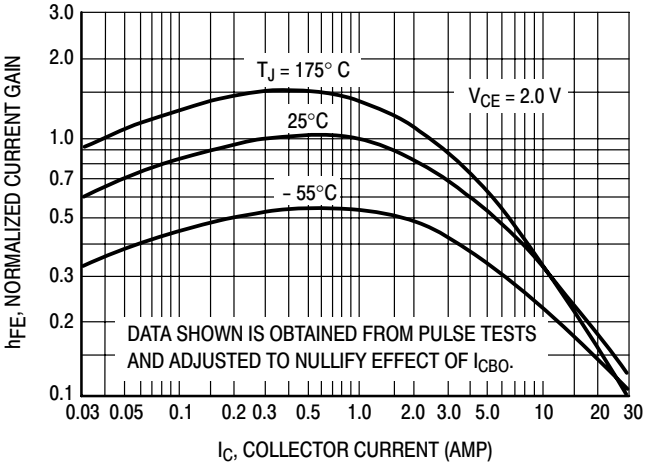


Figure 2. DC Current Gain

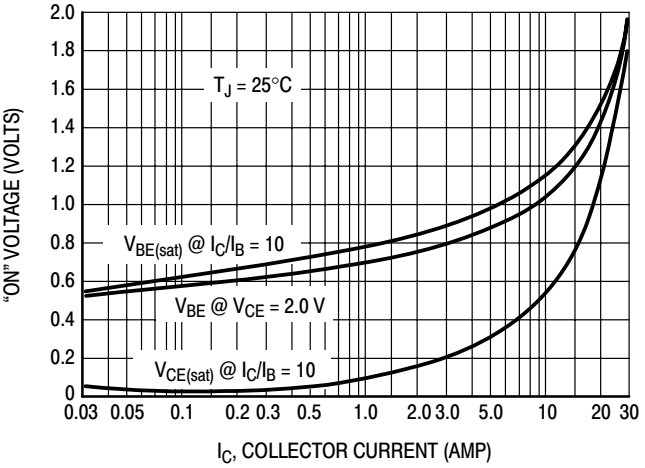


Figure 3. "On" Voltages

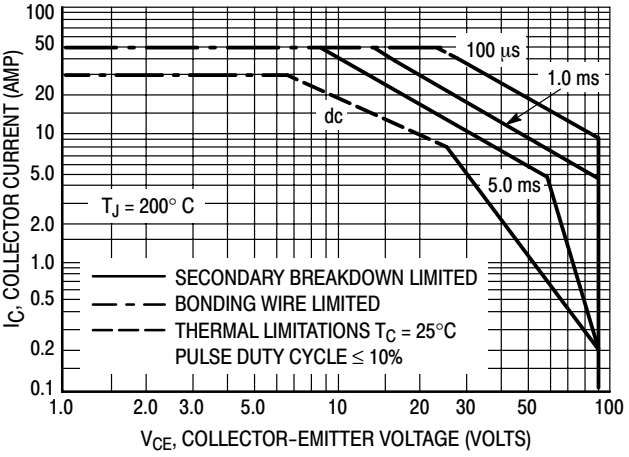
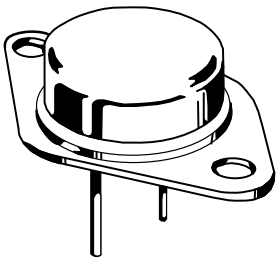


Figure 4. Active Region Safe Operating Area

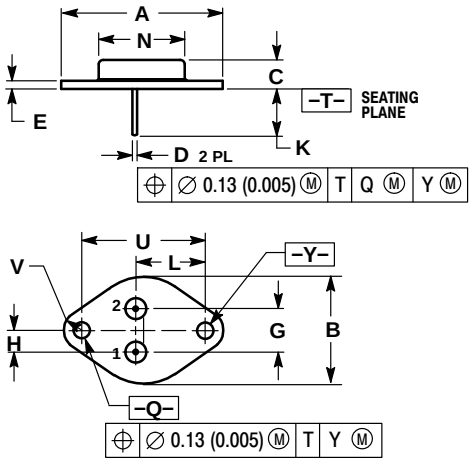
The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power temperature derating must be observed for both steady state and pulse power conditions.



SCALE 1:1

TO−204 (TO−3)
CASE 1−07
ISSUE Z

DATE 05/18/1988



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

PUBLICATION ORDERING INFORMATION

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