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# Low-Voltage CMOS Octal Transceiver/Registered Transceiver With Dual Enable

## With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX652 is a high performance, non-inverting octal transceiver/registered transceiver operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX652 inputs to be safely driven from 5 V devices. The MC74LCX652 is suitable for memory address driving and all TTL level bus oriented transceiver applications.


Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes from a LOW-to-HIGH logic level. Two Output Enable pins ( $\overline{OEBA}$ , OEAB) are provided to control the transceiver outputs. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls (SBA, SAB) can multiplex stored and real-time (transparent mode) data. In the isolation mode (both outputs disabled), A data may be stored in the B register or B data may be stored in the A register. When in the real-time mode, it is possible to store data without using the internal registers by simultaneously enabling OEAB and  $\overline{OEBA}$ . In this configuration, each output reinforces its input (data retention is not guaranteed in this mode).

- Designed for 2.3 to 3.6 V  $V_{CC}$  Operation
- 5 V Tolerant – Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0$  V
- LVTTTL Compatible
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V

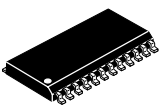
# MC74LCX652

# LCX

**LOW-VOLTAGE CMOS  
OCTAL TRANSCEIVER/  
REGISTERED TRANSCEIVER  
WITH DUAL ENABLE**



**DT SUFFIX**  
24-LEAD PLASTIC TSSOP PACKAGE  
CASE 948H

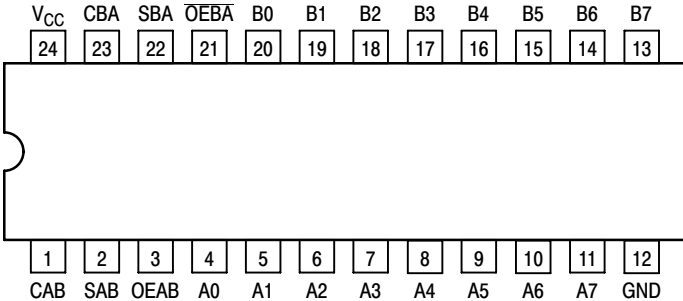


**DW SUFFIX**  
24-LEAD PLASTIC SOIC PACKAGE  
CASE 751E

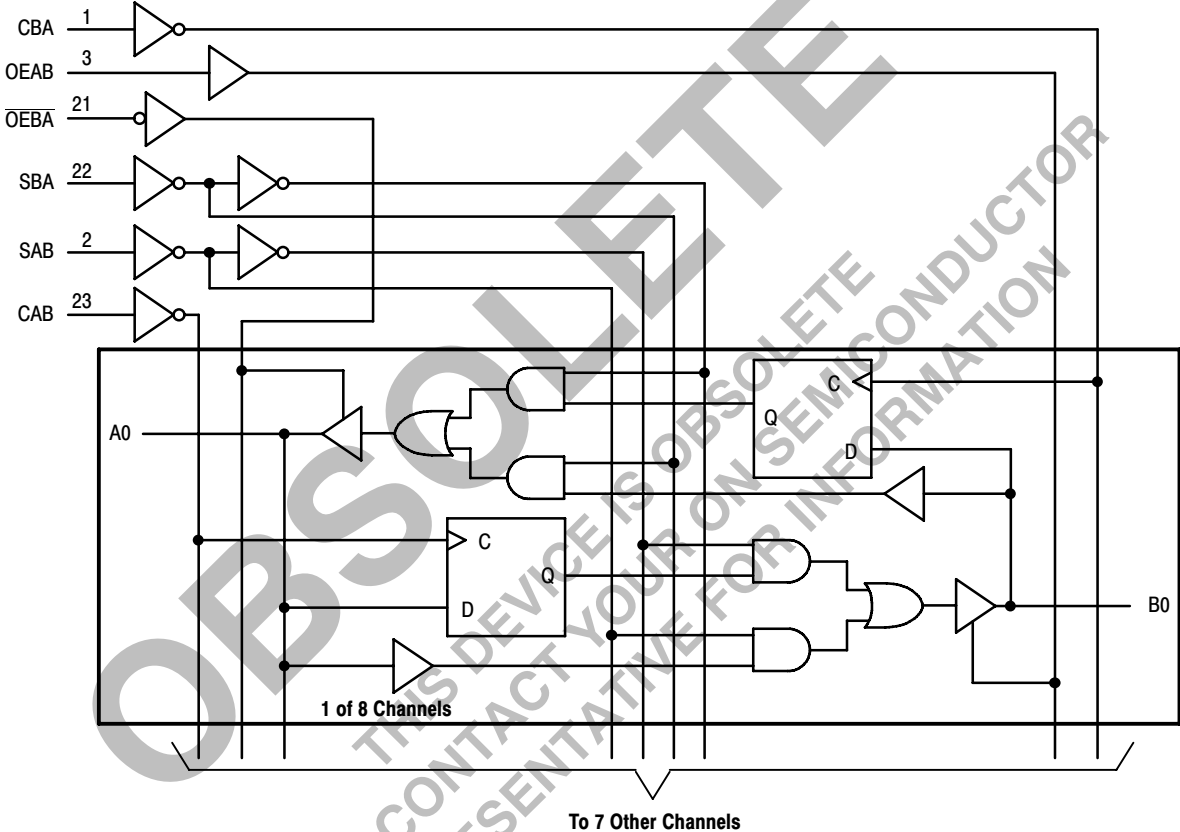
**Figure 1. PIN NAMES**

Pins	Function
A0-A7	Side A Inputs/Outputs
B0-B7	Side B Inputs/Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Select Control Inputs
OEBA, OEAB	Output Enable Inputs

**MC74LCX652**



**Figure 2. 24-Lead Pinout (Top View)**



**Figure 3. Logic Diagram**

# MC74LCX652

## TRUTH TABLE

Inputs						Data Ports		Operating Mode
OEAB	OEBA	CAB	CBA	SAB	SBA	An	Bn	
L	H					Input	Input	
		↑	↑	X	X	X	X	Isolation, Hold Storage
		↑	↑	X	X	l h	l h	Store A and/or B Data
H	H					Input	Output	
		↑	X*	L	X	L H	L H	Real Time A Data to B Bus
				H	X	X	QA	Stored A Data to B Bus
		↑	X*	L	X	l h	L H	Real Time A Data to B Bus; Store A Data
				H	X	L H	QA QA	Clock A Data to B Bus; Store A Data
L	L					Output	Input	
		X*	↑	X	L	L H	L H	Real Time B Data to A Bus
				X	H	QB	X	Stored B Data to A Bus
		X*	↑	X	L	L H	l h	Real Time B Data to A Bus; Store B Data
				X	H	QB QB	L H	Clock B Data to A Bus; Store B Data
H	L					Output	Output	
		↑	↑	H	H	QB	QA	Stored A Data to B Bus, Stored B Data to A Bus

H = High Voltage Level

h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition

L = Low Voltage Level

l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition

X = Don't Care

↑ = Low-to-High Clock Transition

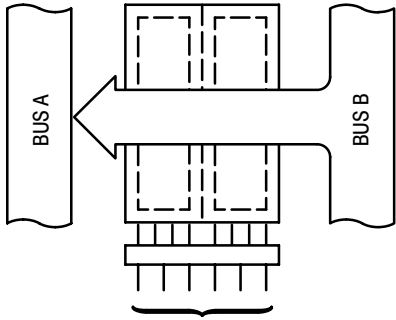
↑ = NOT Low-to-High Clock Transition

QA = A input storage register

QB = B input storage register

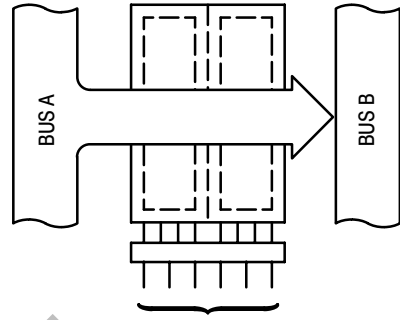
\* = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I<sub>CC</sub> reasons, Do Not Float Inputs.

Real Time Transfer – Bus B to Bus A



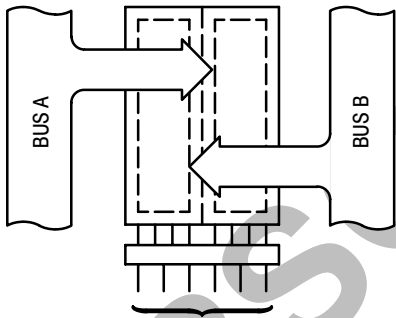
OEAB	OEBA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

Real Time Transfer – Bus A to Bus B



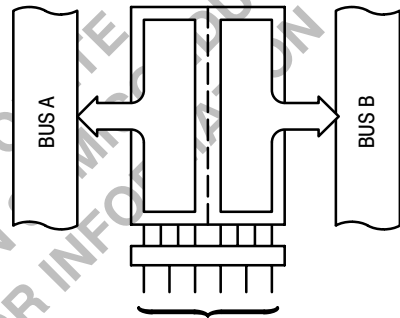
OEAB	OEBA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

Store Data from Bus A, Bus B or Bus A and Bus B



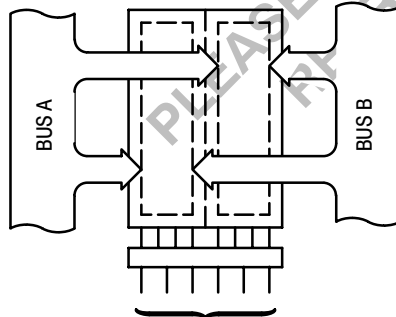
OEAB	OEBA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer A Stored Data to Bus B or B Stored Data to Bus A or Both at the Same Time



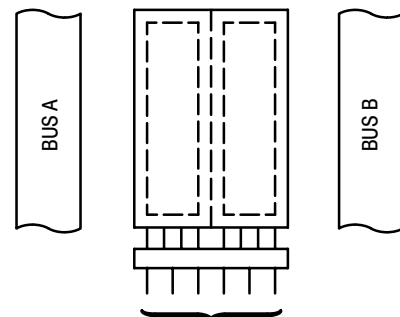
OEAB	OEBA	CAB	CBA	SAB	SBA
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store Bus A in Both Registers or Store Bus B in Both Registers



OEAB	OEBA	CAB	CBA	SAB	SBA
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



OEAB	OEBA	CAB	CBA	SAB	SBA
L	H	H or L	H or L	X	X

Figure 4. Bus Applications

# MC74LCX652

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq +7.0$	Output in 3-State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Note 1.	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Output in HIGH or LOW State.  $I_O$  absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
$V_{CC}$	Supply Voltage	Operating	2.0	3.3	3.6	V
		Data Retention Only	1.5	3.3	3.6	
$V_I$	Input Voltage	0		5.5	V	
$V_O$	Output Voltage (HIGH or LOW State) (3-State)	0		$V_{CC}$	V	
		0		5.5		
$I_{OH}$	HIGH Level Output Current, $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$			-24	mA	
$I_{OL}$	LOW Level Output Current, $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$			24	mA	
$I_{OH}$	HIGH Level Output Current, $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$			-12	mA	
$I_{OL}$	LOW Level Output Current, $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$			12	mA	
$T_A$	Operating Free-Air Temperature	-40		+85	$^{\circ}C$	
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8 V to 2.0 V, $V_{CC} = 3.0\text{ V}$	0		10	ns/V	

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Unit
			Min	Max	
$V_{IH}$	HIGH Level Input Voltage (Note 2.)	$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	2.0		V
$V_{IL}$	LOW Level Input Voltage (Note 2.)	$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$		0.8	V
$V_{OH}$	HIGH Level Output Voltage	$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.7\text{ V}$ ; $I_{OH} = -12\text{ mA}$	2.2		
		$V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -18\text{ mA}$	2.4		
		$V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -24\text{ mA}$	2.2		
$V_{OL}$	LOW Level Output Voltage	$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ ; $I_{OL} = 100\text{ }\mu\text{A}$		0.2	V
		$V_{CC} = 2.7\text{ V}$ ; $I_{OL} = 12\text{ mA}$		0.4	
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 16\text{ mA}$		0.4	
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 24\text{ mA}$		0.55	

2. These values of  $V_I$  are used to test DC electrical characteristics only.

# MC74LCX652

## DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
I <sub>I</sub>	Input Leakage Current	2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V; 0 V ≤ V <sub>I</sub> ≤ 5.5 V		±5.0	μA
I <sub>OZ</sub>	3-State Output Current	2.7 ≤ V <sub>CC</sub> ≤ 3.6 V; 0 V ≤ V <sub>O</sub> ≤ 5.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.7 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub>		10	μA
		2.7 ≤ V <sub>CC</sub> ≤ 3.6 V; 3.6 ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5 V		±10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.7 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		500	μA

## AC CHARACTERISTICS (t<sub>R</sub> = t<sub>F</sub> = 2.5 ns; C<sub>L</sub> = 50 pF; R<sub>L</sub> = 500 Ω)

Symbol	Parameter	Waveform	Limits				Unit
			T <sub>A</sub> = -40°C to +85°C				
			V <sub>CC</sub> = 3.0 V to 3.6 V		V <sub>CC</sub> = 2.7 V		
			Min	Max	Min	Max	
f <sub>max</sub>	Clock Pulse Frequency	3	150				MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Input to Output	1	1.5 7.0	7.0 1.5	1.5 8.0	8.0 8.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Output	3	1.5 8.5	8.5 1.5	1.5 9.5	9.5 9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Select to Output	1	1.5 8.5	8.5 1.5	1.5 9.5	9.5 9.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to High and Low Level	2	1.5 8.5	8.5 1.5	1.5 9.5	9.5 9.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time From High and Low Level	2	1.5 8.5	8.5 1.5	1.5 9.5	9.5 9.5	ns
t <sub>s</sub>	Setup Time, HIGH or LOW Data to Clock	3	2.5		2.5		ns
t <sub>h</sub>	Hold Time, HIGH or LOW Data to Clock	3	1.5		1.5		ns
t <sub>w</sub>	Clock Pulse Width, HIGH or LOW	3	3.3		3.3		ns
t <sub>OSSL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 3.)			1.0 1.0			ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

## DYNAMIC SWITCHING CHARACTERISTICS

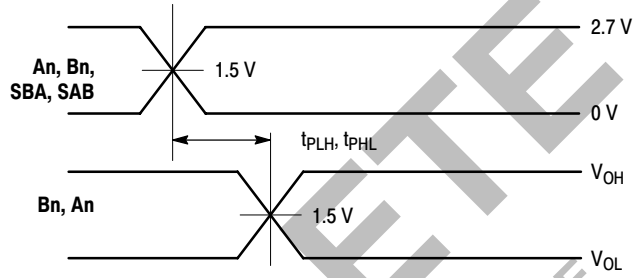
Symbol	Condition	T <sub>A</sub> = +25°C			Unit
		Min	Typ	Max	
V <sub>OLP</sub>	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V		0.8		V
V <sub>OLV</sub>	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V		0.8		V

4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state. The LCX652 is characterized with 7 outputs switching with 1 output held LOW.

# MC74LCX652

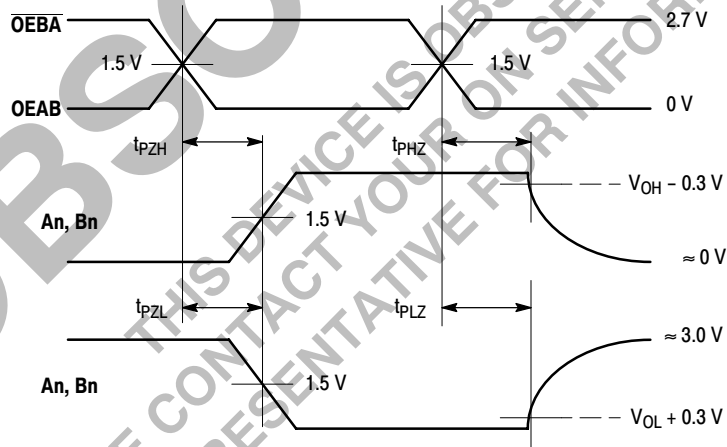
## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = 3.3\text{ V}$ , $V_I = 0\text{ V}$ or $V_{CC}$	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3\text{ V}$ , $V_I = 0\text{ V}$ or $V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	10 MHz, $V_{CC} = 3.3\text{ V}$ , $V_I = 0\text{ V}$ or $V_{CC}$	25	pF



**WAVEFORM 1 – SAB to B and SBA to A, An to Bn PROPAGATION DELAYS**

$t_R = t_F = 2.5\text{ ns}$ , 10% to 90%;  $f = 1\text{ MHz}$ ;  $t_W = 500\text{ ns}$



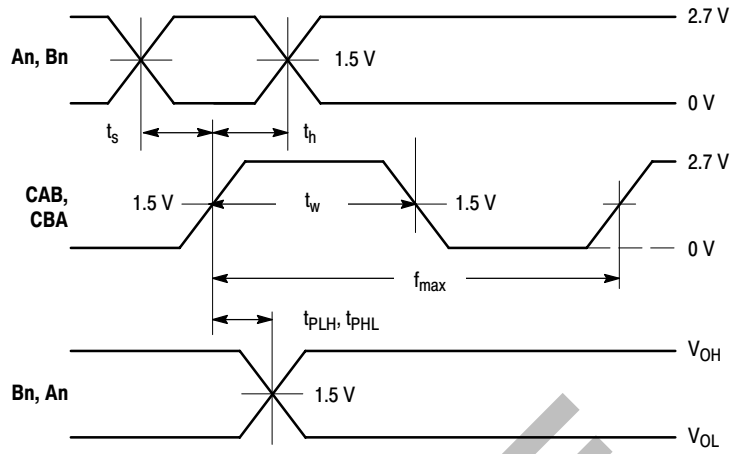
**WAVEFORM 2 – OEBA/OEAB to An/Bn OUTPUT ENABLE AND DISABLE TIMES**

$t_R = t_F = 2.5\text{ ns}$ , 10% to 90%;  $f = 1\text{ MHz}$ ;  $t_W = 500\text{ ns}$

**Figure 5. AC Waveforms**

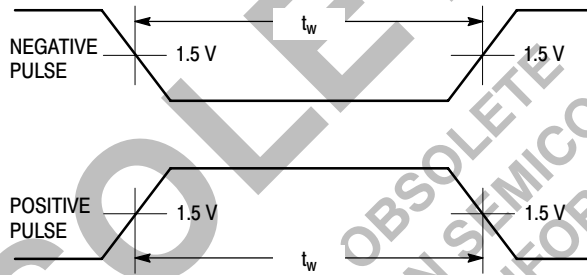


# MC74LCX652



**WAVEFORM 3 - CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES**

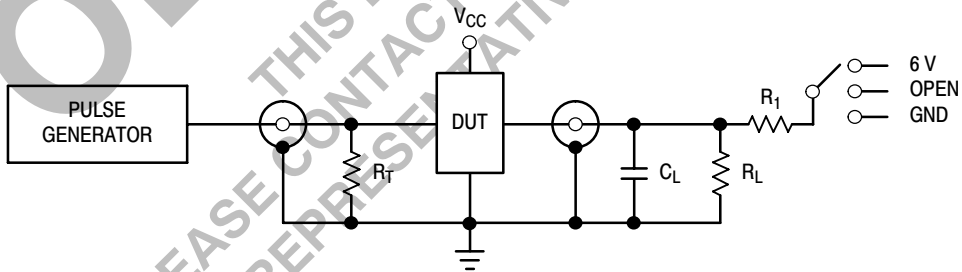
$t_R = t_F = 2.5$  ns, 10% to 90%;  $f = 1$  MHz;  $t_W = 500$  ns except when noted



**WAVEFORM 4 - INPUT PULSE DEFINITION**

$t_R = t_F = 2.5$  ns, 10% to 90% of Q V to 2.7 V

**Figure 5. AC Waveforms (Continued)**



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6 V
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6 V
$t_{PZH}, t_{PHZ}$	GND

$C_L = 50$  pF or equivalent (Includes jig and probe capacitance)

$R_L = R_1 = 500 \Omega$  or equivalent

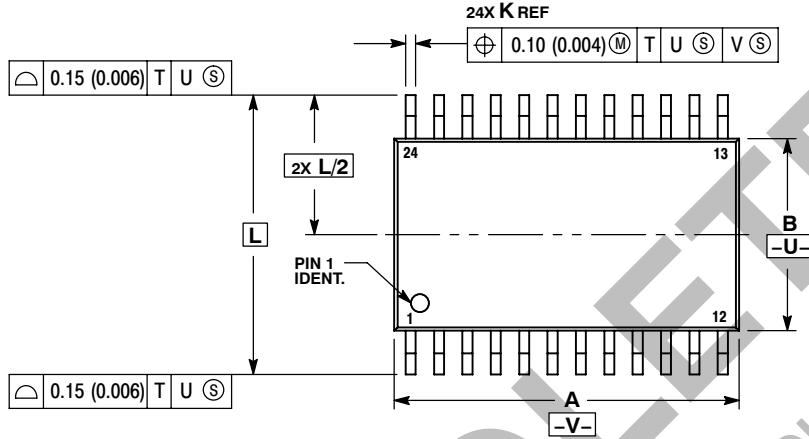
$R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

**Figure 6. Test Circuit**

# MC74LCX652

## PACKAGE DIMENSIONS

DT SUFFIX  
 PLASTIC TSSOP PACKAGE  
 CASE 948H-01  
 ISSUE O

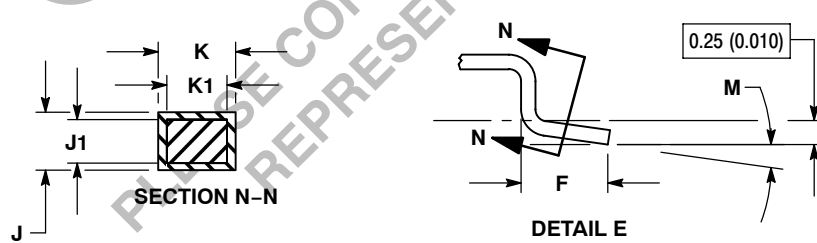
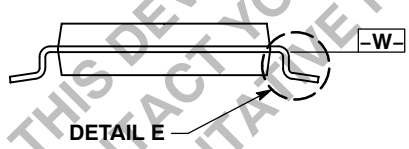


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.



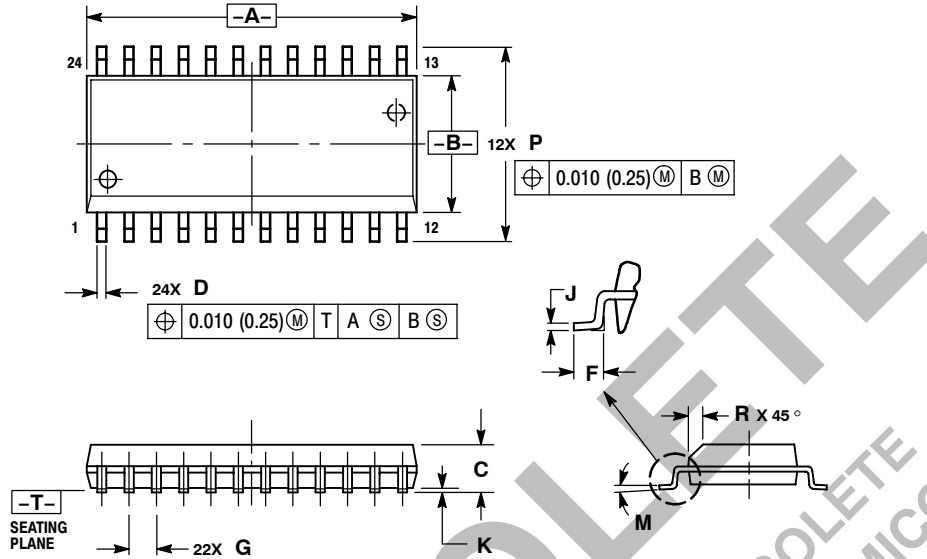
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



# MC74LCX652

## PACKAGE DIMENSIONS

**DW SUFFIX**  
 PLASTIC SOIC PACKAGE  
 CASE 751E-04  
 ISSUE E



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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