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# **Quad Power MOSFET**

# 24 V, 15 A, N-Channel

#### **Features**

- Four N-Channel MOSFETs in a Single Package
- High Drain Current (Up to 80A per Device, Single Pulse  $t_p < 10 \mu s$ ,  $R_{\theta JC} = 1.5 \, ^{\circ}C/W)$
- High Input Impedance for Ease of Drive
- Ultra Low On-resistance (R<sub>DS(on)</sub>) Provides Low Conduction Losses
- Very Fast Switching Times Provides Low Switching Losses
- Low Parasitic Inductance
- Low Stored Charge for Efficient Switching
- Very Low V<sub>SD</sub> Ideal for Synchronous Rectification
- 200% Footprint Reduction Compared to Similar DPAK Solution for the Same Power
- Advanced Leadless Power Integrated Package

### **Applications**

- DC-DC Converters
- Motherboard/Server Voltage Regulator
- Telecomm/Industrial Power Supply
- H-Bridge Circuits
- Low Voltage Motor Control

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Units
Drain-to-Source Voltage			$V_{DSS}$	24	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain	Steady	T <sub>A</sub> =25°C	l <sub>D</sub>	15	Α
Current (Note 1)	State	T <sub>A</sub> =85°C	-0	10.9	
	t≤10 s	T <sub>A</sub> =25°C	0 /	18.8	
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> =25°C	P <sub>D</sub>	2.9	W
	t≤10 s	4×1		4.5	
Continuous Drain	Steady	T <sub>A</sub> =25°C	I <sub>D</sub>	11.4	Α
Current (Note 2)	State	T <sub>A</sub> =85°C		8.2	
Power Dissipation (Note 2)		T <sub>A</sub> =25°C	P <sub>D</sub>	1.7	W
Pulsed Drain Current	tp=10 μs	•	I <sub>DM</sub>	32	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C
Source Current (Body Diode)			IS	15	Α
Single Pulse Drain-to-Source Avalanche Energy $-$ (V <sub>DD</sub> = 25 V, V <sub>G</sub> =10 V, I <sub>PK</sub> =60 A, L=0.1 mH, R <sub>G</sub> = 1.0 k $\Omega$ )			EAS	80	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C



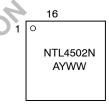
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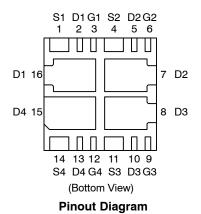
V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> TYP	I <sub>D</sub> MAX (Note 1)
24 V	8.0 mΩ @ 4.5 V	15 A
	11.2 mΩ @ 10 V	L IOA

### **MARKING DIAGRAM**





= Specific Device Code = Assembly Location = Year ww = Work Week



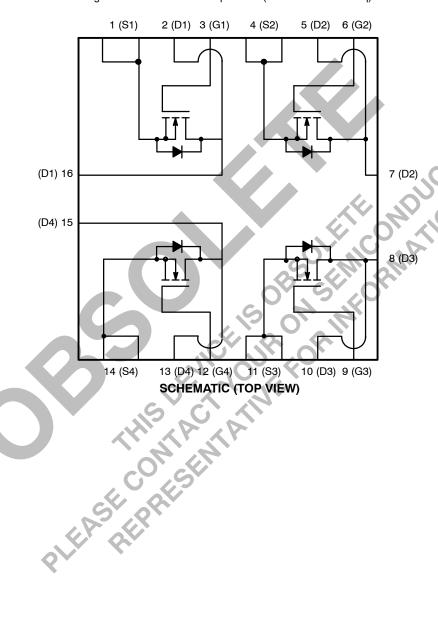
#### **ORDERING INFORMATION**

Device	Package	Shipping		
NTL4502NT1	QFN16 FBIP	1500 / Tape & Reel		

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Case (Drain)	$R_{ heta JC}$	1.5	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	43	
Junction-to-Ambient - t≤10 s (Note 1)	$R_{\theta JA}$	27.5	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	75	

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
   Surface-mounted on FR4 board using minimum recommended pad size (Cu area = 0.440 in sq).



# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Test Condi	tion	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•	•			•		
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		24	27.5		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /				25.5		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V,	T <sub>J</sub> =25°C			1.5	μА
		V <sub>GS</sub> = 0 V	T <sub>J</sub> =125°C			10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{GS} = \pm 20 \text{ V, } V_{I}$	<sub>DS</sub> = 0 V			±100	nA
ON CHARACTERISTICS (Note 3)				_			
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D =$	: 250 μA	1.0	1.5	2.0	V
Gate Threshold Voltage Temperature Coefficient	V <sub>GS(th)</sub> /T <sub>J</sub>				-4.1		mV/°C
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub>	= 15 A		11.2	13	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub>	= 15 A		8.0	11	
Forward Transconductance	9FS	$V_{DS} = 10 \text{ V}, I_{D}$	= 15 A	Þ	27		S
CHARGES AND CAPACITANCES							
Input Capacitance	C <sub>iss</sub>				1070	1605	pF
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 20 V, V <sub>G</sub> f = 1.0 MH		& C	408	612	
Reverse Transfer Capacitance	C <sub>rss</sub>		-0		142	213	
Total Gate Charge	Q <sub>G(TOT)</sub>		000	0 110	13		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub>	= 15 A,	) <sub>V</sub> O'	1.6		
Gate-to-Source Charge	Q <sub>GS</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}, V_{DS} = 24 \text{ V}$		191	3.3		
Gate-to-Drain Charge	$Q_{GD}$		0		7.0		
SWITCHING CHARACTERISTICS, VGS	s = 10 V (Note	e 4)	), \O,	,			
Turn-On Delay Time	t <sub>d(ON)</sub>	10			5.0	8.5	ns
Rise Time	t <sub>r</sub>	$V_{GS}$ = 10 V, $V_{DD}$ = 12 V, $I_{D}$ = 15 A, $R_{G}$ = 3.0 $\Omega$			28	47	
Turn-Off Delay Time	t <sub>d(OFF)</sub>				22	37	
Fall Time	t <sub>f</sub>	$X_{L}X_{L}$			6.0	10	
SWITCHING CHARACTERISTICS, VGS	s = <b>4.5 V</b> (Note	e 4)					
Turn-On Delay Time	t <sub>d(ON)</sub>	,5°			9.5	16	ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DE</sub>	<sub>0</sub> = 12 V,		33	55	
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$I_D = 15 \text{ A}, R_G = 3.0 \Omega$			14	23.5	7
Fall Time	t <sub>f</sub>				7.5	12.5	
DRAIN-SOURCE DIODE CHARACTER	RISTICS						
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V,	T <sub>J</sub> =25°C		0.8	1.2	V
		I <sub>S</sub> = 15 A	T <sub>J</sub> =125°C		0.7		7
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V},$ $dI_{S}/dt = 100 \text{ A}/\mu\text{s}, I_{S} = 15 \text{ A}$			31		ns
Charge Time	ta				17		7
Discharge Time	t <sub>b</sub>				14		7
Reverse Recovery Charge	Q <sub>RR</sub>				20		nC

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

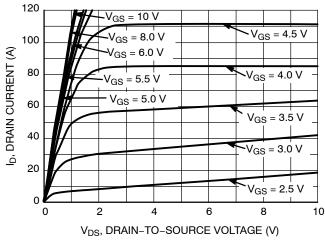


Figure 1. On-Region Characteristics

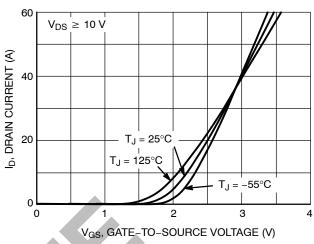


Figure 2. Transfer Characteristics

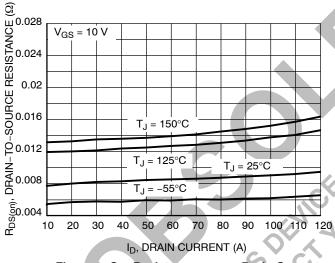


Figure 3. On-Resistance versus Drain Current and Temperature

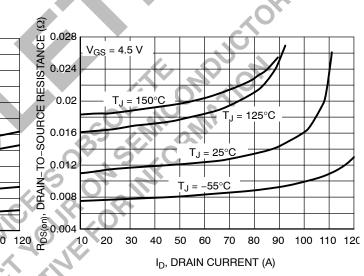


Figure 4. On-Resistance versus Drain Current and Temperature

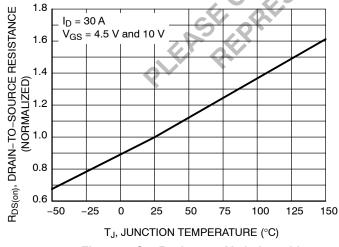


Figure 5. On–Resistance Variation with Temperature

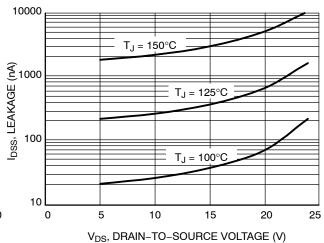
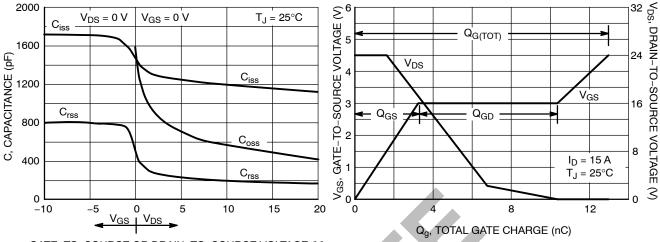


Figure 6. Drain-to-Source Leakage Current versus Voltage



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (V)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source
Voltage versus Total Charge

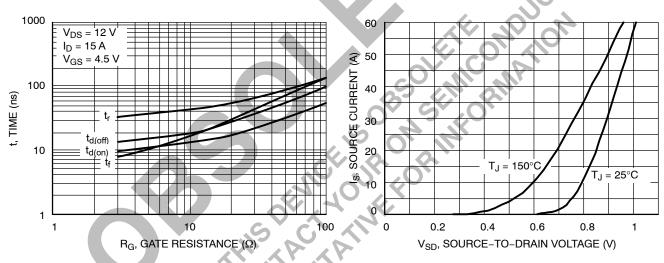


Figure 9. Resistive Switching Time Variation versus Gate Resistance

Figure 10. Diode Forward Voltage versus Current

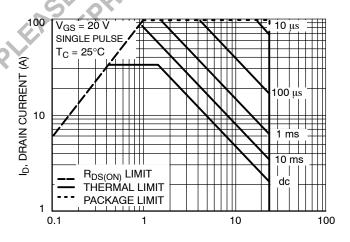
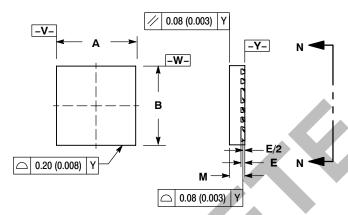
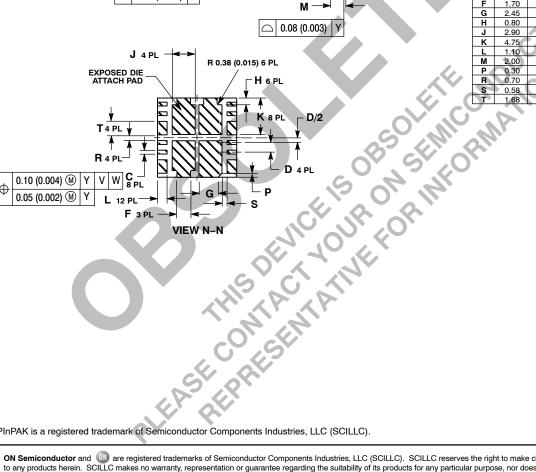


Figure 11. Maximum Rated Forward Biased Safe Operating Area

## PACKAGE DIMENSIONS

### **QFN16 FBIP** CASE 495-01 **ISSUE A**





#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- COPLANARITY APPLIES TO LEAD. DIE ATTACHED PAD.
- OPTIONAL FEATURES ARE FOR REFERENCE ONLY.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	10.40	10.60	0.409	0.417	
В	10.40	10.60	0.409	0.417	
C	0.40	0.50	0.016	0.020	
D	1.27	BSC	0.050	BSC	
Е	0.50	0.52	0.020	0.020	
F	1.70	1.90	0.067	0.075	
G	2.45	2.55	0.096	0.100	
Н	0.80	1.00	0.031	0.039	
J	2.90	3.10	0.114	0.122	
K	4.75	4.95	0.187	0.195	
L	1.10	1.30	0.043	0.051	
M	2.00	2.20	0.079	0.087	
P	0.30	0.50	0.012	0.020	
R	0.70	0.90	0.028	0.035	
S	0.58	0.78	0.023	0.031	
T	1.68	1.78	0.066	0.070	

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