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AN-9075/D

Smart Power Module, Motion 1200 V SPM 2 Series User's Guide

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APPLICATION NOTE

INTRODUCTION

This application note supports the 1200−V rated Motion SPM® family. It should be used in conjunction with Motion SPM 2 datasheets, Motion SPM evaluation board user guides (FEB212_001), and application notes AN−9079 − Thermal Performance Information and AN−9076 − Mounting Guidance.

Design Concept

Minimized package and a low power consumption module with improved reliability. This is achieved by applying a new 1200 V gate−driving high−voltage integrated circuit (HVIC), a new insulated−gate bipolar transistor (IGBT) of advanced silicon technology, and improved direct bonded copper (DBC) substrate base transfer mold package. Motion SPM 2 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverterized motor drives for industrial use, such as air conditioners, general−purpose inverters, and serve motors.

A design advantage integrates an NTC thermistor for temperature measuring of power chips (e.g. IGBTs, Fast−Recovery Diode (FRDs) on the same substrate. Most customers want to know the exact temperature of power chips because temperature affects the quality, reliability, and longevity of products. This desire is thwarted because integrated power chips (e.g. IGBTs, FRD) inside modules operate in high−voltage conditions. Therefore, instead of directly sensing the temperature of power chips, customers have been using an external NTC thermistor for sensing the temperature of the module or heat−sink. This method doesn't accurately reflect the temperature of power components due to cost, but is simple. The NTC thermistor of the Motion SPM 2 is integrated with the power chips on the same ceramic substrate and therefore more accurately reflects the temperature of power chips.

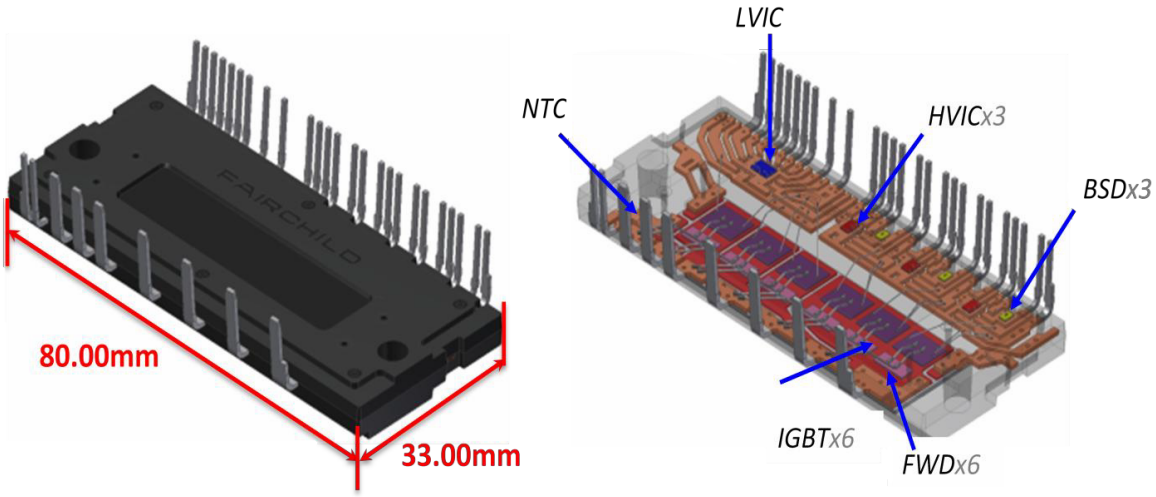


Figure 1. External View and Internal Structure of Motion SPM 2 Series

Table 1. PRODUCT LINE−UP AND TARGET APPLICATION

Target Application	Device	IGBT Rating	Motor Rating (Note 1)	Isolation Voltage
Motor Drives for Individual Use, System Air Conditioners, General Purpose Inverters, Servo Motors	FNA21012A	10 A/1200 V	1.5 kW/440 V_{AC}	V_{ISO} = 2500 V_{RMS} (Sine 60 Hz, 1−min. All Shorted Pins Heat Sink)
	FNA22512A	25 A/1200 V	3.7 kW/440 V_{AC}	
	FNA23512A	35 A/1200 V	5.5 kW/440 V_{AC}	
	FNA25012A	50 A/1200 V	7.5 kW/440 V_{AC}	

1. These motor ratings are simulation results under following conditions: V_{AC} = 440 V, V_{DD} = 15 V, T_C = 100°C, T_j = 150°C, f_{PWM} = 5 kHz, PF = 0.8, MI = 0.9, Motor efficiency = 0.75, overload 150% for 1min.
These motor ratings are general ratings, so may be changed by conditions.

Features and Integrated Functions

- DBC Substrate
  - Excellent Thermal Conductivity, Keeping 2500 Vrms Isolation Voltage from Pin to Heat Sink
- Integrated Components:
  - One−Channel HVIC (three HVIC) for High−Side IGBTs Control
  - Three−Channel LVIC (one LVIC) for Low−Side IGBTs Control
  - Six IGBTs/Diodes; Sense IGBTs for Low−Side
  - NTC Thermistor for Temperature Sensing
  - Bootstrap Diodes
- Control Drive Supply:
  - Single DC Supply Compatible Using Integrated Bootstrap Diode
- High−Side Gate Driver (One−Channel)
  - High−Voltage Level−Shift Circuit
  - Input interface: Active HIGH
  - Compatible with 3.3 V Controller Outputs
  - Under−Voltage Lockout without Fault Signal
- Low−Side Gate Driver (Three−Channel)
  - Input Interface: Active HIGH
  - Compatible with 3.3 V Controller Outputs
  - Under−Voltage Lockout with Fault Signal
  - Short−Circuit & Over−Current Protection
- Detecting Sense Current from External Resistor (RSC) with RSC Pin
- Soft Turn−off for Preventing Excessive Surge Voltage
- Controllable Fault−Out Duration by External Capacitor (C_{FOD}) with CFOD Pin

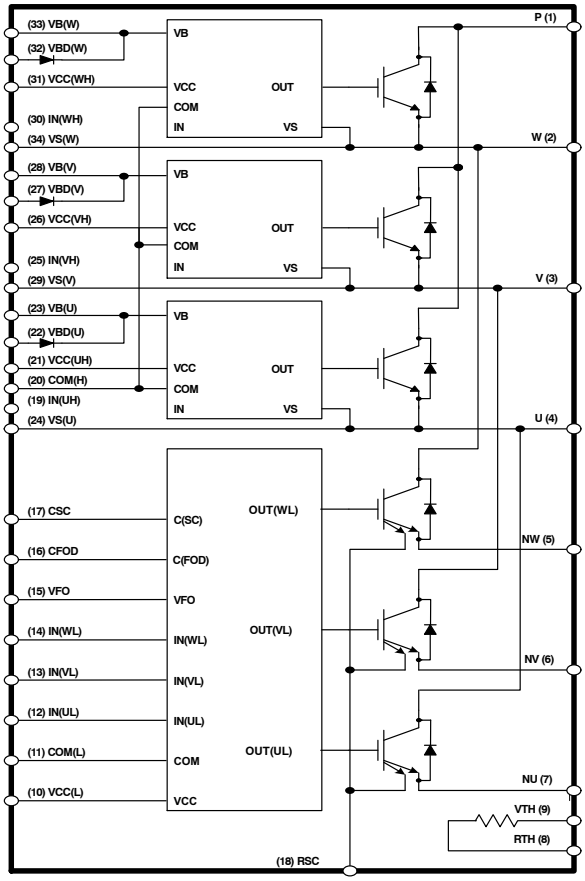


Figure 2. Internal Equivalent Circuit, Input/Output Pins

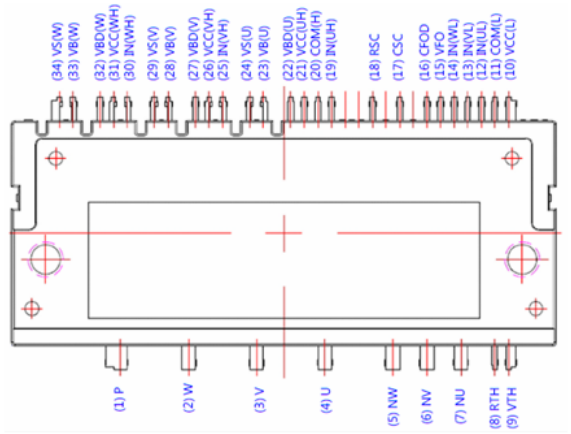


Figure 3. Package Top−view and Pin Assignment

PRODUCT SYNOPSIS

This section discusses pin descriptions, electrical specifications, characteristics, and packaging.

Table 2. PIN DESCRIPTION

Pin Number	Name	Description
1	P	Positive DC Link Input
2	W	Output for W Phase
3	V	Output for V Phase
4	U	Output for U Phase
5	NW	Negative DC Link Input for W Phase
6	NV	Negative DC Link Input for V Phase
7	NU	Negative DC Link Input for U Phase
8	RTH	Series Resistor for Thermistor (Temperature Detection)
9	VTH	Thermistor Bias Voltage
10	VCC(L)	Low−Side Bias Voltage for IC and IGBT Driving
11	COM(L)	Low−Side Common Supply Ground
12	IN(UL)	Signal Input for Low−Side U Phase
13	IN(VL)	Signal Input for Low−Side V Phase
14	IN(WL)	Signal Input for Low−Side W Phase
15	VFO	Fault Output
16	CFOD	Capacitor for Fault Output Duration Selection
17	CSC	Capacitor (Low−Pass Filter) for Short−Circuit Current Detection Input
18	RSC	Resistor for Short−Circuit Current Detection
19	IN(UH)	High−Side Common Supply Ground
20	COM(H)	No Connection
21	VCC(UH)	High−Side Bias Voltage for U Phase IGBT Driving
22	VBD(U)	Anode of Bootstrap Diode for High−Side U Phase
23	VB(U)	High−Side Bias Voltage for U Phase IGBT Driving
24	VS(U)	High−Side Bias Voltage Ground for U Phase IGBT Driving
25	IN(VH)	Signal Input for High−Side V Phase
26	VCC(VH)	High−Side Bias Voltage for V Phase IC
27	VBD(V)	Anode of Bootstrap Diode for High−Side V Phase
28	VB(V)	High−Side Bias Voltage for V Phase IGBT Driving
29	VS(V)	High−Side Bias Voltage Ground for V Phase IGBT Driving
30	IN(WH)	Signal Input for High−Side W Phase
31	VCC(WH)	High−Side Bias Voltage for W Phase IC
32	VBD(W)	Anode of Bootstrap Diode for High−Side W Phase
33	VB(W)	High−Side Bias Voltage for W Phase IGBT Driving
34	VS(W)	High−Side Bias Voltage Ground for W Phase IGBT Driving

Detailed Pin Definition & Notification

- High−side bias voltage pins for driving the IGBT/ high−side bias voltage ground pins for driving the IGBTs:
  - ♦ Pins: VB(U)−VS(U), VB(V)−VS(V), VB(W)−VS(W)
  - – These are drive power supply pins for providing gate drive power to the high−side IGBTs.
  - – By virtue of the ability of bootstrap, the circuit scheme is that no external power supplies are required for the high−side IGBTs.
  - – Each bootstrap capacitor is charged from the V_{CC} supply during ON state of the corresponding low−side IGBT.
  - – To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, low−ESL filter capacitor should be mounted very close to these pins.
- Low−Side Bias Voltage Pin/High−Side Bas Voltage Pins:
  - ♦ Pins: VCC(L), VCC(WH), VCC(VH), VCC(UH)
  - – These are control supply pins for the built−in ICs.
  - – These four pins should be connected externally.
  - – To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, low−ESL filter capacitor should be mounted very close to these pins.
- Low−Side Common Supply Ground Pins:
  - ♦ Pins: COM(L), COM(H)
  - – These are supply ground pins for the built−in ICs.
  - – These two pins should be connected externally.
  - – **Important!** To avoid noise influences, the main power circuit current should not be allowed to flow through this pin.
- Anode Pins of Bootstrap Diode:
  - ♦ Pins: VBD(UH), VBD(VH), VBD(WH),
  - – These are pins to connect internal bootstrap diode for each high−side bootstrapping.
  - – External resistor should be connected between these pins and each V_{CC}(xH).
- Signal Input Pins:
  - ♦ Pins: IN(UL), IN(VL), IN(WL), IN(UH), IN(VH), IN(WH)
  - – These pins control the operation of the built−in IGBTs.
  - – They are activated by voltage input signals. The terminals are internally connected to a Schmitt−trigger circuit composed of 5 V−class CMOS.
  - – The signal logic of these pins is active HIGH. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
  - – The wiring of each input should be as short as possible to protect the Motion SPM 2 against noise influences.
  - – To prevent signal oscillations, a RC coupling as illustrated in Figure 45 is recommended.
- Resistor Connection Pin for Short−Circuit Current Detection
  - ♦ Pin: RSC
  - – Low−side sense IGBT current flows through this pin. Short−circuit and over−current can be detected at this pin through an external resistor. (refer to Figure 45)
  - – If using three shunt resistors at N terminals for OCP and SCP without sense detecting from RSC, RSC should be connected to COM.
- Short−Circuit and Over−Current Detection Input Pin
  - ♦ Pin: CSC
  - – The current sense current detecting resistor (R_{SC}) should be connected between CSC and COM pins to detect over−current and short−circuit current. (refer to Figure 45).
    The shunt resistor should be selected to meet the detection levels matched for the specific application. The RC filter should be connected to the CSC pin to eliminate noise.
  - – The connection length between the shunt resistor and CSC pin should be minimized.
- Fault Output Pin
  - ♦ Pin: VFO
  - – This is the fault output alarm pin. An active LOW output is given on this pin for a fault state condition in the SPM.
  - – The alarm conditions are: Short−Circuit Current Protection (SCP), and low−side bias Under−Voltage Lockout (UVLO).
  - – The VFO output is open drain configured. The V_{FO} signal line should be pulled to the 5 V logic power supply with approximately 4.7 kΩ resistance.
- Thermistor Bias Voltage
  - ♦ Pin: VTH
  - – This is the bias voltage pin of internal thermistor. This pin should be connected to the 5 V logic power supply.
- Series Resistor for Thermistor (Temperature Detection)
  - ♦ Pin: RTH
  - – For case temperature (T_C) detection, this pin should be connected to an external series resistor.
  - – The external series resistor should be selected to meet the detection range matched for the specification of each application (for details, refer to Figure 45).
- Positive DC−Link Pin
  - ♦ Pin: P
  - – This is the DC−link positive power supply pin of the inverter.
  - – It is internally connected to the collectors of the high−side IGBTs.

– To suppress surge voltage caused by the DC−link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (Tip: metal film capacitor is typically used).

- Negative DC−link Pins
  - ♦ Pins: NU, NV, NW
  - – These are the DC−link negative power supply pins (power ground) of the inverter.
  - – These pins are connected to the low−side IGBT emitters of the each phase.
- Inverter Power Output Pins
  - ♦ Pins: U, V, W
  - – Inverter output pins for connecting to the inverter load (e.g. motor).

Table 3. ABSOLUTE MAXIMUM RATINGS (T_J = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions		Rating	Units
INVERTER					
V_{PN}	Supply Voltage	Applied between P – NU, NV, NW		900	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P – NU, NV, NW		1000	V
V_{CES}	Collector – Emitter Voltage			1200	V
$\pm I_C$	Each IGBT Collector Current	T_C = 25°C, $T_J \le$ 150°C	FNA21012A	10	A
			FNA22512A	25	
			FNA23512A	35	
			FNA25012A	50	
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C = 25°C, $T_J \le$ 150°C, Under 1 ms Pulse Width	FNA21012A	20	A
			FNA22512A	50	
			FNA23512A	70	
			FNA25012A	75	
P_C	Collector Dissipation	T_C = 25°C per One Chip	FNA21012A	93	W
			FNA22512A	154	
			FNA23512A	171	
			FNA25012A	347	
T_J	Operating Junction Temperature (Note 2)			−40~150	°C
CONTROL PART					
V_{CC}	Control Supply Voltage	Applied between VCC(H), VCC(H) – COM		20	V
V_{BS}	High−Side Control Bias Voltage	Applied between VB(x), VS(x)		20	V
V_{IN}	Input Signal Voltage	Applied between IN(xH), IN(xL) – COM		−0.3~V_{CC}+0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between VFO – COM		−0.3~V_{CC}+0.3	V
I_{FO}	Fault Output Current	Sink Current at VFO Pin		2	mA
V_{SC}	Current Sensing Input Voltage	Applied between CSC – COM		−0.3~V_{CC}+0.3	V
BOOTSTRAP PART					
V_{RRM}	Maximum Repetitive Reverse Voltage			1200	V
I_F	Forward Current	T_C = 25°C, $T_J \le$ 150°C		1.0	A
I_{FP}	Forward Current (Peak)	T_C = 25°C, $T_J \le$ 150°C, Under 1 ms Pulse Width		2.0	A
T_J	Operating Junction Temperature			−40~150	°C

Table 3. ABSOLUTE MAXIMUM RATINGS (T_J = 25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Conditions		Rating	Units
TOTAL SYSTEM					
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short−Circuit Protection Capability)	V_{CC}, V_{BS} = 13.5~16.5 V, T_J = 50°C, Non−Repetitive, < 2 μs		800	V
T_C	Module Case Operation Temperature	See Figure 45		−40~125	°C
T_{STG}	Storage Temperature			−40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1−Minute, Connect Pins to Heat Sink		2500	V_{rms}
THERMAL RESISTANCE					
$R_{th(j-c)Q}$	Junction−to−Case Thermal Resistance	Inverter IGBT Part (per 1/6 Module)	FNA21012A	1.33	°C/W
			FNA22512A	0.81	
			FNA23512A	0.73	
			FNA25012A	0.36	
$R_{th(j-c)F}$	Junction−to−Case Thermal Resistance	Inverter FWD Part (per 1/6 Module)	FNA21012A	2.30	°C/W
			FNA22512A	1.58	
			FNA23512A	1.26	
			FNA25012A	0.66	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. The maximum junction temperature rating of the power chips integrated within the Motion SPM 2 product is 150°C.

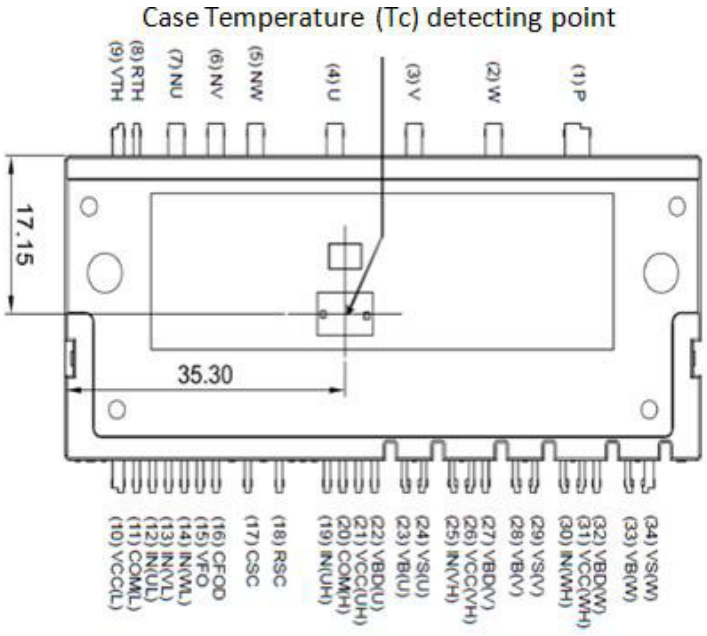


Figure 4. Case Temperature (T_C) Detecting Point

Table 4. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied between P − NU, NV, NW		400	600	800	V
V_{CC}	Control Supply Voltage	Applied between VCC(xH) − COM(H), VCC(L) − COM(L)		13.5	15.0	16.5	V
V_{BS}	High−Side Bias Voltage	Applied between VB(x) − VS(x)		13.0	15.0	18.5	V
dV_{CC}/dt, dV_{BS}/dt	Control Supply Variation			−1	−	+1	V/μs
td_{ead}	Blanking Time for Preventing Arm−Short	For Each Input Signal	FNA21012A	2.0	−	−	μs
			FNA22512A	2.0	−	−	
			FNA23512A	2.0	−	−	
			FNA25012A	2.0	−	−	
f_{PWM}	PWM Input Signal	$-40°C \le T_C \le 125°C$, $-40°C \le T_J \le 150°C$		−	−	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between NU, NV, NW − COM(H, L) (Including Surge Voltage)		−5	−	5	V
$P_{WIN(ON)}$	Minimum Input Pulse Width (Note 3)			1.5	−	−	μs
$P_{WIN(OFF)}$				1.5	−	−	
T_J	Junction Temperature			−40	−	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. This product might not make response if the input pulse width is less than the recommended value.

Table 5. ELECTRICAL CHARACTERISTICS − INVERTER PART (BASED ON FNA21012A)

(T_J = 25°C, unless otherwise specified.)

Symbol		Parameter	Conditions		Min	Typ	Max	Units
$V_{CE(SAT)}$		Collector−Emitter Saturation Voltage	V_{CC}, V_{BS} = 15 V, V_{IN} = 5 V	I_C = 10 A, T_J = 25°C	−	2.2	2.8	V
V_F		FWD Forward Voltage	V_{IN} = 0 V	I_F = 10 A, T_J = 25°C	−	2.2	2.8	V
H_S	t_{ON}	Switching Times	V_{PN} = 600 V, V_{CC} = 15 V, V_{BS} = 15 V, I_C = 10 A T_J = 25, V_{IN} = 0 V ↔ 5 V, Inductive Load (Note 4)		0.45	0.85	1.35	μs
	$t_{C(ON)}$				−	0.25	0.55	
	t_{OFF}				−	0.95	1.45	
	$t_{C(OFF)}$				−	0.10	0.40	
	t_{rr}				−	0.25	−	
L_S	t_{ON}				−	0.75	1.25	
	$t_{C(ON)}$				−	0.20	0.50	
	t_{OFF}				−	0.95	1.45	
	$t_{C(OFF)}$				−	0.10	0.40	
	t_{rr}				−	0.20	−	
I_{CES}		Collector − Emitter Leakage Current	V_{CE} = V_{CES}		−	−	5	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of the IGBT itself under the given gate driving condition internally. For the detailed information, see Figure 5 and Figure 6.

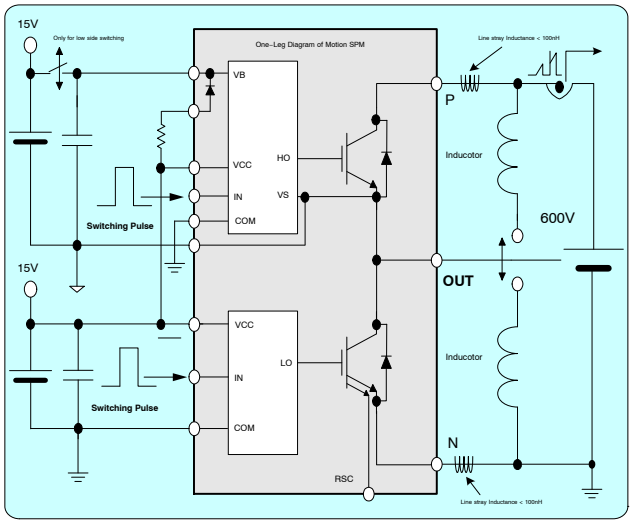


Figure 5. Switching Evaluation Circuit

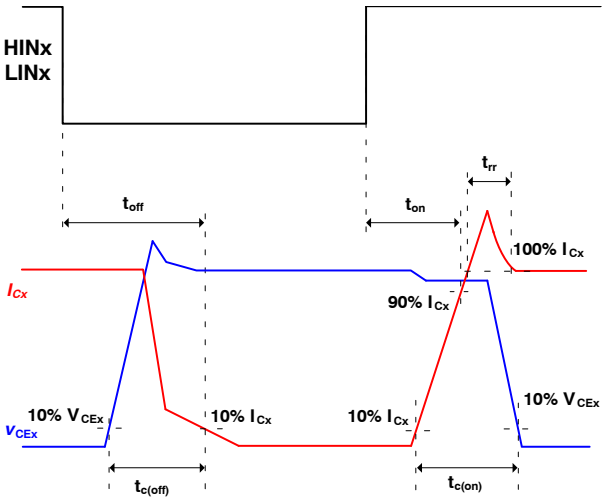


Figure 6. Switching Time Definition

Table 6. CONTROL PART

Symbol	Parameter	Conditions			Min.	Typ.	Max.	Unit
I_{QCCH}	Quiescent V_{CC} Supply Current	VCC(xH) = 15 V, IN(xH) = 0 V	VCC(xH) − COM(H)		−	−	0.15	mA
I_{QCCL}		VCC(L) = 15 V, IN(xL) = 0 V	VCC(L) − COM(L)		−	−	5.0	
I_{PCCH}	Operating High−Side V_{CC} Supply Current	VCC(xH) = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High Side	FNA21012A		−	−	0.3	mA
			FNA22512A		−	−	0.3	
			FNA23512A		−	−	0.3	
			FNA25012A		−	−	0.3	
I_{PCCL}	Operating Low−Side V_{CC} Supply Current	VCC(L) = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for Low Side	FNA21012A		−	−	8.5	mA
			FNA22512A		−	−	13.0	
			FNA23512A		−	−	15.5	
			FNA25012A		−	−	15.5	
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15 V, IN(xH) = 0 V	VB(x) − VS(x)		−	−	0.3	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{CC} = V_{BS} = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High Side	FNA21012A		−	−	4.5	mA
			FNA22512A		−	−	9.0	
			FNA23512A		−	−	12.0	
			FNA25012A		−	−	12.0	
V_{FOH}	Fault Output Voltage	V_{CC} = 15 V, V_{SC} = 0 V, V_{FO} Circuit: 4.7 kW to 5 V Pull−up			4.5	−	−	V
V_{FOL}		V_{CC} = 15 V, V_{SC} = 1 V, V_{FO} Circuit: 4.7 kW to 5 V Pull−up			−	−	0.5	
I_{SEN}	Sensing Current of Each Sense IGBT	V_{CC} = 15 V, V_{IN} = 5 V, R_{SC} = 0, No Connection of Shunt Resistor at NU, NV, NW Terminal	FNA21012A	I_C = 10 A	−	7	−	mA
			FNA22512A	I_C = 25 A	−	23	−	
			FNA23512A	I_C = 35 A	−	36	−	
			FNA25012A	I_C = 50 A	−	43	−	
$V_{SC(ref)}$	Short−Circuit Trip Level	V_{CC} = 15 V (Note 5)	CSC − COM(L)		0.43	0.50	0.57	V
I_{SC}	Short−Circuit Current Level for Trip	No Connection of Shunt Resistor at NU, V, W Terminal (Note 5)	FNA21012A	R_{SC}= 68 (±1%)	−	20	−	A
			FNA22512A	R_{SC}= 27 (±1%)	−	50	−	
			FNA23512A	R_{SC}= 16 (±1%)	−	70	−	
			FNA25012A	R_{SC}= 15 (±1%)	−	75	−	
UV_{CCD}	Supply Circuit, Under−Voltage Protection	Detection Level			10.3	−	12.8	V
UV_{CCR}		Reset Level			10.8	−	13.3	
UV_{BSD}		Detection Level			9.5	−	12.0	
UV_{BSR}		Reset Level			10.0	−	12.5	
t_{FOD}	Fault−Out Pulse Width (Note 6)	C_{FOD} = Open			50.0	−	−	μs
		C_{FOD} = 2.2 nF			1.7	−	−	ms
$V_{IN(ON)}$	ON Threshold Voltage	Applied between IN(xH)−COM(H), IN(xL)−COM(L)			−	−	2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage				0.8	−	−	
R_{TH}	Resistance of Thermistor (Note 7)	T_{TH} = 25°C			_	47.0	−	kΩ
		T_{TH} = 100°C			_	2.9	−	

5. Short−circuit current protection functions only at the low−sides because the sense current is divided from main current at the low−side IGBT. If inserting the shunt resistor for monitoring the phase current at NU, NV, NW terminal, the trip level of the short circuit current changes.
6. The fault−out pulse width t_{FOD} depends on the capacitance value of C_{FOD}.
7. T_{TH} is the thermistor temperature. To determine case temperature (T_C), experiment with the specific application.

PACKAGE

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade−off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In 1200 V Motion SPM 2, technology was developed with DBC substrate that resulted in good heat dissipation characteristics. Power chips are attached directly to the DBC substrate. This technology is applied 1200 V Motion SPM 2 achieving improved reliability and heat dissipation.

Figure 7 and Figure 8 show the package outline and the cross−sections of the Motion SPM 2 package.

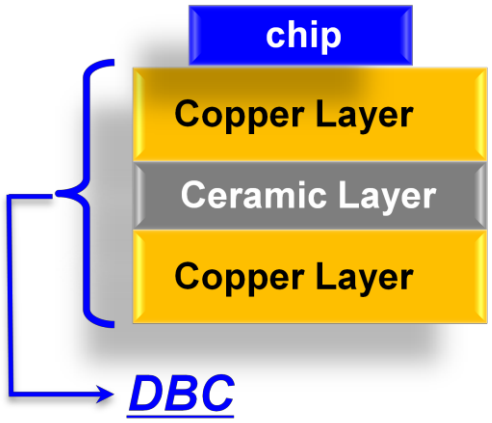


Figure 7. Vertical Structure for Heat Dissipation

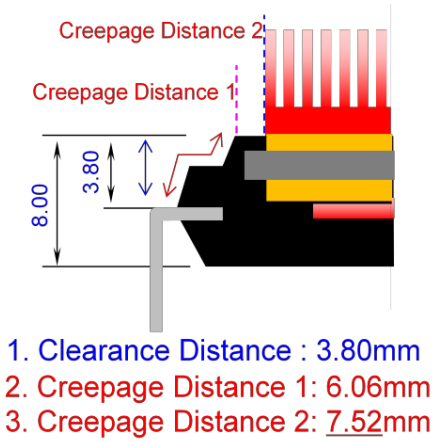


Figure 8. Distance for Isolation

Table 7. MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions		Value			Unit
			Min.	Typ.	Max.	
Device Flatness	See Figure 9		0		+200	μm
Mounting Torque	Mounting Screw: M4	Recommended 0.9 N·m	0.9	1.0	1.5	N·m
		Recommended 9.1 kg·cm	9.1	10.1	15.1	kg·cm
Terminal Pulling Strength	Load 19.6 N		10			s
Terminal Bending Strength	Load 9.8 N, 90° Bend		2			Times
Weight				50		g

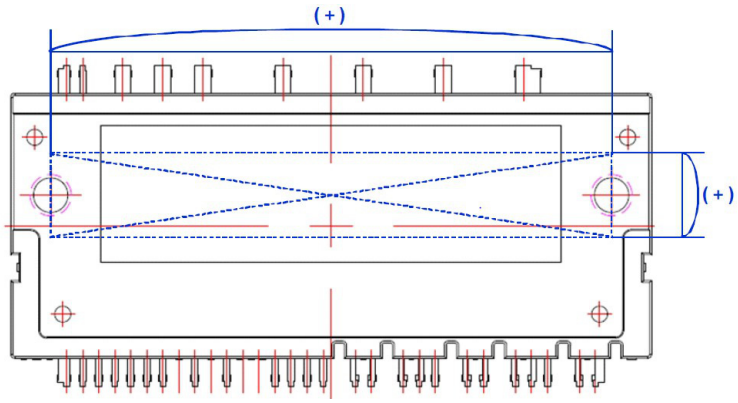


Figure 9. Flatness Measurement Position

Detailed Package Outline Drawing

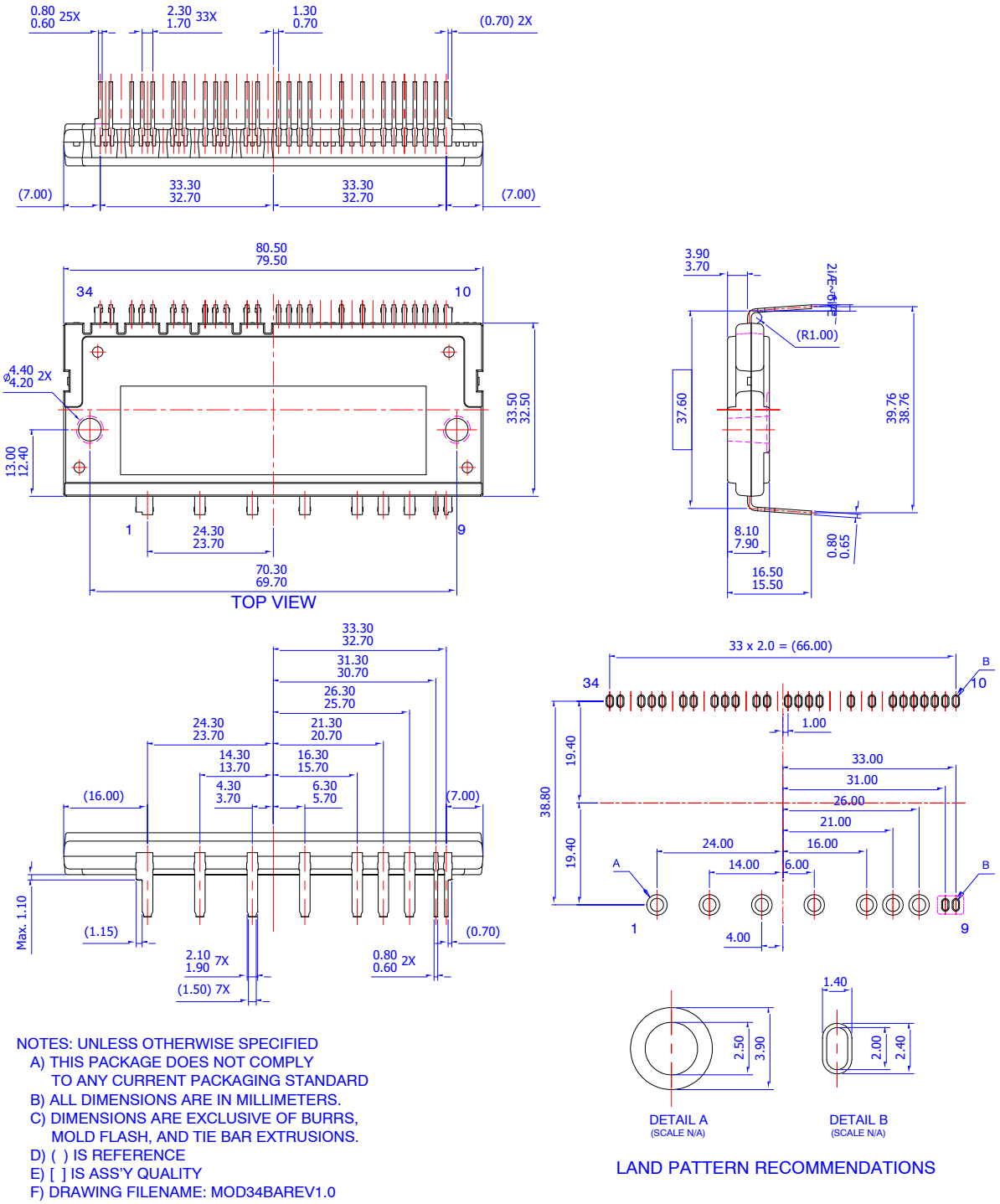


Figure 10. Package Outline Drawing

OPERATING SEQUENCE FOR PROTECTIONS

Short−Circuit Current Protection (SCP)

Motion SPM 2 uses a sense current detecting resistor (R_{SC}) for the short circuit current detection, as shown in Figure 11. LVIC has a built−in short−circuit current protection function. This protection function senses the voltage to the CSC pin. If this voltage exceeds the $V_{SC(ref)}$ (the threshold voltage trip level of the short−circuit) specified in the device datasheets (typ. $V_{SC(ref)}$ is 0.5 V), a fault signal is asserted and the all low side IGBTs are turned off. Typically, the maximum short−circuit current magnitude is gate−voltage dependent: higher gate voltage (V_{CC} & V_{BS}) results in larger short−circuit current. To avoid potential problems, the maximum short−circuit trip level is set below 1.5 times the nominal rated collector current. The LVIC short−circuit current protection−timing chart is shown in Figure 12.

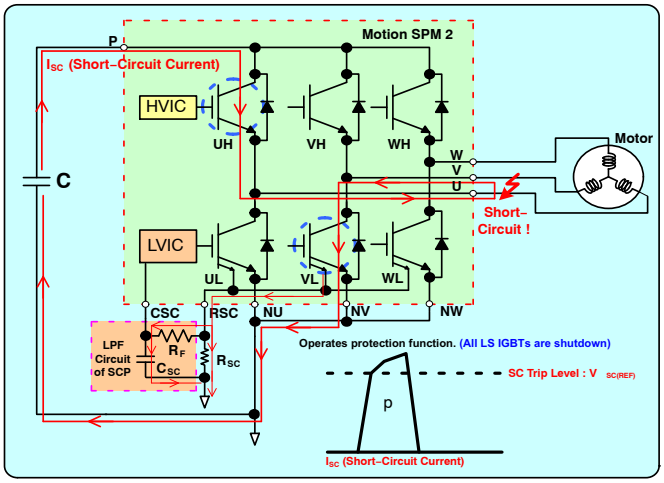
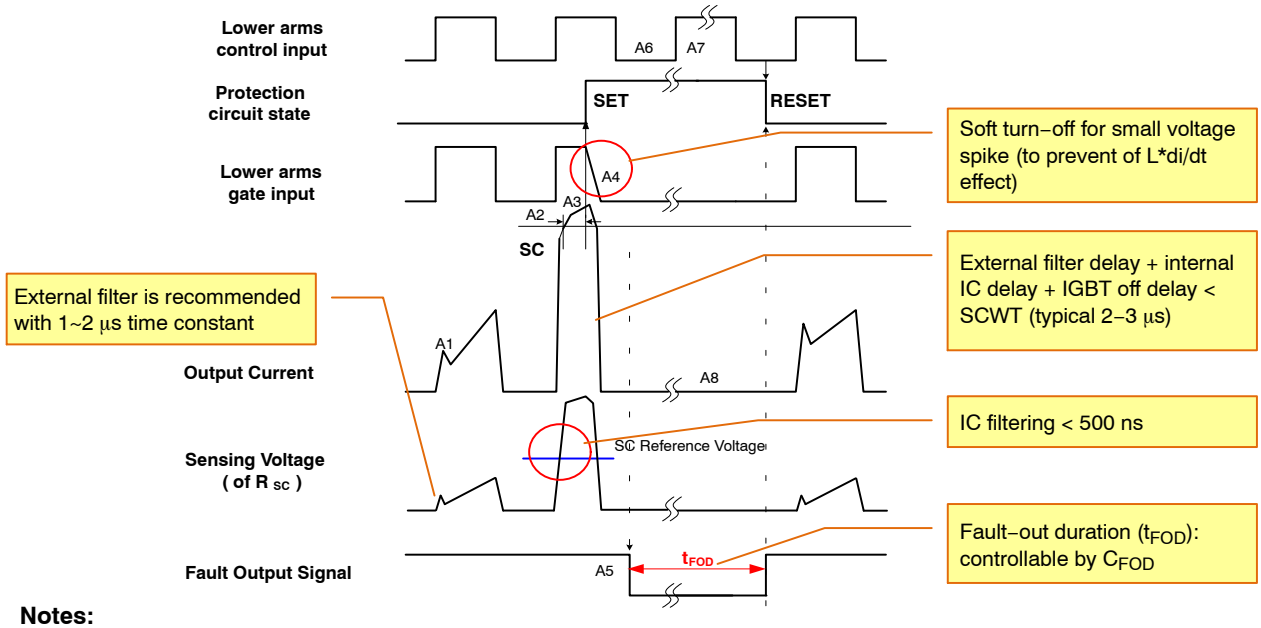


Figure 11. Operation of Short−Circuit Current Protection



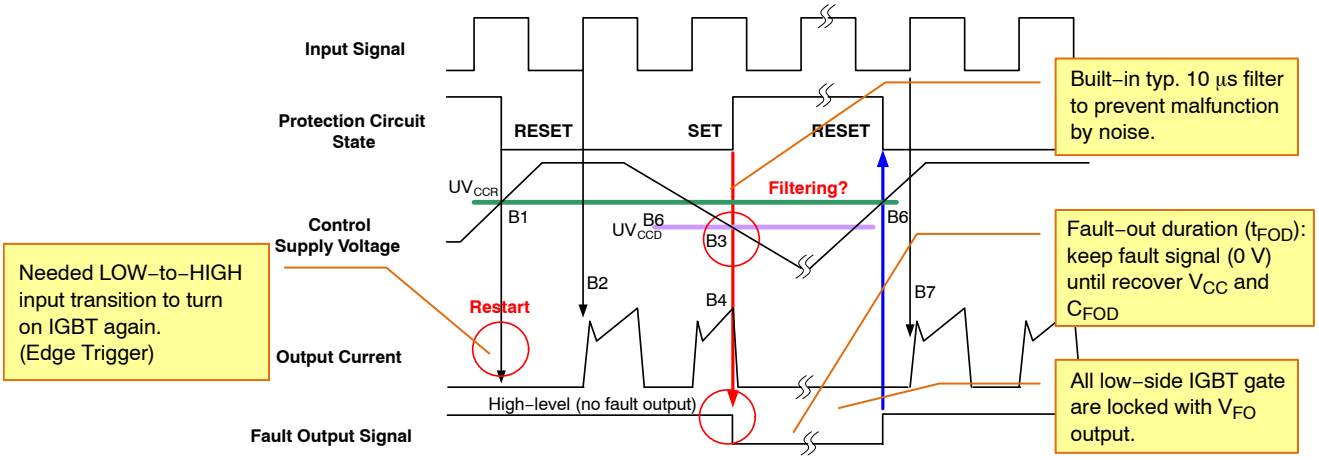
Notes:

A1-normal operation: IGBT on and carrying current.
A2-short-circuit current detection (SC trigger).
A3-hard IGBT gate interrupt.
A4-IGBT turns OFF by soft-off function.
A5-fault output timer operation start with internal delay (typ. 2.0 μs). t_{FOD}=controlled by C_{FOD}.
A6-input “L”: IGBT OFF state,
A7-input “H”: IGBT ON state. but during the active period of fault output the IGBT doesn’t turn ON.
A8-IGBT keeps OFF state.

Figure 12. Timing Chart of Short−Circuit Current Protection Function

Under−Voltage Lockout Protection

The LVIC has an under−voltage lockout protection (UVLO) function to protect the low−side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 13.

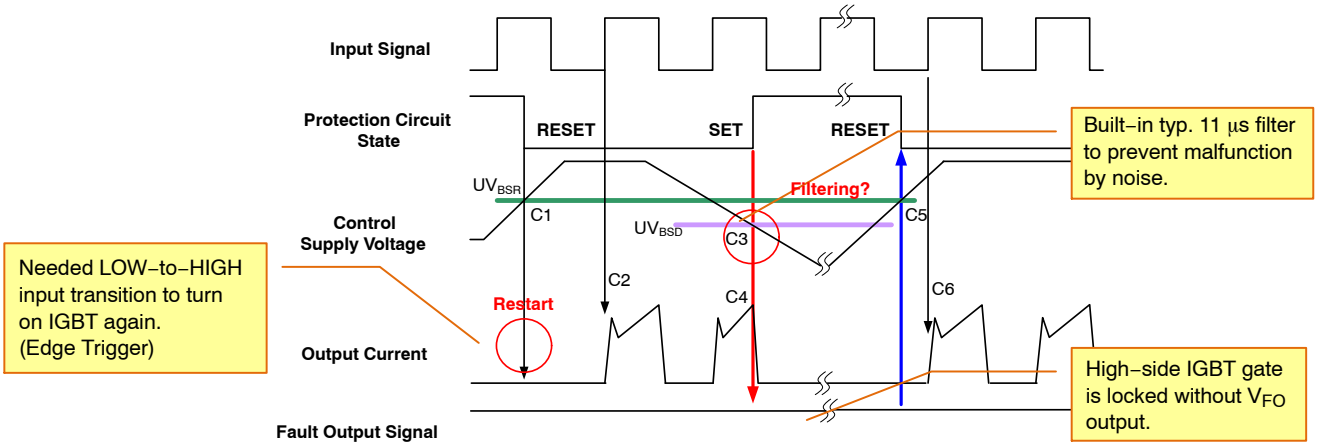


Notes:

B1-control supply voltage rise: after the voltage rises UV_{CCR}, the circuits starts to operate when the next input is applied.
B2-normal operation: IGBT ON and carrying current.
B3-under-voltage detection (UV_{CCD}).
B4-IGBT OFF in spite of control input is alive.
B5-fault output signal starts.
B6-under-voltage reset (UV_{CCR}).
B7-normal operation: IGBT ON and carrying current. If fault-out duration (t_{FOD}) by external capacitor at C_{FOD} pin is longer than UVCCR timing, fault output and IGBT state are cleared after t_{FOD}.

Figure 13. Timing Chart of Low−Side Under−Voltage Protection Function

The HVIC has an under−voltage lockout function to protect the high−side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 14. A fault−out (FO) alarm is not given for low HVIC bias conditions.



Notes:

C1-control supply voltage rises: after the voltage reaches UV_{BSR}, the circuit starts when the next input is applied.
C2-normal operation: IGBT ON and carrying current.
C3-under-voltage detection (UV_{BSD}).
C4-IGBT OFF in spite of control input is alive, but there is no fault output signal.
C5-under-voltage reset (UV_{BSR}).
C6-normal operation: IGBT ON and carrying current.

Figure 14. Timing Chart of High−Side Under−Voltage Protection Function

KEY PARAMETER DESIGN GUIDANCE

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of Motion SPM 2 series.

Selection of RSC Resistor for Protection

Figure 15 is an example circuit of the short−circuit protection using the R_{SC} resistor. Sense IGBT is employed for the low side. The designer can use the RSC pin for Over−Current Protection (OCP) and Short−Circuit Protection (SCP) without an external shunt resistor at the N−terminal. The line current on RSC is detected and the protective operation signal is passed through the RC filter. If the current exceeds the $V_{SC(ref)}$, all the gates of the N−side three IGBTs are turned off and the fault signal is transmitted from Motion SPM 2 to MCU. Since repetitive short circuit is not allowable, IGBT operation should be immediately halted when the fault signal is given.

Figure 16 shows "R_{SC} resistance vs. trip current" curve of FNA21012A under the shunt resistor = 0 Ω condition.

For current sensing, apply an external shunt resistor at each N terminal. Sensing voltage from RSC pin is influenced by an external shunt resistor, as shown in Figure 17.

Figure 16 through Figure 17 show RSC value of Motion SPM2 under one−shunt resistor condition. For adequate RSC value in a three−shunt structure, the RSC value needs to be considered by the N−terminal shunt resistor value and target protection current level.

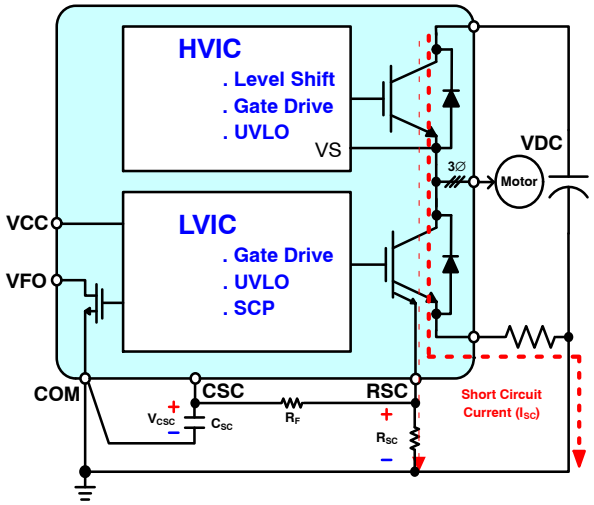


Figure 15. Current Path in Short−Circuit Condition by Leg Short Circuit

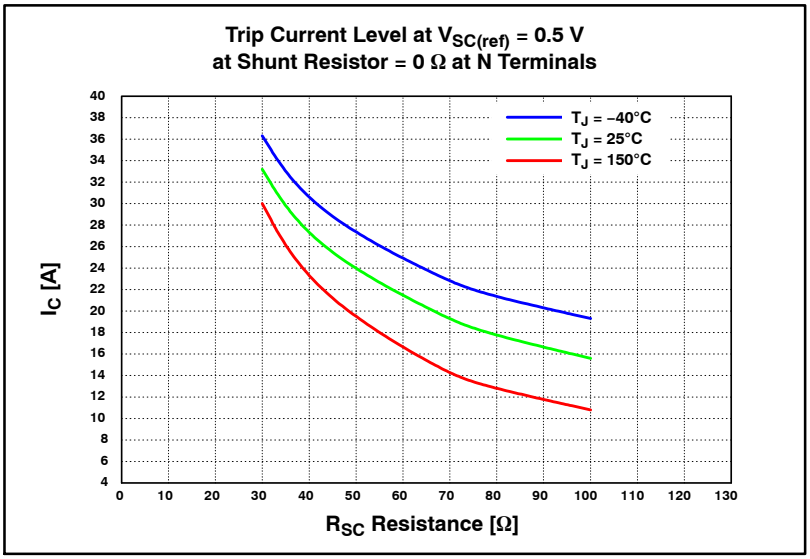
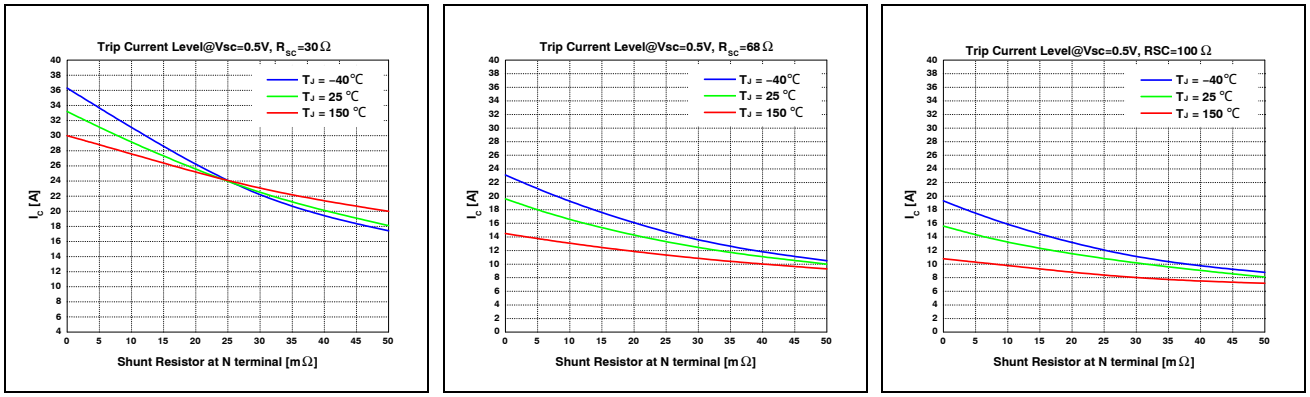


Figure 16. R_{SC} Resistance vs. Trip Current Level for Protection at Variable Junction Temperature of FNA21012A



(a) (b) (c)

Figure 17. Trip Current Level vs. Shunt Resistor of FNA21012A
(a): R_{SC} = 30 Ω, (b): R_{SC} = 68 Ω, (c): R_{SC} = 100 Ω

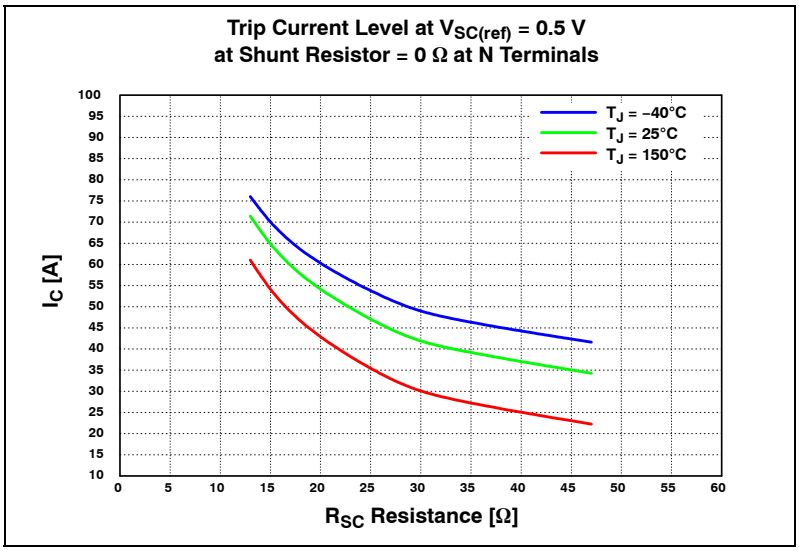
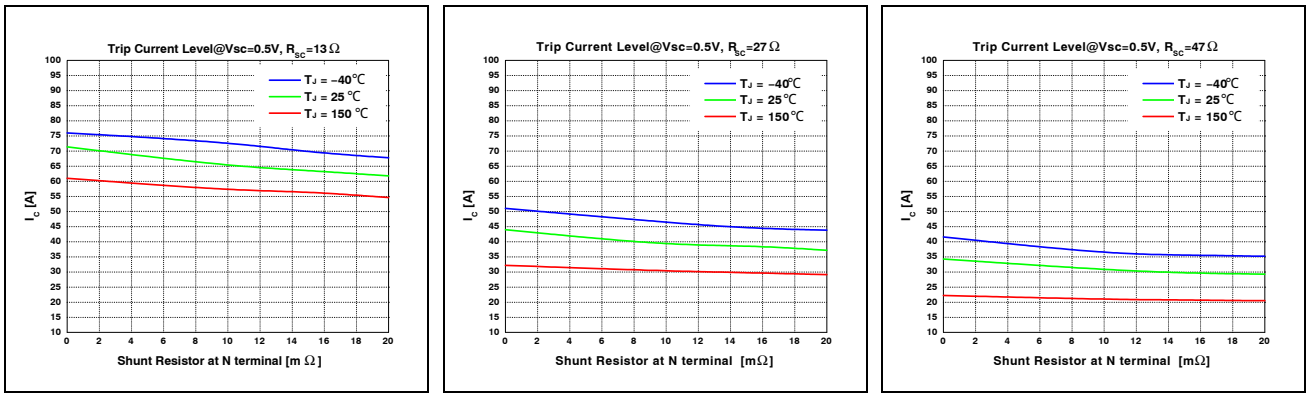


Figure 18. R_{SC} Resistance vs. Trip Current Level for Protection at Variable Junction Temperature of FNA22512A



(a) (b) (c)

Figure 19. Trip Current Level vs. Shunt Resistor of FNA22512A
(a): R_{SC} = 13 Ω, (b): R_{SC} = 27 Ω, (c): R_{SC} = 47 Ω

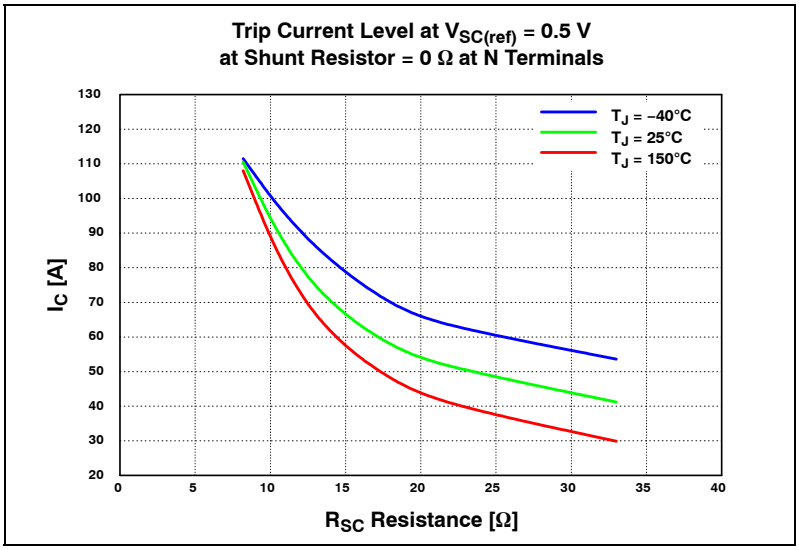
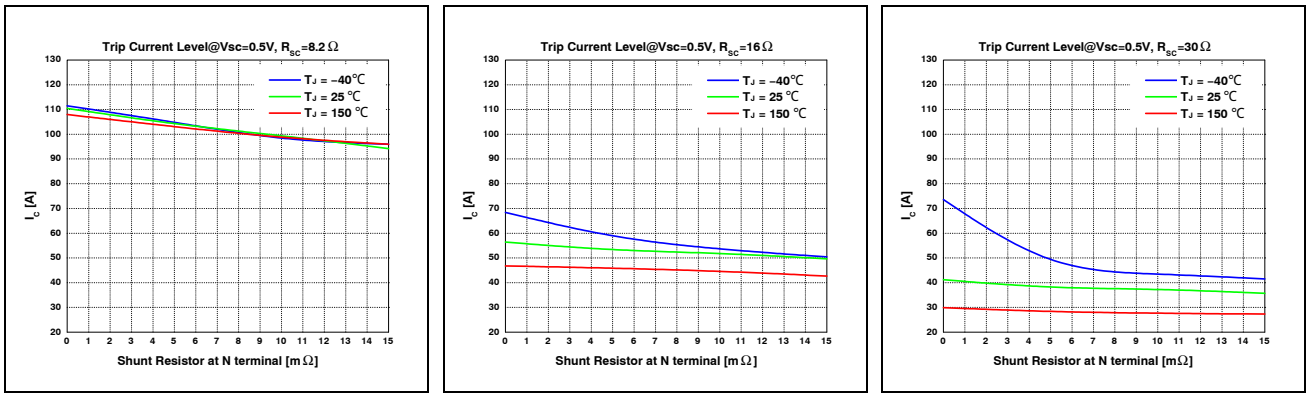


Figure 20. R_{SC} Resistance vs. Trip Current Level for Protection at Variable Junction Temperature of FNA23512A and FNA25012A



(a) (b) (c)

Figure 21. Trip Current Level vs. Shunt Resistor of FNA23512A and FNA25012A (a): R_{SC} = 8.2 Ω, (b): R_{SC} = 16 Ω, (c): R_{SC} = 30 Ω

Shunt Resistor Selection at N−Terminal for Current Sensing & Protection

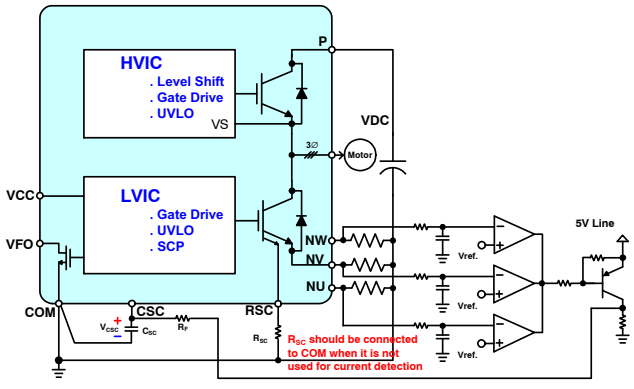


Figure 22. Recommended Circuitry for Over−Current & Short−Circuit Protection without RSC Pin Usage

If using three shunt resistors at N terminals for OCP and SCP without sense detecting from RSC, RSC should be connected to COM. The external RC time constant from the N−terminal shunt resistor to CSC must be lower than 2 μs in short circuit for stable shutdown.

The proper shunt resistance can be calculated by simple equations as below.

SC trip reference voltage (depend on datasheet):

$V_{SC(ref)}$=min. 0.43 V / typ. 0.5 V / max. 0.57 V (see Table 8)

Shunt resistance:

$I_{SC(max)} = V_{SC(max)} / R_{SHUNT(min)} \rightarrow$

$R_{SHUNT(min)} = V_{SC(max)} / I_{SC(max)}$

If the deviation of the shunt resistor is limited below ±5%:

$R_{SHUNT(typ)} = R_{SHUNT(min)} / 0.95 \rightarrow$

$R_{SHUNT(max)} = R_{SHUNT(typ)} \times 1.05$

Actual SC Trip Current level becomes:

$I_{SC(typ)} = V_{SC(typ)} / R_{SHUNT(typ)} \rightarrow$

$I_{SC(min)} = V_{SC(min)} / R_{SHUNT(max)}$

Inverter Output Power:

$P_{OUT} = \sqrt{3} \times V_{O\_LL} \times I_{RMS} \times PF$

$V_{O\_LL} = (\sqrt{3}/\sqrt{2}) \times MI \times (1/2) \times V_{DC\_Link}$

where:

V_{O_LL} = Inverter Output Lin to Line

MI = Modulation Index;

V_{DC_Link} = DC link voltage;

I_{RMS} = Maximum load current of inverter

PF = Power Factor

Average DC Current

$I_{DC\_AVG} = V_{DC\_Link} / (P_{out} \times Eff)$

where:

Eff = Inverter efficiency

The power rating of shunt resistor is calculated by the following equation:

$P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin)$ / De-rating Ratio

where:

I_{DC_AVG} = Average load current of inverter

R_{SHUNT} = Shunt resistor typical value at T_C = 25°C

De-rating Ratio = Shunt resistor at T_{SHUNT} = 100°C from datasheet of shunt resistor

Margin = Safety margin determined by customer's system

Example value of shunt resistor calculation: FNA21012A shunt resistor deviation is ±5%

Table 8. OCP & SCP LEVEL (V_{SC}(ref)) SPECIFICATION

Conditions	Min.	Typ.	Max.	Unit
Specification at T_J= 25°C, V_{CC}= 15 V	0.43	0.50	0.57	V

Shunt Resistor Calculation Examples

Calculation Conditions:

- DUT: FNA21012A
- Tolerance of shunt resistor: ±5%
- SC Trip Reference Voltage: $V_{SC(min)}$=0.43 V, $V_{SC(typ)}$=0.50 V, $V_{SC(max)}$=0.57 V
- Maximum Load Current of Inverter (I_{RMS}): 5 A_{rms}
- Maximum Peak Load Current of Inverter ($I_{C(max)}$): 10 A
- Modulation Index (MI): 0.9
- DC Link Voltage (V_{DC_Link}): 600 V
- Power Factor (PF): 0.8
- Inverter Efficiency (Eff): 0.95
- Shunt Resistor Value at T_C = 25°C (R_{SHUNT}): 40 mΩ
- De−rating Ratio of Shunt Resistor at T_{SHUNT} = 100°C: 70% (refer to Figure 23)
- Safety Margin: 20%

Calculation Results:

- $I_{SC(max)}$: $1.5 \times I_{C(max)} = 1.5 \times 10$ A = 15 A
- $R_{SHUNT(min)}$: $V_{SC(max)} / I_{SC(max)}$ = 0.57 V / 15 A = 38 mΩ
- $R_{SHUNT(typ)}$: $R_{SHUNT(min)}$ / 0.95 = 38 mΩ / 0.95 = 40 mΩ
- $R_{SHUNT(max)}$: $R_{SHUNT(typ)} \times 1.05$ = 40 mΩ x 1.05 = 42 mΩ
- $I_{SC(min)}$: $V_{SC(min)} / R_{SHUNT(max)}$ = 0.43 V / 42 mΩ = 10.2 A
- $I_{SC(typ)}$: $V_{SC(typ)} / R_{SHUNT(typ)}$ = 0.5 V / 40 mΩ = 12.5 A
- $V_{O\_LL} = (\sqrt{3}/\sqrt{2}) \times MI \times ½ \times V_{DC\_Link}$ = $= (\sqrt{3}/\sqrt{2}) \times 0.9 \times 0.5 \times 600 = 330.7$
- $P_{OUT} = \sqrt{3} \times V_{O\_LL} \times I_{RMS} \times PF$ = $= \sqrt{3} \times 330.7 \times 5 \times 0.8 = 2291$ W
- $I_{DC\_AVG} = (P_{OUT}/Eff) / V_{DC\_LINK}$ = 4.64 A
- $P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin)$ / De-rating Ratio = $(4.64 \times 0.040 \times 1.2) / 0.7 = 1.48$ W (Therefore, the proper power rating of shunt resistor is over 2 W)

Table 9. OPERATION SHORT−CIRCUIT CURRENT RANGE OF FNA21012A at T_J= 25°C

(R_{SHUNT} = 38 mΩ (Min.), 40 mΩ (Typ.), 42 mΩ (Max.)

Conditions	Min.	Typ.	Max.	Unit
Operation SC Level	10	12	15	A

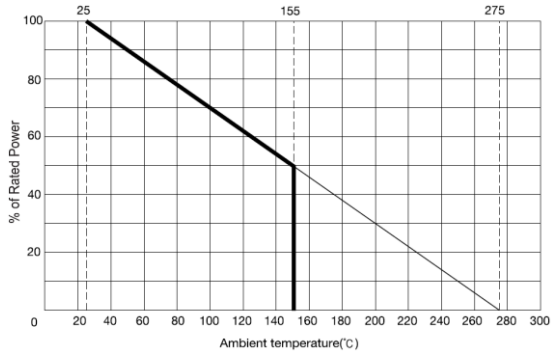
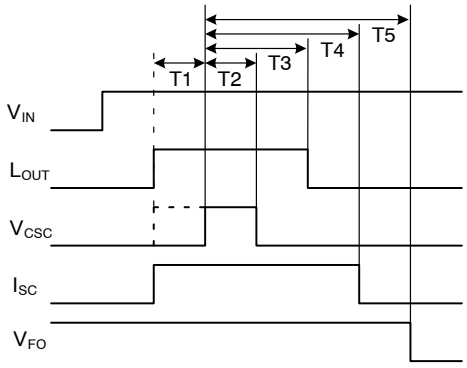


Figure 23. De−rating Curve Example of Shunt Resistor (from RARA Elec.)

Time Constant of Internal Delay

An RC filter is prevents noise−related Short−Circuit Current Protection (SCP) circuit malfunction. The RC time constant is determined by the applied noise time and the Short−Circuit Current Withstanding Time (SCWT) of Motion SPM 2. When the R_{SC} voltage exceeds the SCP level, this is applied to the CSC pin via the RC filter. The RC filter delay (T1) is the time required for the CSC pin voltage to rise to the referenced SCP level. The LVIC has an internal filter time (logic filter time for noise elimination: T2).

Consider this filter time when designing the RC filter of V_{CSC}.



Notes:
V_{IN}: Voltage of input signal.
L_{OUT}: V_{GE} of low−side IGBT.
V_{CSC}: Voltage of CSC pin.
I_{SC}: Short−circuit current.
V_{FO}: Voltage of VFO pin.
T1: filtering time of RC filter of V_{CSC}.
T2: filtering time of CSC. If V_{CSC} width is less than T2, SCP does not operate.
T3: delay from CSC triggering to gate−voltage down.
T4: delay from CSC triggering to short−circuit current.
T5: delay from CSC triggering to fault−out signal.

Figure 24. Timing Diagram

Table 10. TIME TABLE ON SHORT−CIRCUIT CONDITIONS: V_{CSC} to L_{OUT}, I_{SC}, V_{FO} (Notes 8 and 9)

Device Under Test	Typ. at T_J=25°C	Typ. at T_J=150°C	Max. at T_J=25°C
FNA21012A	T2 = 0.25 μs	T2 = 0.09 μs	Considering ±20% Deviation, T4 = 3.6 μs
	T3 = 0.62 μs	T3 = 0.57 μs	
	T4 = 3 μs	T4 = 3.3 μs	
	T5 = 4.1 μs	T5 = 4.25 μs	

8. To guarantee safe short−circuit protection under all operating conditions, C_{SC} should be triggered within 1.0 μs after short−circuit occurs. (Recommendation: SCWT < 5.0 μs, Conditions: V_{DC} = 800 V, V_{CC} = 16.5 V, T_J = 150°C).
9. It is recommended that delay from short−circuit to CSC triggering should be minimized.

Soft Turn−Off

An LVIC soft turn−off function protects the low side IGBTs from over voltage of V_{PN} (supply voltage) by "short−circuit hard off," which is when IGBTs are turned off by short input signal before the SCP function under short−circuit condition. In this case, V_{PN} rapidly rises by fast and big di/dt of I_{SC} (short−circuit current). This kind of rapid rise of V_{PN} can cause destruction of IGBT by over−voltage. Therefore, soft−off function prevents IGBT rapid turning off by slow discharging of V_{GE} (gate−to−emitter voltage of IGBT).

An internal block diagram of LVIC and operation sequence of soft turn−off function is shown in Figure 25 and Figure 26. This function operates by two internal protection functions (UVLO and SCP). When the IGBT is turned off in normal conditions, LVIC turns off the IGBT immediately by turn−off gate signal ($IN_{(xL)}$) via gate driver block. Pre−driver turns on output buffer of gate driver block (path **1**). When the IGBT is turned off by a protection function, the gate driver is disabled by the protection function signal via output of protection circuit (disable output buffer, high−Z) and output of the protection circuit turn−on switch of the soft−off function. V_{GE} (IGBT gate−emitter voltage) is discharged slowly via circuit of soft−off (path **2**).

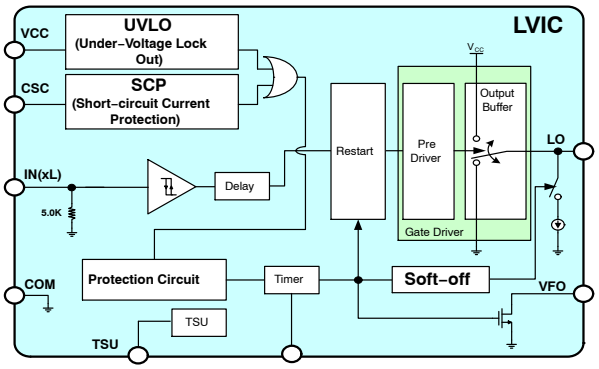


Figure 25. Internal Block Diagram of LVIC

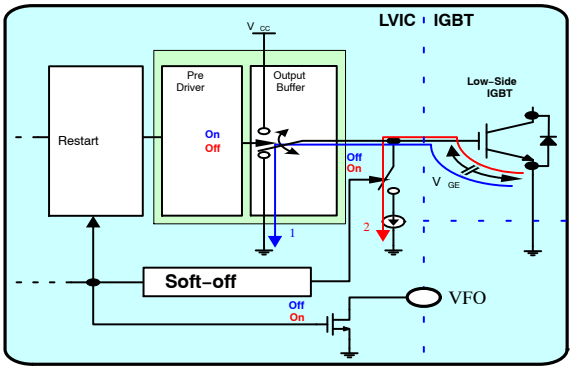


Figure 26. Operating Sequence of Soft Turn−Off

Figure 27 and Figure 28 show normal turn−off switching operations performed satisfactorily at a V_{DC}=800 V with the surge voltage between the P and N pins ($V_{PN(Surge)}$) limited to under 1000 V. The difference between the hard and soft turn−off switching operation is also shown in Figure 27 and Figure 28. The hard turn−off of the IGBT creates a large overshoot (155 V). The DC−link capacitor supply voltage should be limited to 800 V to safely protect the 1200 V Motion SPM 2. A hard turn−off, with a duration of less than ~2 μs, may occur in the case of a short−circuit fault. For a normal short−circuit fault, the protection circuit becomes active and the IGBT is turned off softly to prevent excessive

overshoot voltage. An overshoot voltage of <100 V occurs in this condition.

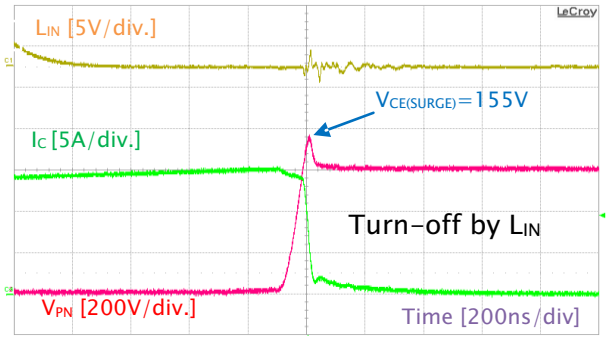


Figure 27. Turn−Off by Input (FNA21012A, Ref. Condition: V_{DC} = 600 V, T_J = 25°C)

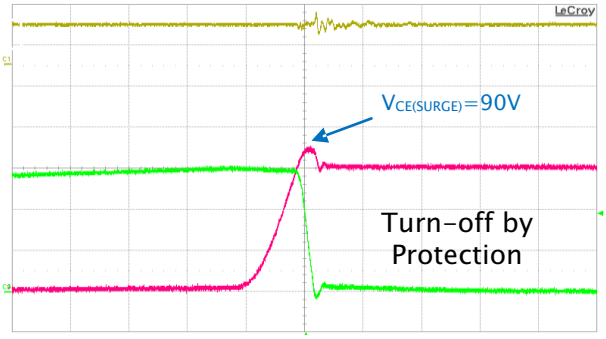


Figure 28. Turn−Off by Soft Off Function (FNA21012A, Ref. Condition: V_{DC} = 600 V, T_J = 25°C)

Fault Output Circuit

Table 11. FAULT−OUTPUT MAXIMUM RATINGS

Symbol	Item	Condition	Rating	Unit
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} − COM	−0.3 ~ V_{CC}+0.3	V
I_{FO}	Fault Output Current	Sink Current at VFO Pin	2	mA

Table 12. ELECTRICAL CHARACTERISTICS

Symbol	Item	Condition	Min.	Max.	Unit
V_{FOH}	Fault Output Supply Voltage	V_{CC} = 15 V, V_{SC} = 0, V_{FO} Circuit: 4.7 kΩ to 5 V Pull−Up	4.5	−	V
V_{FOL}			−	0.5	V

Because V_{FO} terminal is an open−drain type; it should be pulled up via a pull−up resistor. The resistor must satisfy the above specifications.

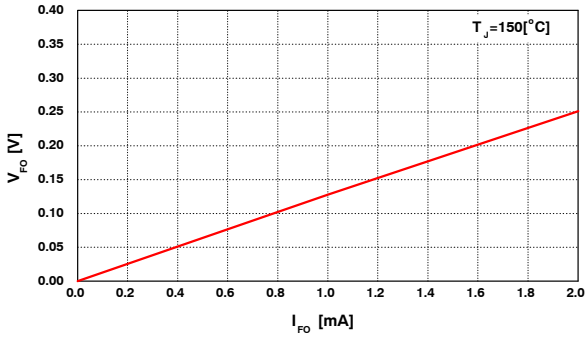


Figure 29. Voltage−Current Characteristics of V_{FO} Terminal

Circuit of Input Signal (IN(xH), IN(xL))

Figure 30 shows the I/O interface circuit between the MCU and Motion SPM 2. Because the Motion SPM 2 input logic is an active HIGH and there are built−in pull−down resistors, external pull−down resistors are not needed.

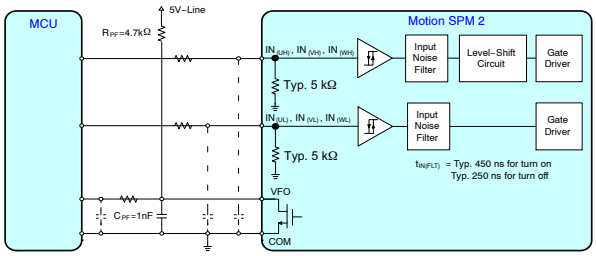


Figure 30. Recommended CPU I/O Interface Circuit

The input and fault output maximum rated voltages are shown in Table 11. Since the fault output is open drain, its rating is V_{CC}+0.3 V, 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the decoupling capacitors be placed at both the MCU and Motion SPM 2 ends of the V_{FO} signal line, as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 46) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the Motion SPM 2 series integrates a 5 kΩ (typical) pull−down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM 2 input, attention should be given to the signal voltage drop at the Motion SPM 2 input terminals to satisfy the turn−on threshold voltage requirement.

Table 13. MAXIMUM RATINGS OF INPUT AND VFO PINS

Symbol	Item	Condition	Rating	Unit
V_{IN}	Input Signal Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$−COM(x)	−0.3 ~ V_{CC}+0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} − COM(L)	−0.3 ~ V_{CC}+0.3	V

Table 14. INPUT THRESHOLD VOLTAGE RATINGS (V_{CC} = 15 V, T_J = 25°C)

Symbol	Item	Condition	Min.	Max.	Unit
$V_{IN(ON)}$	Turn−On Threshold Voltage	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$−COM(H)	−	2.6	V
$V_{IN(OFF)}$	Turn−Off Threshold Voltage	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$−COM(L)	0.8	−	V

Bootstrap Circuit Design

Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between VB (U, V, W) and VS (U, V, W), provides the supply to the HVIC within the Motion SPM 2 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high−side IGBT. The under−voltage lockout protection for V_{BS} ensures that the HVIC does not drive the high−side IGBT if the V_{BS} voltage drops below a specific voltage *(refer to the datasheet)*. This function prevents the IGBT from operating in a high−dissipation mode.

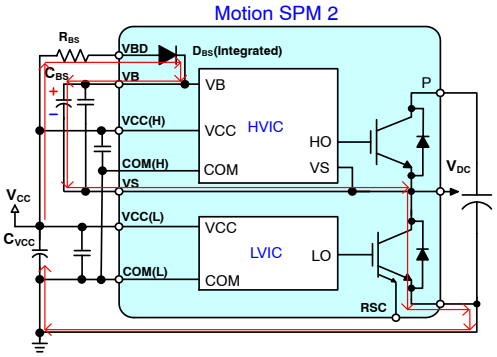


Figure 31. Current Path of Bootstrap Circuit for the Supply Voltage (V_{BS}) of a HVIC when Low−Side IGBT Turns On

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 31). This method has the advantage of being simple and inexpensive. However, the duty cycle and on−time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of a bootstrap diode, resistor, and capacitor. The current flow path of the bootstrap circuit is shown in Figure 31. When Vs is pulled down to ground (low−side IGBT turn−on or low−side FRD freewheeling), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{CC} supply.

Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on−time of the low−side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\Delta} \times \ln \frac{V_{CC}}{V_{CC} - V_{BS(min)} - V_F - V_{LS}} \quad \text{(eq. 1)}$$

where:

V_F = Forward voltage drop across the bootstrap diode

$V_{BS(min)}$ = The minimum value of the bootstrap capacitor

V_{LS} = Voltage drop across the low−side IGBT or load

Δ = Duty ratio of PWM

When the bootstrap capacitor is charged initially; V_{CC} drop voltage is generated based on initial charging method, V_{CC} line SMPS output current, V_{CC} source capacitance, and bootstrap capacitance. If V_{CC} drop voltage reaches UV_{CCD} level, the low side is shutdown and a fault signal is activated. To avoid this malfunction, related parameter and initial charging method should be considered. To reduce V_{CC} voltage drop at initial charging, a large V_{CC} source capacitor and selection of optimized low−side turn−on method are recommended. Adequate on−time duration of the low−side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts.

Figure 33 shows shows an example of initial bootstrap charging sequence. Once V_{CC} establishes, V_{BS} needs to be charged by turning on the low−side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency. Therefore, it is desired to maintain this structure without creating complementary high−side PWM signals. The capacitance of V_{CC} should be sufficient to supply necessary charge to V_{BS} capacitance in all three phases. If a normal PWM operation starts before V_{BS} reaches V_{UVLO} reset level, the high−side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over−current protection level. Therefore, initial charging time for bootstrap capacitors should be separated, as shown in Figure 33. The effect of the bootstrap capacitance factor and charging method (low−side IGBT driving method) is shown in Figure 34.

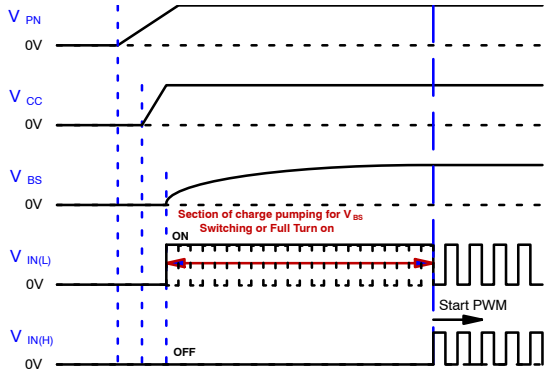


Figure 32. Timing Chart of Initial Bootstrap Charging

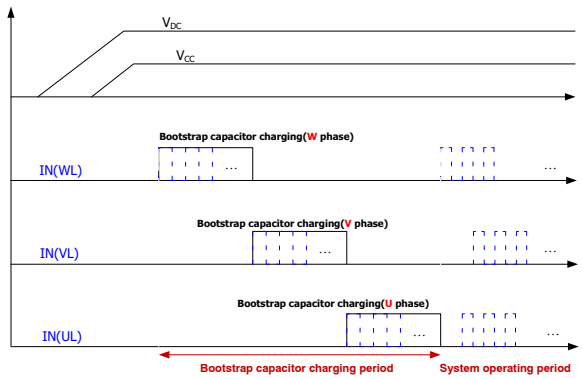


Figure 33. Recommended Initial Bootstrap Capacitors Charging Sequence

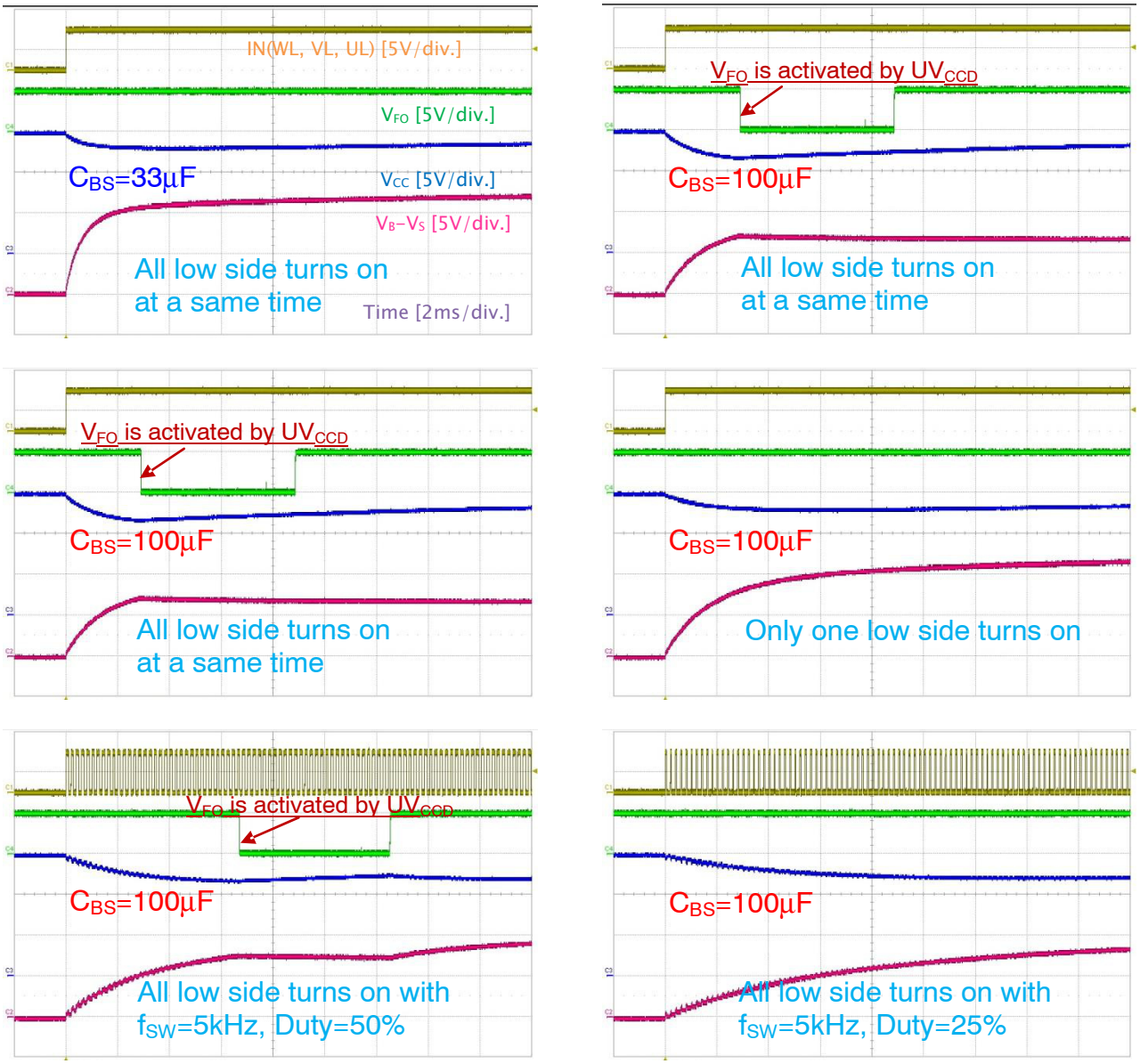


Figure 34. Initial Charging According to Bootstrap Capacitance and Charging Method (Ref. Condition: V_{CC} = 15 V / 300 mA, V_{CC} Capacitor = 220 µF, Bootstrap Capacitor = 100 µF, R_{BS} = 20 Ω)

Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} \quad \text{(eq. 2)}$$

where:

Δt = maximum on pulse width of high−side IGBT

ΔV_{BS} = the allowable discharge voltage of the C_{BS} (voltage ripple)

I_{Leak} = maximum discharge current of the C_{BS}

Mainly via the following mechanisms:

- Gate charge for turning the high−side IGBT on
- Quiescent current to the high−side circuit in HVIC
- Level−shift charge required by level−shifters in HVIC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non−electrolytic capacitors)
- Bootstrap diode reverse recovery charge

Practically, 4.5 mA of I_{Leak} is recommended for the Motion SPM 2 family. By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The C_{BS} is only charged when the high−side IGBT is off and the $V_{S(x)}$ voltage is pulled down to ground.

The on−time of the low−side IGBT must be sufficient to for the charge drawn from the C_{BS} capacitor to be fully replenished. This creates an inherent minimum on−time of the low−side IGBT (or off−time of the high−side IGBT).

Calculation Examples of Bootstrap Capacitance A

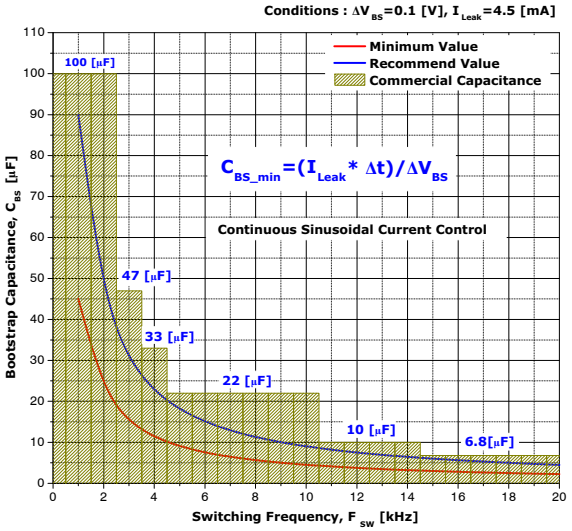


Figure 35. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔV_{BS}

- I_{Leak} = circuit current = 4.5 mA (for FNA21012A, refer to Figure 27)
- ΔV_{BS} = discharged voltage = 0.1 V (recommended value)
- Δt = maximum on pulse width of high−side IGBT = 0.2 ms (depends on application)

$$C_{BS\_min} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} = \frac{4.5\ mA \times 0.2\ ms}{0.1\ V} = 19 \times 10^{-6} \quad \text{(eq. 3)}$$

→ More than 2 times → 18 μF (22 μF STD value)

Table 15. OPERATING VBS SUPPLY CURRENT

Symbol	Conditions	Device	Max.	Unit
IPBS	V_{CC} = V_{BS} = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for High−Side	FNA21012A	4.5	mA
		FNA22512A	9.0	
		FNA23512A	12.0	

10. The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended V_{BS} voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

Calculation Examples of Bootstrap Capacitance B

Based on operating conditions, UV_{BS} function, and allowable recommended $V_{B(x)}$−$V_{S(x)}$.

To avoid unexpected under−voltage protection and to keep V_{BS} within recommended value, bootstrap capacitance should be selected based on the operating conditions. Bootstrap voltage ripple is influenced by bootstrap resistor, load condition, output frequency, and switching frequency. Check the bootstrap voltage under the maximum load condition in the system. Figure 36 shows example of $V_{B(x)}$−$V_{S(x)}$ ripple voltage during operation.

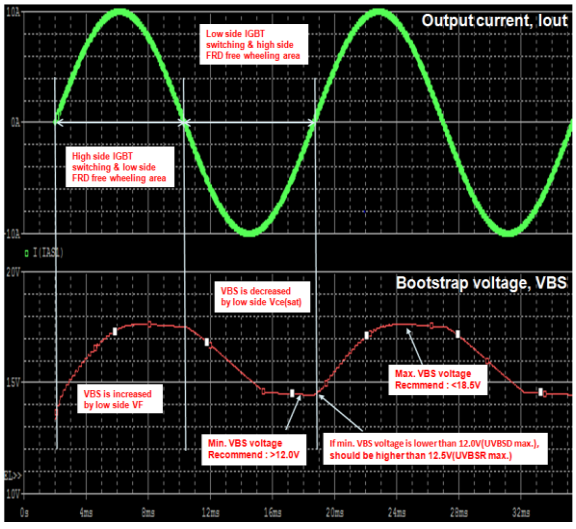


Figure 36. Recommendation of Bootstrap Ripple Voltage during Operation

Built−in Bootstrap Diode

When the high−side IGBT or FRD conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. A withstand voltage of more than 1200 V is recommended for the bootstrap diode. It is important that this diode should be fast recovery (recovery time < 100 ns) to minimize the amount of charge fed back from the bootstrap capacitor into the V_{CC} supply. Normally, bootstrap circuit consists of bootstrap diode (D_{BS}), bootstrap resistor (R_{BS}), and bootstrap capacitor (C_{BS}). I−V characteristics of Motion SPM 2 bootstrap diode are shown in Figure 37 and Figure 38. The bootstrap resistor (R_{BS}) slows down the dV_{BS}/dt and limits initial charging current (I_{charge}) of bootstrap capacitor. To prevent large inrush current at initial bootstrap capacitor charging, an additional series resistor should be used for current limitation. Large inrush current can result in over−current protection and stress of bootstrap diode. Guaranteed pulse current of bootstrap diode is limited by 2 A; therefore, minimum 10 Ω series resistor should be used for the current limitation. Generally, tens of Ω is recommended as R_{BS}. For the selection of R_{BS}, pulse power rating should be considered for initial charging of bootstrap capacitor. To use a large bootstrap capacitor, high pulse power rating is required for the bootstrap resistor. An example of resistor pulse power rating is shown in Figure 39.

The characteristics of Motion SPM 2 bootstrap diode are:

- Fast recovery diode = 1200 V / 1 A
- t_{rr} = 80 ns (typical)

Table 16. SPECIFICATION FOR BOOTSTRAP DIODE

Symbol	Parameter	Conditions	Typ.	Unit
V_F	Forward−Drop Voltage	I_F = 1 A, T_C = 25°C	2.2	V
t_{rr}	Reverse−Recovery Time	I_F = 1 A, T_C = 25°C, dI_F/dt = 50 A/μs	80	ns

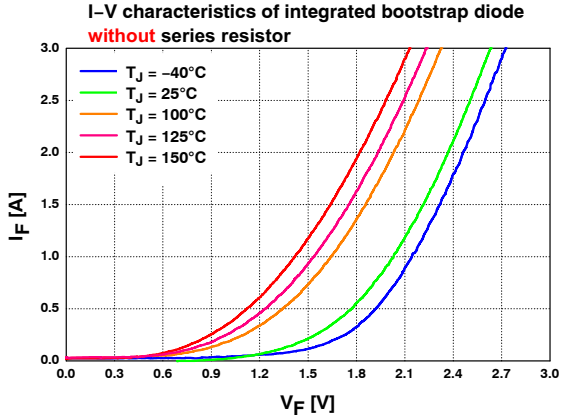


Figure 37. I−V Characteristics of Integrated Bootstrap Diode Series without Series Resistor

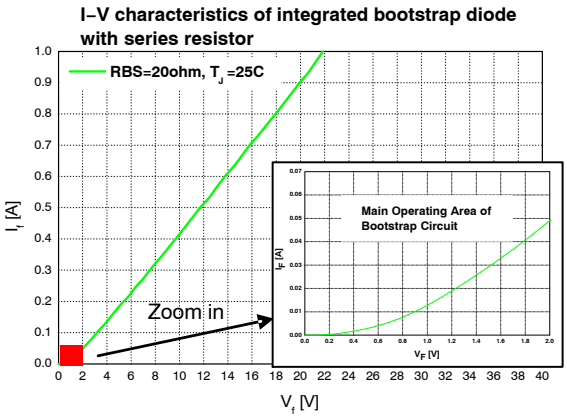


Figure 38. I−V Characteristics of Integrated Bootstrap Diode Series with Series Resistor

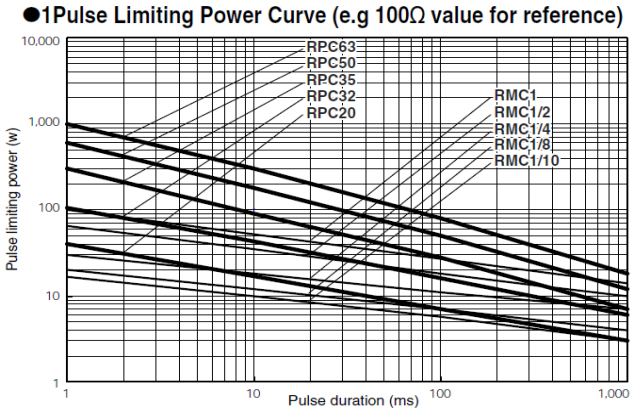


Figure 39. Example of Pulse Power Curve of Resistor

Circuit of NTC Thermistor (Temperature Monitoring of Module)

Motion SPM 2 series include a Negative Temperature Coefficient (NTC) thermistor for temperature sensing inside the module. This thermistor is located in the DBC substrate with the power chip (IGBT/FRD) and accurately reports the temperature of the power chip (see Figure 41). Normally, circuit designers use two kinds of circuit for temperature protection (monitoring) by NTC thermistor. One is circuit by Analog−Digital Converter (ADC). The other is circuit by comparator. Figure 43 and Figure 44 show examples of both circuits for NTC thermistor.

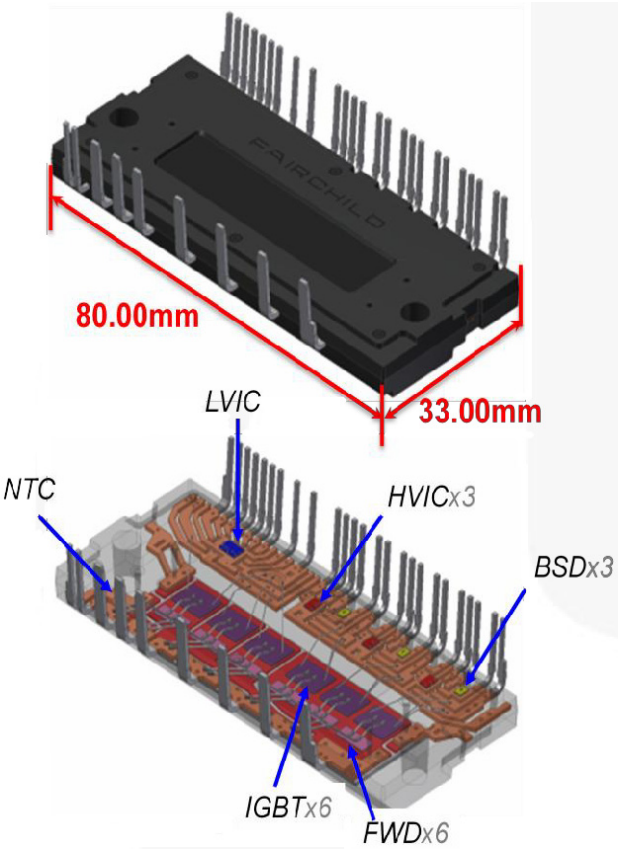


Figure 40. 1200 V Motion SPM 2 Series

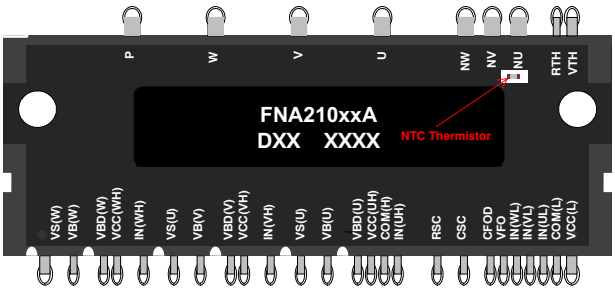


Figure 41. Location of NTC Thermistor in 1200 V Motion SPM 2

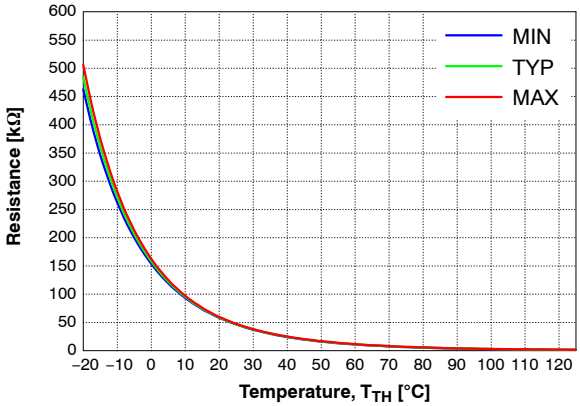


Figure 42. R−T Curve of NTC Thermistor

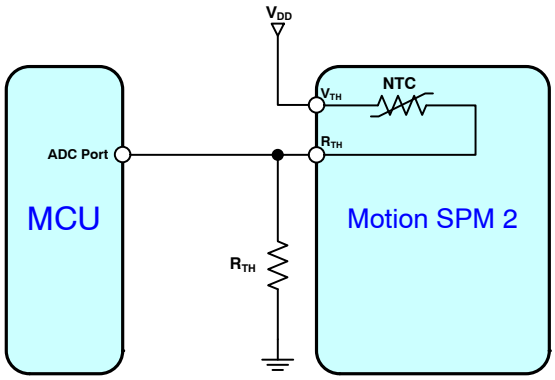


Figure 43. OT Protection Circuit by MCU

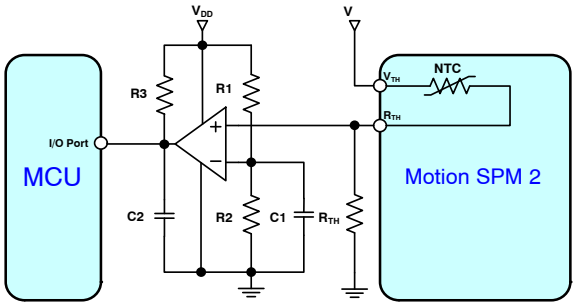


Figure 44. OT Protection Circuit by Comparator

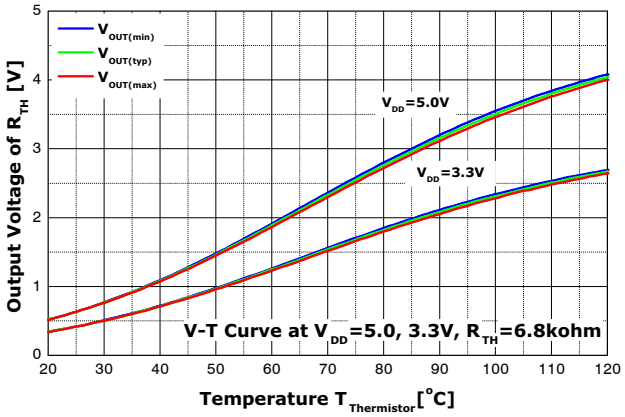


Figure 45. V−T Curve of Figure 43

Table 17. R−T TABLE OF NTC THERMISTOR

T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)
0	153.8063	158.2144	162.7327	61	10.4594	10.8007	11.1520
1	146.0956	150.1651	154.3326	62	10.0746	10.4091	10.7536
2	138.8168	142.5725	146.4152	63	9.7058	10.0336	10.3714
3	131.9431	135.4081	138.9502	64	9.3522	9.6734	10.0046
4	125.4497	128.6453	131.9091	65	9.0133	9.3279	9.6525
5	119.3135	122.2594	125.2655	66	8.6882	8.9963	9.3145
6	113.5129	116.2273	118.9947	67	8.3764	8.6782	8.9899
7	108.0276	110.5275	113.0739	68	8.0773	8.3727	8.6782
8	102.8388	105.1398	107.4814	69	7.7902	8.0795	8.3787
9	97.9288	100.0454	102.1974	70	7.5147	7.7979	8.0910
10	93.2812	95.2267	97.2031	71	7.2496	7.5268	7.8138
11	88.8803	90.6673	92.4810	72	6.9950	7.2663	7.5474
12	84.7119	86.3519	88.0148	73	6.7505	7.0160	7.2913
13	80.7624	82.2661	83.7894	74	6.5157	6.7755	7.0450
14	77.0190	78.3963	79.7903	75	6.2901	6.5443	6.8082
15	73.4700	74.7302	76.0043	76	6.0739	6.3227	6.5810
16	70.1042	71.2558	72.4189	77	5.8662	6.1096	6.3624
17	66.9112	67.9620	69.0224	78	5.6665	5.9046	6.1521
18	63.8812	64.8386	65.8039	79	5.4745	5.7075	5.9498
19	61.0050	61.8759	62.7530	80	5.2899	5.5178	5.7549
20	58.2739	59.0647	59.8601	81	5.1129	5.3358	5.5680
21	55.6798	56.3961	57.1160	82	4.9426	5.1607	5.3879
22	53.2152	53.8628	54.5127	83	4.7788	4.9921	5.2145
23	50.8732	51.4569	52.0422	84	4.6211	4.8299	5.0475
24	48.6469	49.1715	49.6969	85	4.4694	4.6736	4.8866
25	46.5300	47.0000	47.4700	86	4.3228	4.5226	4.7310
26	44.4567	44.9360	45.4159	87	4.1817	4.3771	4.5811
27	42.4868	42.9737	43.4618	88	4.0459	4.2369	4.4366
28	40.6147	41.1075	41.6021	89	3.9150	4.1019	4.2973
29	38.8351	39.3323	39.8319	90	3.7890	3.9717	4.1629
30	37.1428	37.6431	38.1463	91	3.6675	3.8463	4.0334
31	35.5329	36.0351	36.5408	92	3.5505	3.7253	3.9084
32	34.0011	34.5041	35.0111	93	3.4377	3.6087	3.7879
33	32.5433	33.0462	33.5534	94	3.3290	3.4963	3.6716
34	31.1555	31.6573	32.1640	95	3.2242	3.3878	3.5593
35	29.8340	30.3339	30.8392	96	3.1235	3.2836	3.4515
36	28.5760	29.0734	29.5764	97	3.0264	3.1830	3.3473
37	27.3776	27.8717	28.3720	98	2.9328	3.0860	3.2468
38	26.2356	26.7260	27.2228	99	2.8425	2.9923	3.1497
39	25.1472	25.6332	26.1261	100	2.7553	2.9019	3.0559
40	24.1094	24.5907	25.0792	101	2.6712	2.8146	2.9654
41	23.1198	23.5960	24.0796	102	2.5901	2.7303	2.8779

Table 17. R−T TABLE OF NTC THERMISTOR (continued)

T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)
42	22.1759	22.6466	23.1249	103	2.5117	2.6489	2.7933
43	21.2753	21.7401	22.2129	104	2.4360	2.5703	2.7117
44	20.4158	20.8746	21.3416	105	2.3630	2.4943	2.6327
45	19.5953	20.0478	20.5088	106	2.2921	2.4206	2.5560
46	18.8120	19.2580	19.7126	107	2.2236	2.3493	2.4819
47	18.0638	18.5032	18.9514	108	2.1575	2.2805	2.4102
48	17.3492	17.7818	18.2234	109	2.0936	2.2139	2.3409
49	16.6663	17.0921	17.5269	110	2.0319	2.1496	2.2739
50	16.0137	16.4325	16.8605	111	1.9725	2.0877	2.2094
51	15.3899	15.8016	16.2227	112	1.9151	2.0278	2.1470
52	14.7934	15.1981	15.6122	113	1.8596	1.9699	2.0866
53	14.2230	14.6205	15.0277	114	1.8060	1.9139	2.0282
54	13.6773	14.0677	14.4678	115	1.7541	1.8598	1.9716
55	13.1552	13.5385	13.9316	116	1.7042	1.8076	1.9171
56	12.6556	13.0318	13.4178	117	1.6559	1.7572	1.8644
57	12.1774	12.5465	12.9255	118	1.6092	1.7083	1.8134
58	11.7195	12.0815	12.4536	119	1.564	1.6611	1.7639
59	11.2810	11.6361	12.0011	120	1.5203	1.6153	1.7161
60	10.8610	11.2091	11.5673				

PRINT CIRCUIT BOARD (PCB) DESIGN

General Application Circuit Example

Figure 46 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. Figure 47 shows guidance of PCB layout for Motion SPM 2.

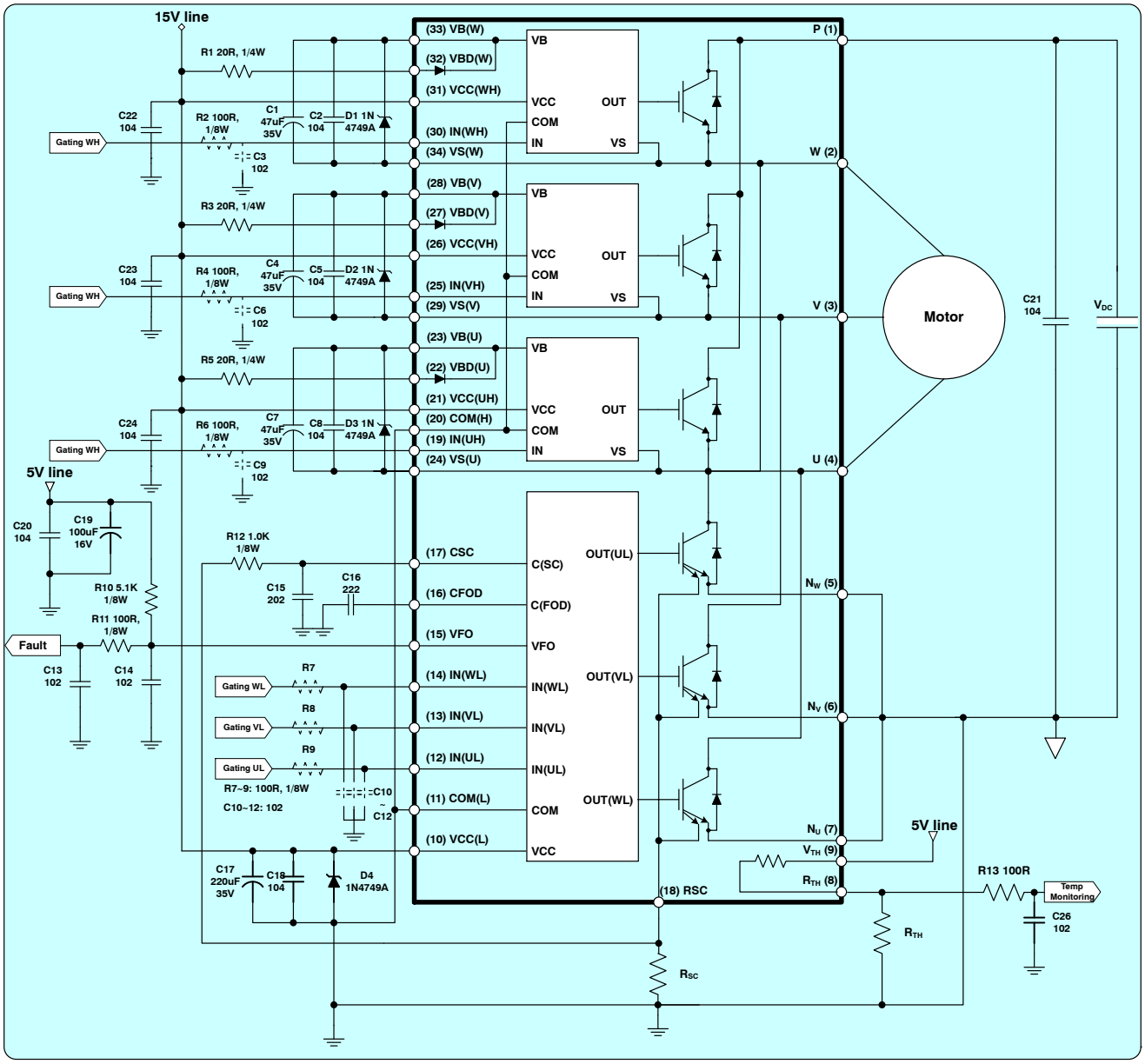


Figure 46. General Application Circuitry for Motion SPM 2

PCB Layout Guidance

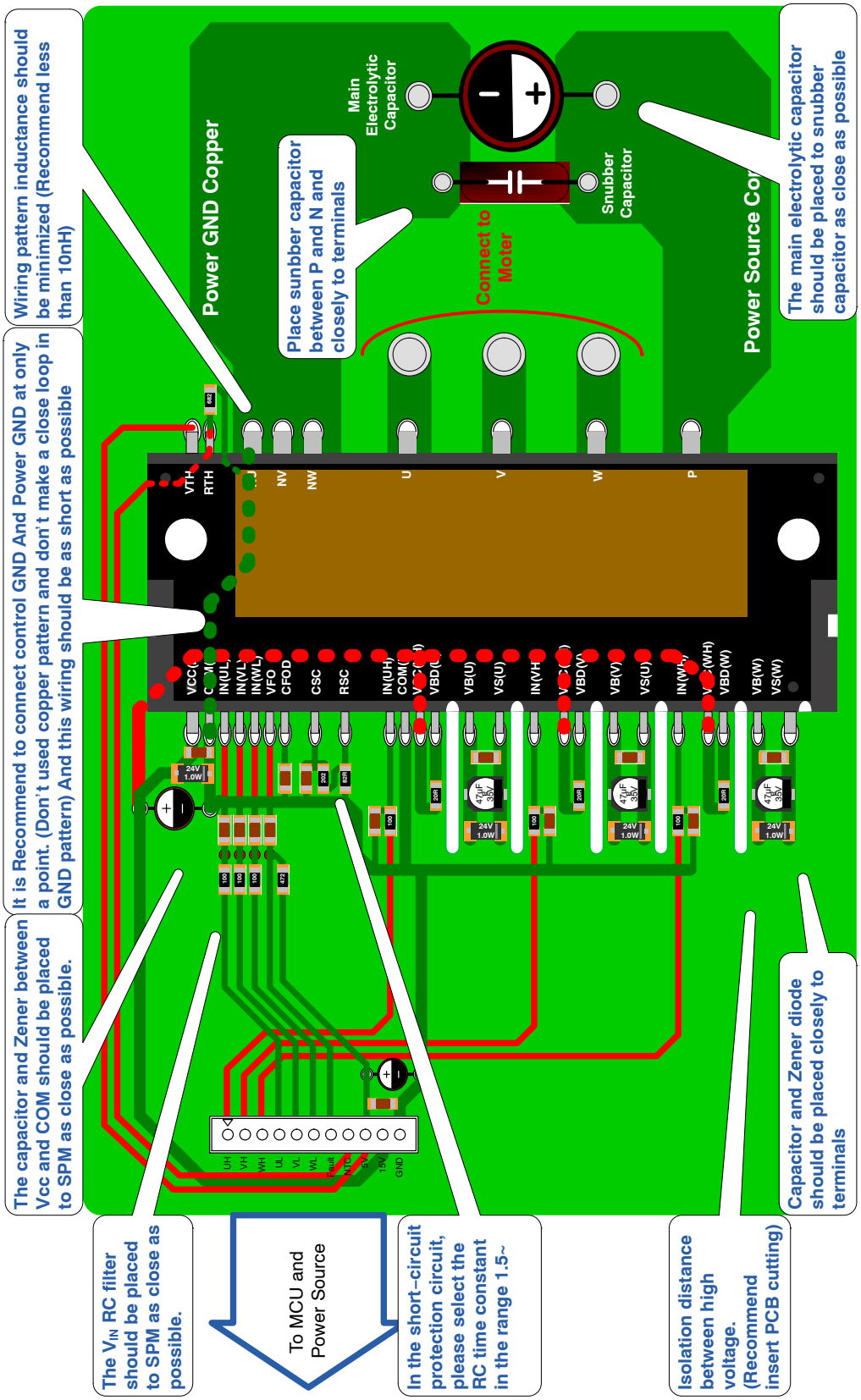


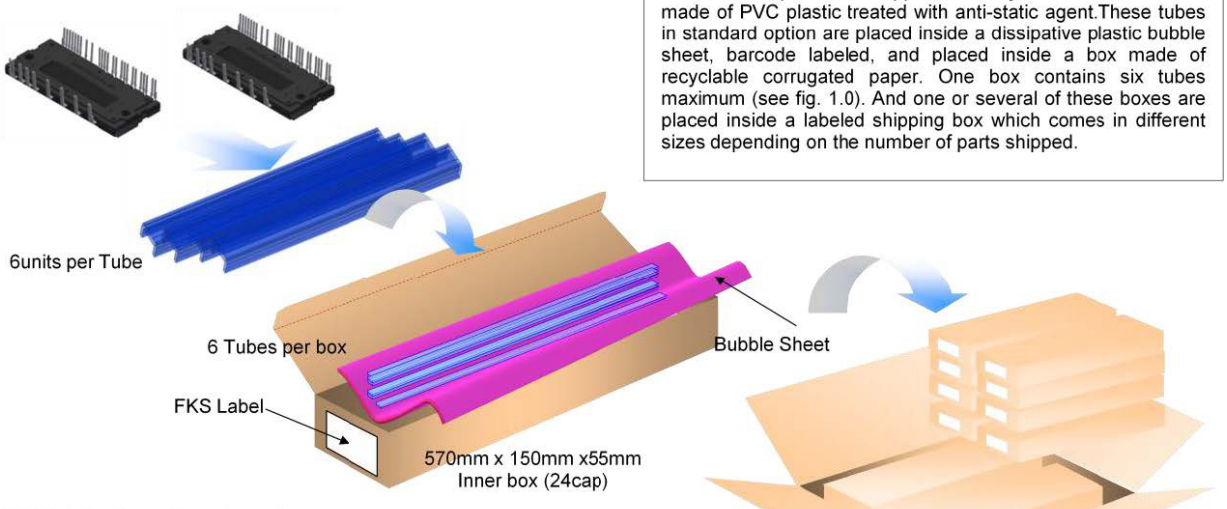
Figure 47. Print Circuit Board (PCB) Layout Guidance for Motion SPM 2

Packing Information

SPMCA-A34 Tube Packing Configuration: Figure 1.0

Packaging Description:

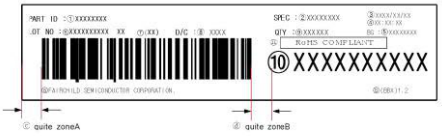
SPMCA-A34 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains six tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.



SPMCA-A34 Packaging Configuration: Figure 2.0

Inner Box Barcode Label Sample

Outer Box Barcode Label Sample



SPMCA-A34 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	6
Inner Box Dimension (mm)	570x150x55
Max qty per Box	24
Outer Box Dimension (mm)	590x330x245
Max qty per Box	192
Weight per unit (gm)	-
Note/Comments	

SPMCA-A34 Tube Configuration: Figure 3.0

Note: All dimensions are in mm

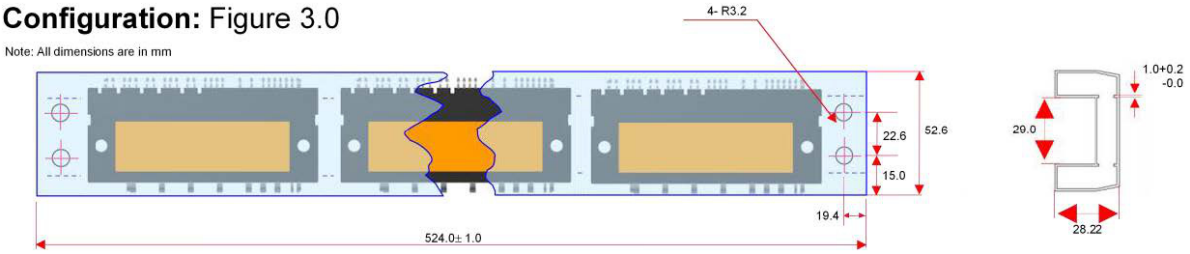


Figure 48. Packing Information

Related Resources

AN−9076 − New SPM 2 Package Mounting Guidance
AN−9079 − SPM 2 Series Thermal Performance by Mounting Torque
FNA21012A Product Information
FNA22512A Product Information
FNA23512A Product Information

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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