MAC15SD, MAC15SM, MAC15SN

Preferred Device

Sensitive Gate Triacs

Silicon Bidirectional Thyristors

Designed for industrial and consumer applications for full wave control of AC loads such as appliance controls, heater controls, motor controls, and other power switching applications.

Features

- Sensitive Gate allows Triggering by Microcontrollers and other Logic Circuits
- High Immunity to dv/dt − 25 V/μs minimum at 110°C
- High Commutating di/dt − 8.0 A/ms minimum at 110°C
- Maximum Values of I_{GT}, V_{GT} and I_H Specified for Ease of Design
- On-State Current Rating of 15 Amperes RMS at 70°C
- High Surge Current Capability − 120 Amperes
- Blocking Voltage to 800 Volts
- Rugged, Economical TO−220AB Package
- Uniform Gate Trigger Currents in Three Quadrants, Q1, Q2, and Q3
- Pb−Free Packages are Available*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (T_J = −40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open) MAC15SD MAC15SM MAC15SN	V_{DRM}, V_{RRM}	 400 600 800	V
On−State RMS Current (Full Cycle Sine Wave, 60Hz, T_J = 70°C)	$I_{T(RMS)}$	15	A
Peak Non-repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T_J = 110°C)	I_{TSM}	120	A
Circuit Fusing Consideration (t = 8.3 ms)	I^2t	60	A^2s
Peak Gate Power (Pulse Width ≤ 1.0 μs, T_C = 70°C)	P_{GM}	20	W
Average Gate Power (t = 8.3 ms, T_C = 70°C)	$P_{G(AV)}$	0.5	W
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

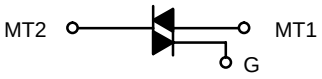
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

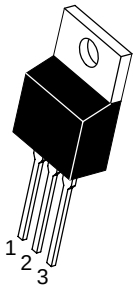
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

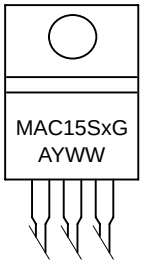
TRIACS
15 AMPERES RMS
400 thru 800 VOLTS





TO−220AB
CASE 221A−09
STYLE 4

MARKING DIAGRAM



x = D, M, or N
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

PIN ASSIGNMENT	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

Device	Package	Shipping
MAC15SD	TO−220AB	50 Units / Rail
MAC15SDG	TO−220AB (Pb−Free)	50 Units / Rail
MAC15SM	TO−220AB	50 Units / Rail
MAC15SMG	TO−220AB (Pb−Free)	50 Units / Rail
MAC15SN	TO−220AB	50 Units / Rail
MAC15SNG	TO−220AB (Pb−Free)	50 Units / Rail

Preferred devices are recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Thermal Resistance,	Junction−to−Case Junction−to−Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds		T_L	260	°C

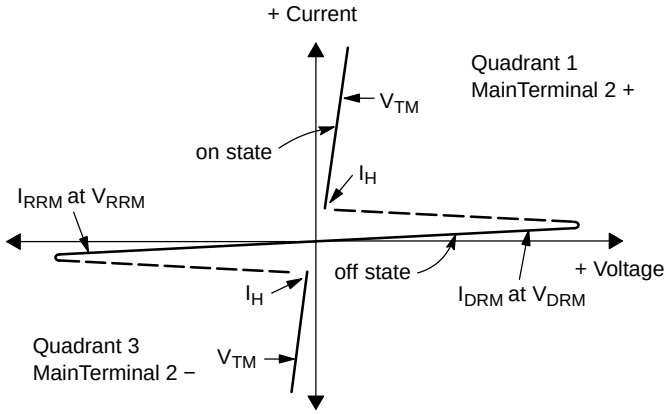
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, V_{RRM}; Gate Open)	 T_J = 25°C T_J = 110°C	I_{DRM}, I_{RRM}	 − −	 − −	 0.01 2.0	mA
ON CHARACTERISTICS						
Peak On-State Voltage (Note 2) (I_{TM} = ±21A)		V_{TM}	−	−	1.8	V
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100Ω) MT2(+), G(+) MT2(+), G(−) MT2(−), G(−)		I_{GT}	 − − −	 2.0 3.0 3.0	 5.0 5.0 5.0	mA
Hold Current (V_D = 12 V, Gate Open, Initiating Current = ±150mA)		I_H	−	3.0	10	mA
Latching Current (V_D = 24V, I_G = 5mA) MT2(+), G(+) MT2(+), G(−) MT2(−), G(−)		I_L	 − − −	 5.0 10 5.0	 15 20 15	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100Ω) MT2(+), G(+) MT2(+), G(−) MT2(−), G(−)		V_{GT}	 0.45 0.45 0.45	 0.62 0.60 0.65	 1.5 1.5 1.5	V
DYNAMIC CHARACTERISTICS						
Rate of Change of Commutating Current (V_D = 400V, I_{TM} = 3.5A, Commutating dv/dt = 10Vμ/sec, Gate Open, T_J = 110°C, f= 500Hz, Snubber: C_S = 0.01 μF, R_S =15Ω, see Figure 15)		(di/dt)c	8.0	10	−	A/ms
Critical Rate of Rise of Off-State Voltage (V_D = Rate V_{DRM}, Exponential Waveform, R_{GK} = 510Ω, T_J = 110°C)		dv/dt	25	75	−	V/μs

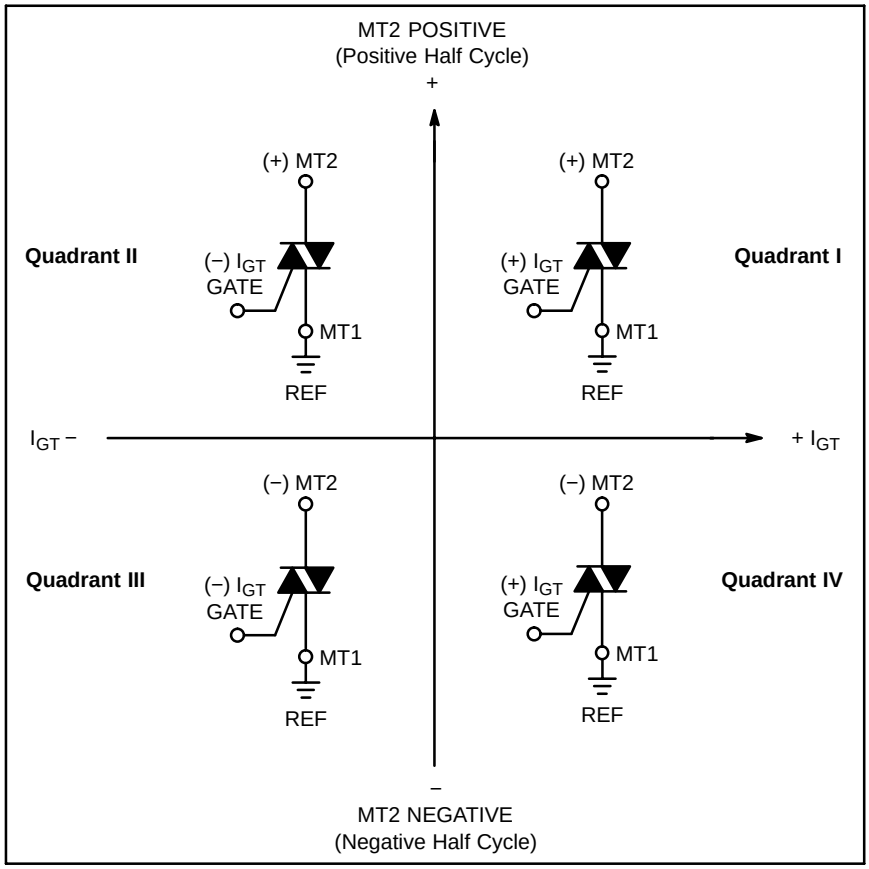
2. Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in−phase signals (using standard AC lines) quadrants I and III are used.

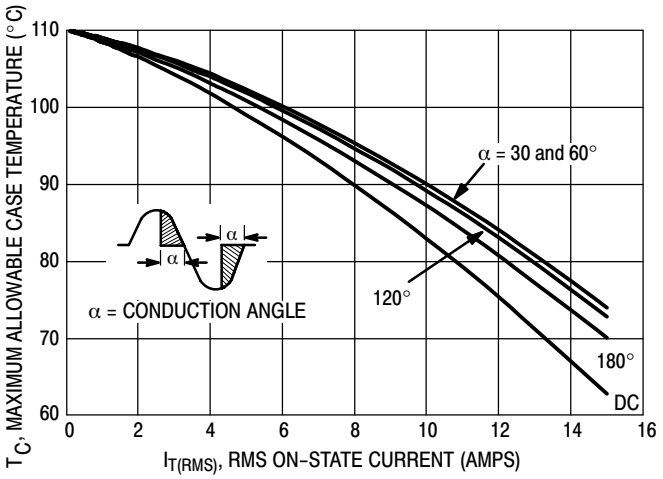


Figure 1. RMS Current Derating

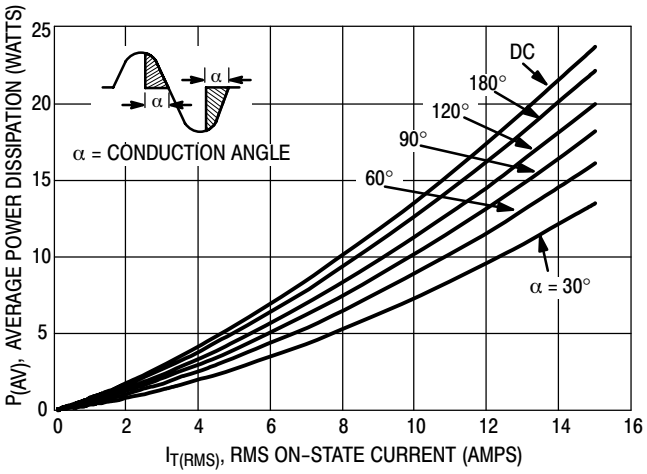


Figure 2. Maximum On−State Power Dissipation

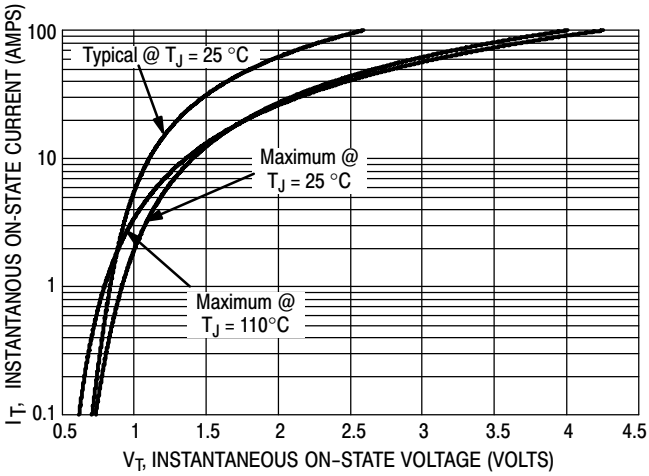


Figure 3. On−State Characteristics

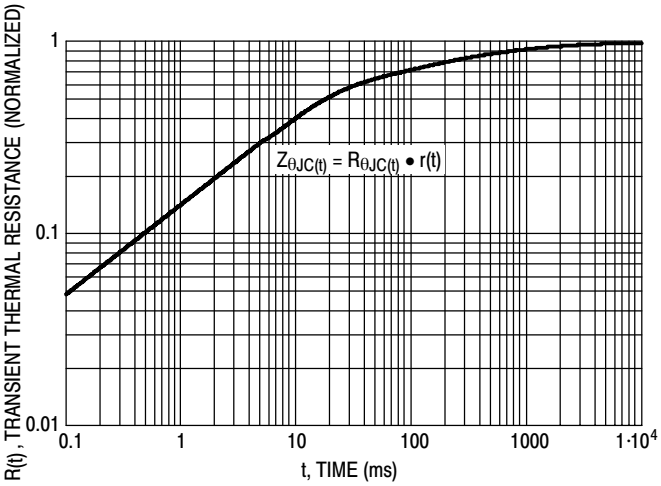


Figure 4. Transient Thermal Response

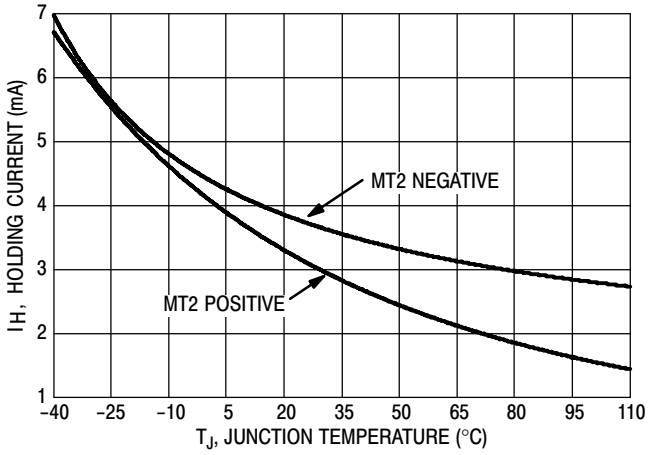


Figure 5. Typical Holding Current Versus Junction Temperature

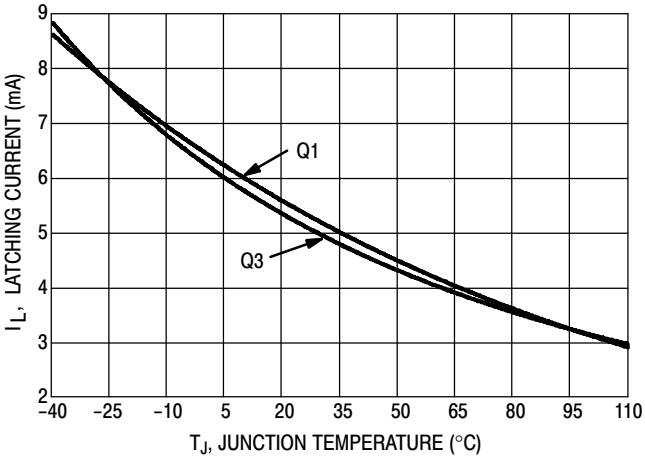


Figure 6. Typical Latching Current Versus Junction Temperature

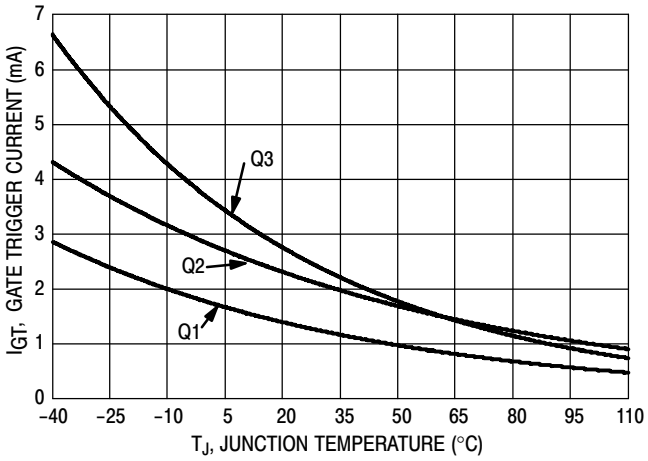


Figure 7. Typical Gate Trigger Current Versus Junction Temperature

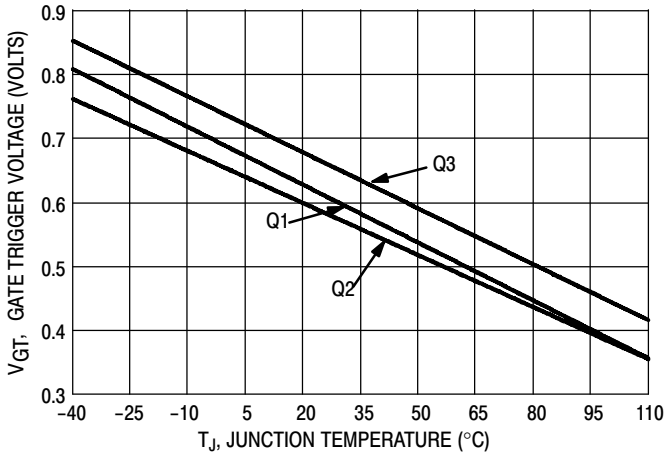


Figure 8. Typical Gate Trigger Voltage Versus Junction Temperature

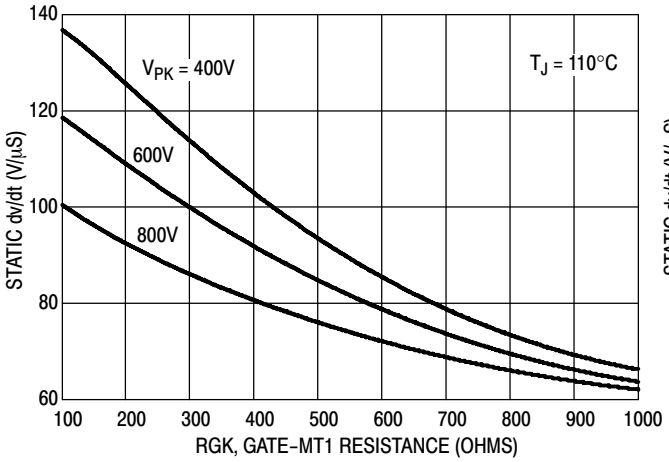


Figure 9. Typical Exponential Static dv/dt Versus Gate−MT1 Resistance, MT2(+)

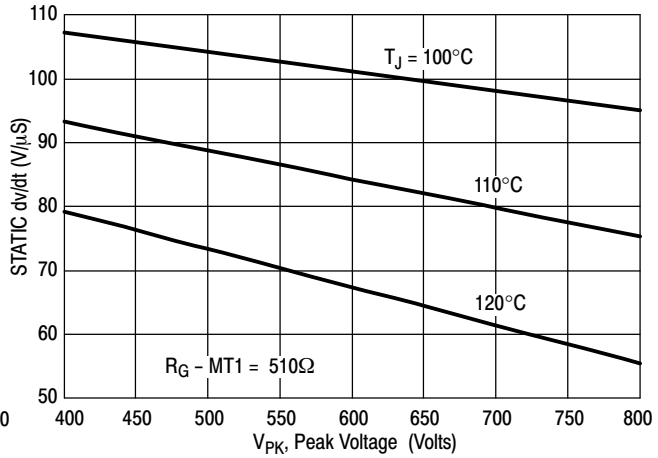


Figure 10. Typical Exponential Static dv/dt Versus Peak Voltage, MT2(+)

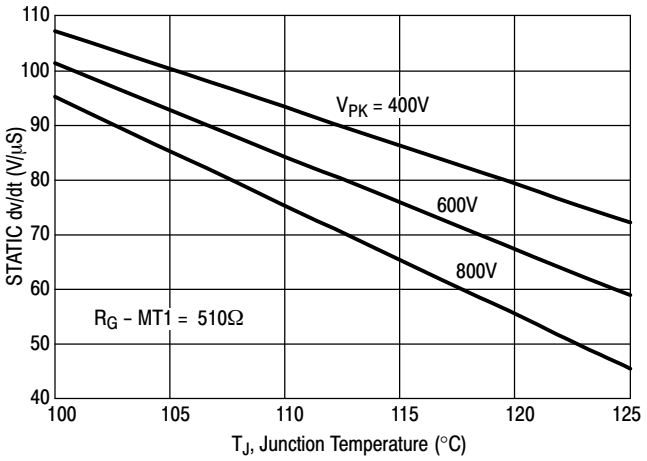


Figure 11. Typical Exponential Static dv/dt Versus Junction Temperature, MT2(+)

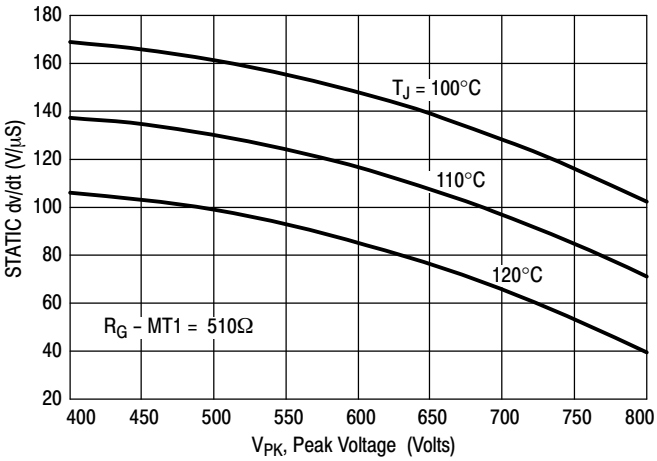


Figure 12. Typical Exponential Static dv/dt Versus Peak Voltage, MT2(−)

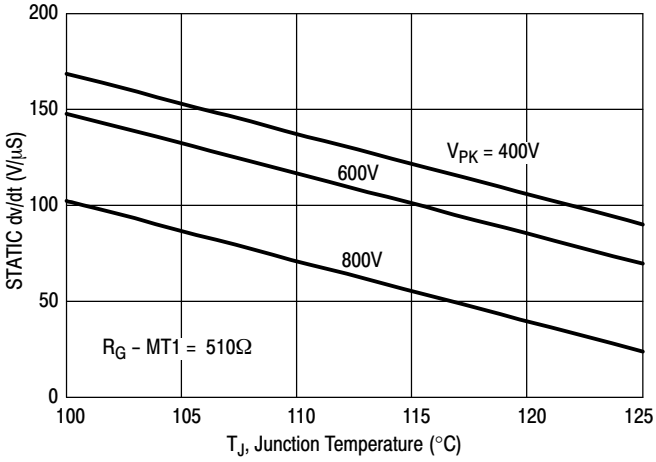


Figure 13. Typical Exponential Static dv/dt Versus Junction Temperature, MT2(−)

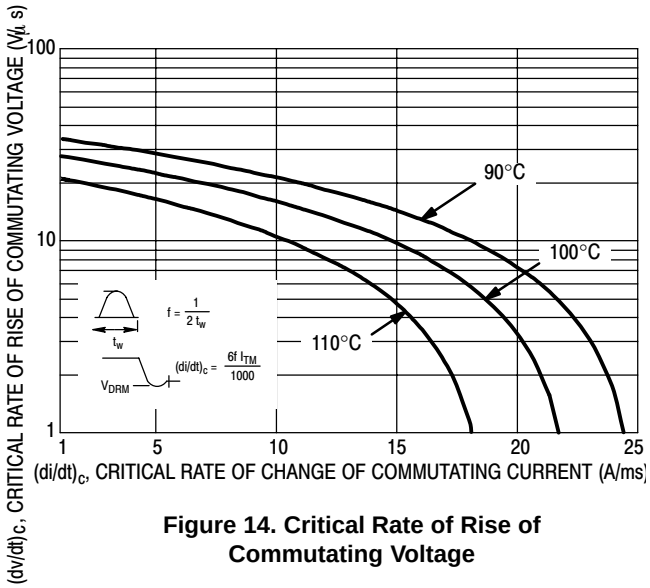
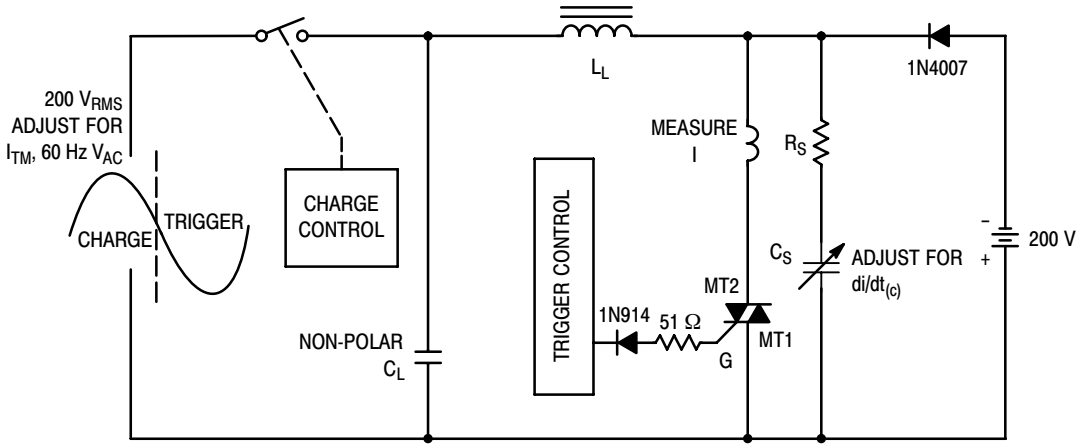


Figure 14. Critical Rate of Rise of Commutating Voltage



Note: Component values are for verification of rated $(di/dt)_c$. See AN1048 for additional information.

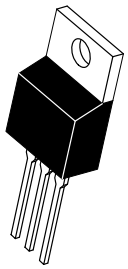
Figure 15. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current $(di/dt)_c$

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

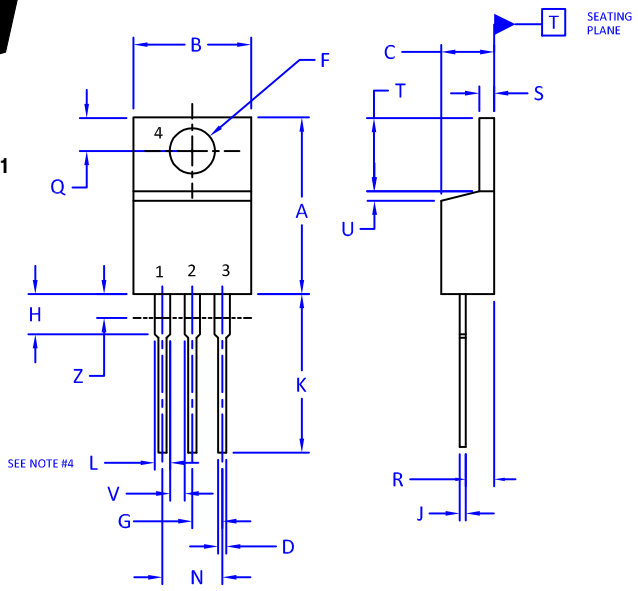
ON Semiconductor®

TO−220
CASE 221A−09
ISSUE AJ

DATE 05 NOV 2019



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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