

# NSS1C301ET4G

## 100 V, 3.0 A, Low $V_{CE(sat)}$ NPN Transistor

ON Semiconductor's e<sup>2</sup>PowerEdge family of low  $V_{CE(sat)}$  transistors are surface mount devices featuring ultra low saturation voltage ( $V_{CE(sat)}$ ) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e<sup>2</sup>PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

### Features

- Complement to NSS1C300ET4G
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Rating	Symbol	Max	Unit
Collector-Base Voltage	$V_{CBO}$	140	Vdc
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	6.0	Vdc
Collector Current - Continuous	$I_C$	3.0	Adc
Collector Current - Peak	$I_{CM}$	6.0	Adc
Base Current	$I_B$	0.5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	33 0.26	W W/ $^\circ\text{C}$
Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.1 0.017	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

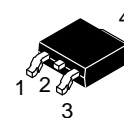
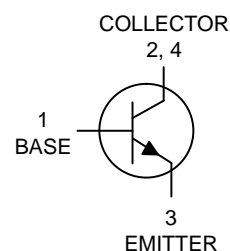
1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.



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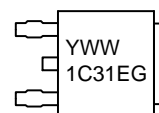
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## 100 VOLTS, 3.0 AMPS 12.5 WATTS NPN LOW $V_{CE(sat)}$ TRANSISTOR



DPAK  
CASE 369C  
STYLE 1

### MARKING DIAGRAM



Y = Year  
WW = Work Week  
1C31E = Device Code  
G = Pb-Free

### ORDERING INFORMATION

Device	Package	Shipping†
NSS1C301ET4G	DPAK (Pb-Free)	2500/ Tape & Reel
NSV1C301ET4G	DPAK (Pb-Free)	2500/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NSS1C301ET4G

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.8	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	59.5	$^{\circ}C/W$

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ( $I_C = 10\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	100	-	-	V
Collector-Base Breakdown Voltage ( $I_C = 0.1\text{ mA}$ , $I_E = 0$ )	$V_{(BR)CBO}$	140	-	-	V
Emitter-Base Breakdown Voltage ( $I_E = 0.1\text{ mA}$ , $I_C = 0$ )	$V_{(BR)EBO}$	6.0	-	-	V
Collector Cutoff Current ( $V_{CB} = 140\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	-	-	0.1	$\mu A$
Emitter Cutoff Current ( $V_{EB} = 6.0\text{ V}$ )	$I_{EBO}$	-	-	0.1	$\mu A$

### ON CHARACTERISTICS

DC Current Gain (Note 3) ( $I_C = 0.1\text{ A}$ , $V_{CE} = 2.0\text{ V}$ ) ( $I_C = 0.5\text{ A}$ , $V_{CE} = 2.0\text{ V}$ ) ( $I_C = 1.0\text{ A}$ , $V_{CE} = 2.0\text{ V}$ ) ( $I_C = 3.0\text{ A}$ , $V_{CE} = 2.0\text{ V}$ )	$h_{FE}$	200 200 120 80	- - - -	- - 360 -	-
Collector-Emitter Saturation Voltage (Note 3) ( $I_C = 0.1\text{ A}$ , $I_B = 10\text{ mA}$ ) ( $I_C = 1.0\text{ A}$ , $I_B = 0.100\text{ A}$ ) ( $I_C = 2.0\text{ A}$ , $I_B = 0.200\text{ A}$ ) ( $I_C = 3.0\text{ A}$ , $I_B = 0.300\text{ A}$ )	$V_{CE(sat)}$	- - - -	0.015 0.045 0.080 0.115	0.050 0.090 0.150 0.250	V
Base-Emitter Saturation Voltage (Note 3) ( $I_C = 1.0\text{ A}$ , $I_B = 0.1\text{ A}$ )	$V_{BE(sat)}$	-	-	1.0	V
Base-Emitter Turn-on Voltage (Note 3) ( $I_C = 1.0\text{ A}$ , $V_{CE} = 2.0\text{ V}$ )	$V_{BE(on)}$	-	-	0.90	V
Cutoff Frequency ( $I_C = 500\text{ mA}$ , $V_{CE} = 10\text{ V}$ , $f = 100\text{ MHz}$ )	$f_T$	-	120	-	MHz
Input Capacitance ( $V_{EB} = 5.0\text{ V}$ , $f = 1.0\text{ MHz}$ )	$C_{ibo}$	-	360	-	pF
Output Capacitance ( $V_{CB} = 10\text{ V}$ , $f = 1.0\text{ MHz}$ )	$C_{obo}$	-	30	-	pF

3. Pulsed Condition: Pulse Width = 300  $\mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NSS1C301ET4G

## TYPICAL CHARACTERISTICS

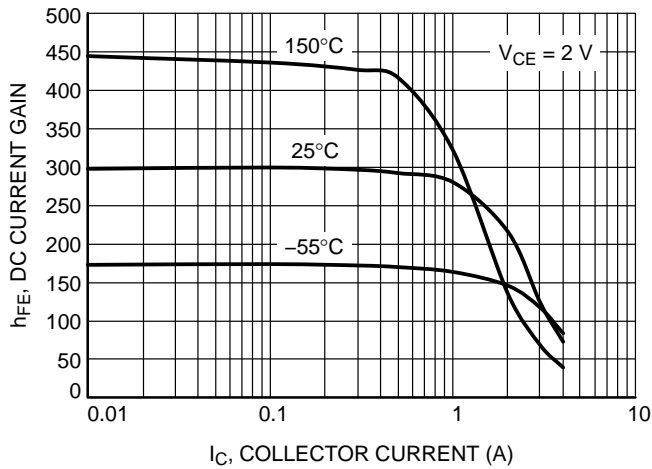


Figure 1. DC Current Gain

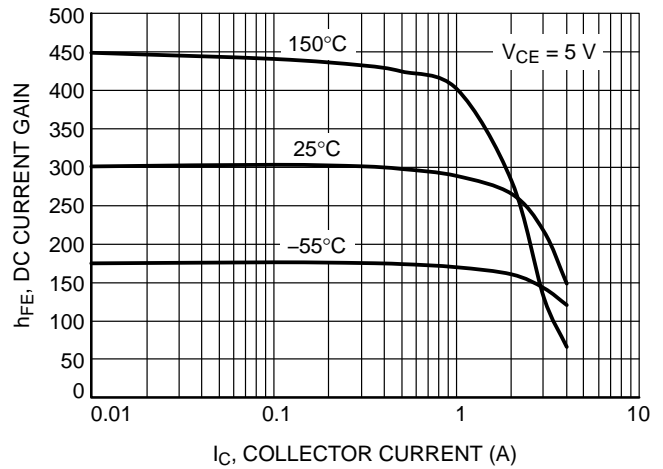


Figure 2. DC Current Gain

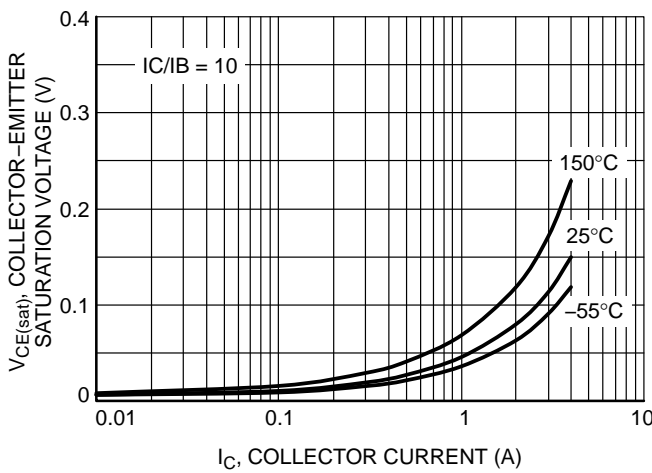


Figure 3. Collector-Emitter Saturation Voltage

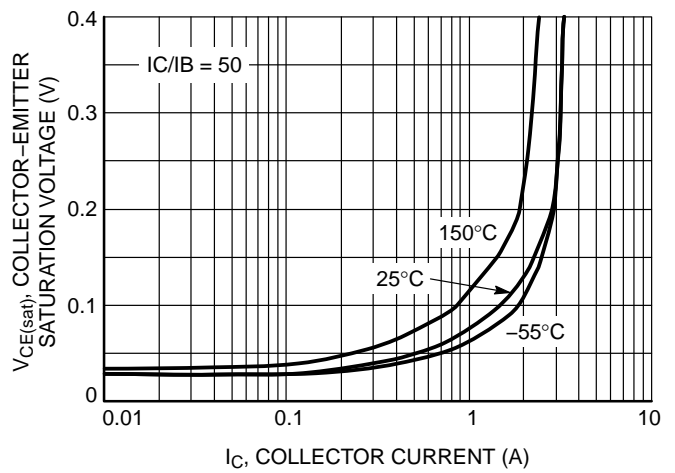


Figure 4. Collector-Emitter Saturation Voltage

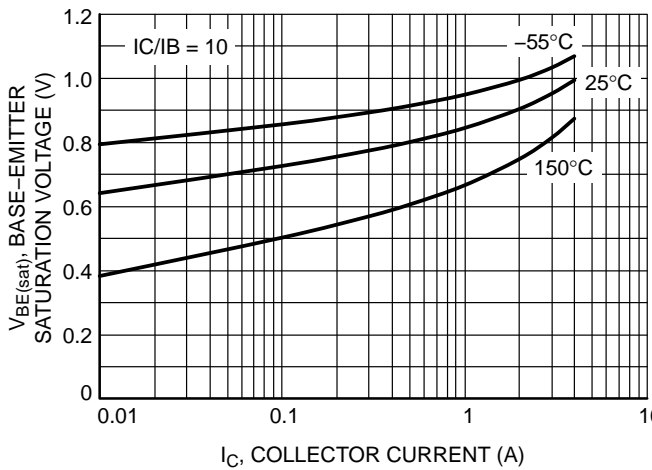


Figure 5. Base-Emitter Saturation Voltage

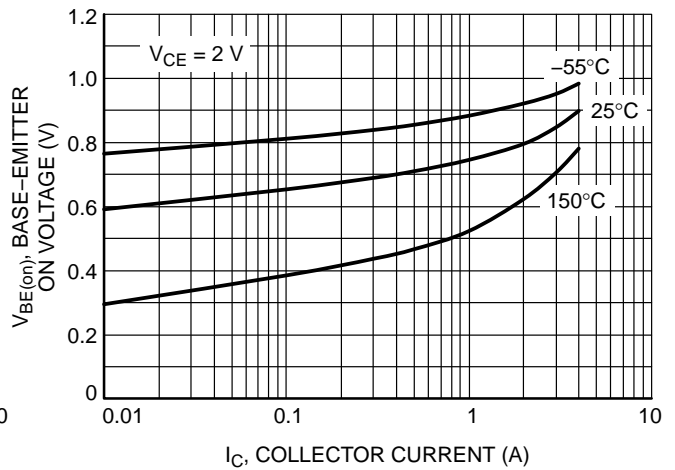


Figure 6. Base-Emitter "On" Voltage

# NSS1C301ET4G

## TYPICAL CHARACTERISTICS

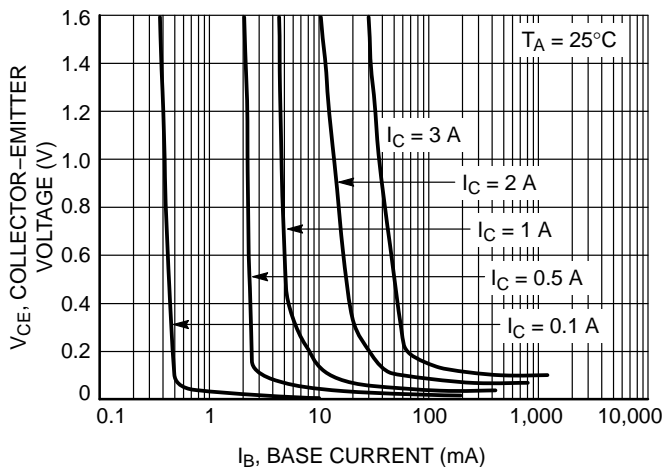


Figure 7. Collector Saturation Region

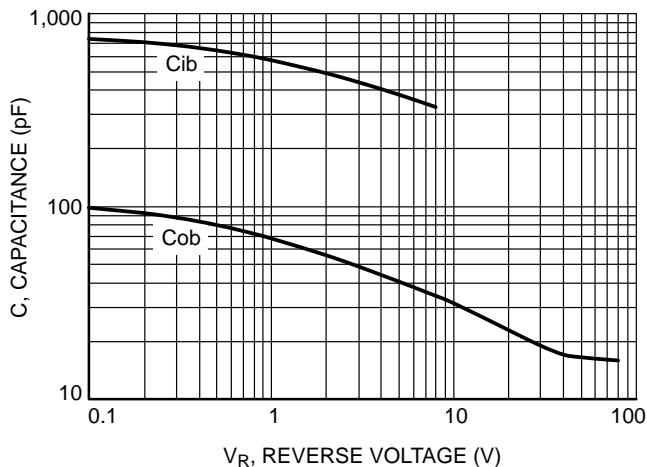


Figure 8. Capacitance

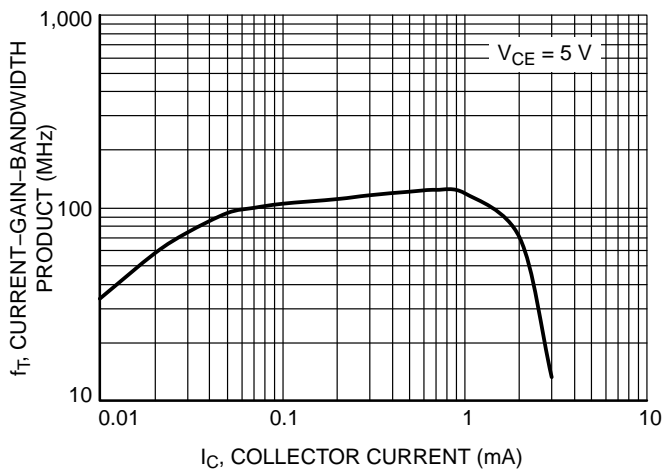


Figure 9. Current-Gain-Bandwidth Product

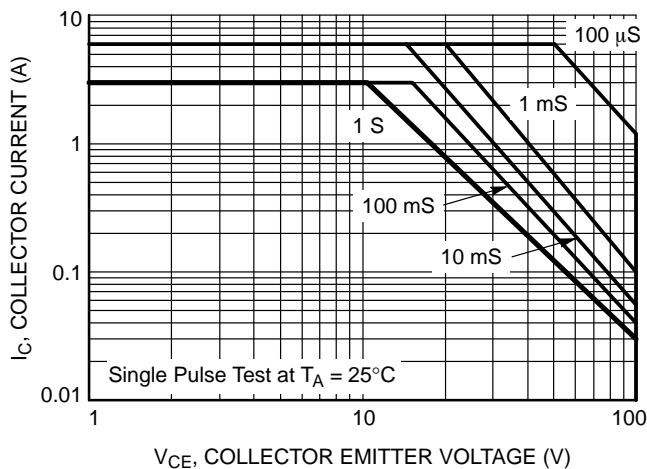


Figure 10. Safe Operating Area

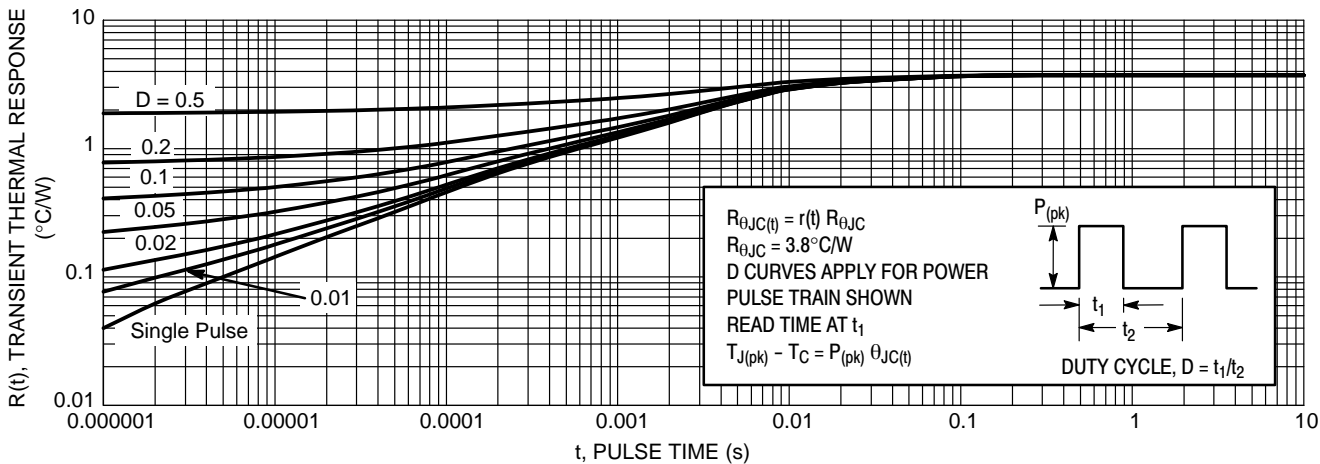
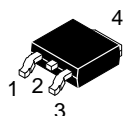


Figure 11. Typical Transient Thermal Response, Junction-to-Case

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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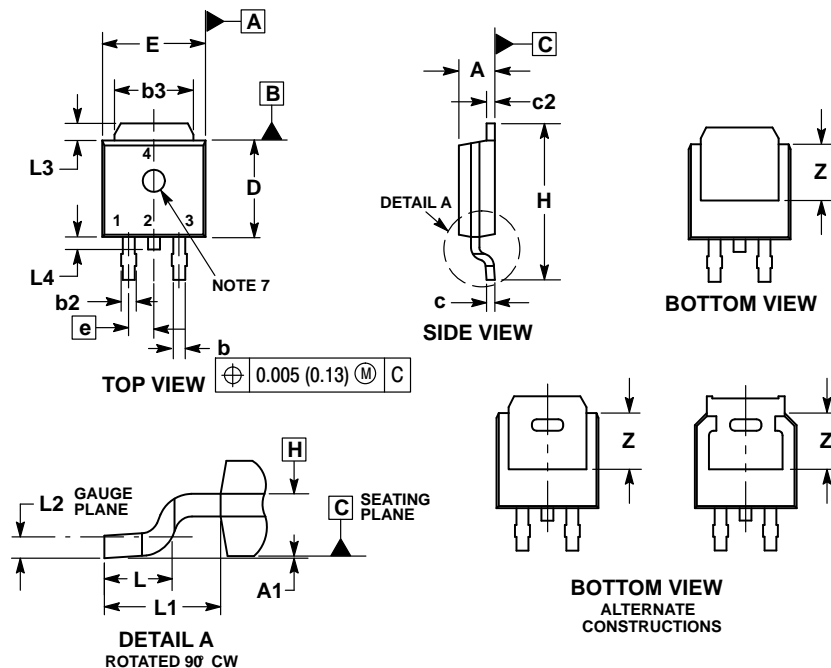
SCALE 1:1

### DPAK (SINGLE GAUGE)

#### CASE 369C

#### ISSUE F

DATE 21 JUL 2015

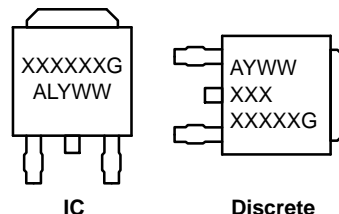


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*

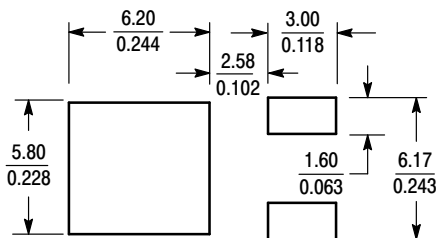


- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>          | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p> | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p>              | <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>     |
| <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 8:<br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p>STYLE 9:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm / inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>NEW STANDARD:</b>	<b>REF TO JEDEC TO-252</b>	
<b>DESCRIPTION:</b>	<b>DPAK SINGLE GAUGE SURFACE MOUNT</b>	<b>PAGE 1 OF 2</b>



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