SCY99250

LDO Regulator, 200 mA, Dual Selectable Output Voltage, Low V_{IN}, Low Noise and High PSRR

The SCY99250 is a state of art ultra-small Linear Regulator capable of supplying 200 mA output current from as low as 1.1 V input voltage, with superior low noise and high PSRR performance. The device provides two output levels on one output pin, selectable via SEL pin. Each output level is factory programmable in increments of 50 mV ranging from 1.0 V up to 4.0 V. Output transition between high to low level is internally controlled for optimum operation. Device is enabled upon applying a valid input voltage. Due to low quiescent current the SCY99250 is suitable for battery powered devices such as smartphones and tablets. The device is designed to work with a 1 μF input and 1 μF output ceramic capacitor. It is available in two very thin ultra-small 0.64 mm × 0.64 mm 4-pin Wafer Level Chip Scale Packages (WLCSP).

Features

- Two Output Levels on One Output Pin, Selectable via SEL Pin
- Operating Input Voltage Range: 1.1 V to 5.5 V
- Available in Fixed Voltage Option: 1.0 V to 4.0 V
- ±2% Accuracy Over Load/Temperature
- Low Quiescent Current Typ. 80 μA
- Standby Current: Typ. 0.1 μA
- Very Low Dropout: 33 mV for 2.4 V @ 100 mA
- High PSRR: Typ. 95 dB at 20 mA, f = 1 kHz
- Ultra Low Noise: 8.8 μV_{RMS}
- Stable with a 1 μF Small Case Size Ceramic Capacitors
- Available in:
  – WLCSP4 0.64 mm x 0.64 mm x 0.33 mm, CASE 567VS
  – WLCSP4 0.64 mm x 0.64 mm x 0.4 mm, CASE 567XW
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

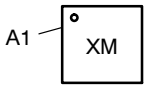
Applications

- Battery-powered Equipment
- Wireless LAN Devices
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

WLCSP4
CASE 567VS

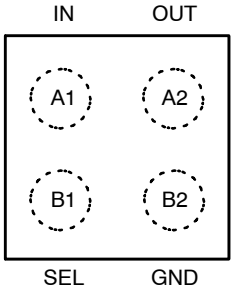
WLCSP4
CASE 567XW

MARKING DIAGRAM



X = Specific Device Code
M = Month

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

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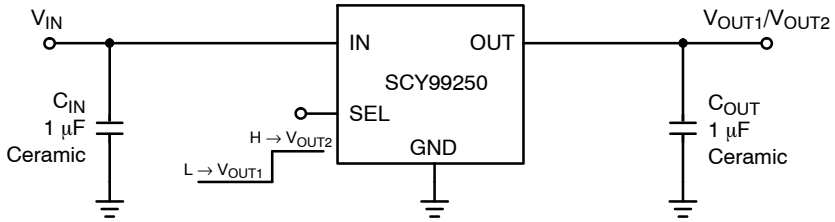


Figure 1. Typical Application Schematic

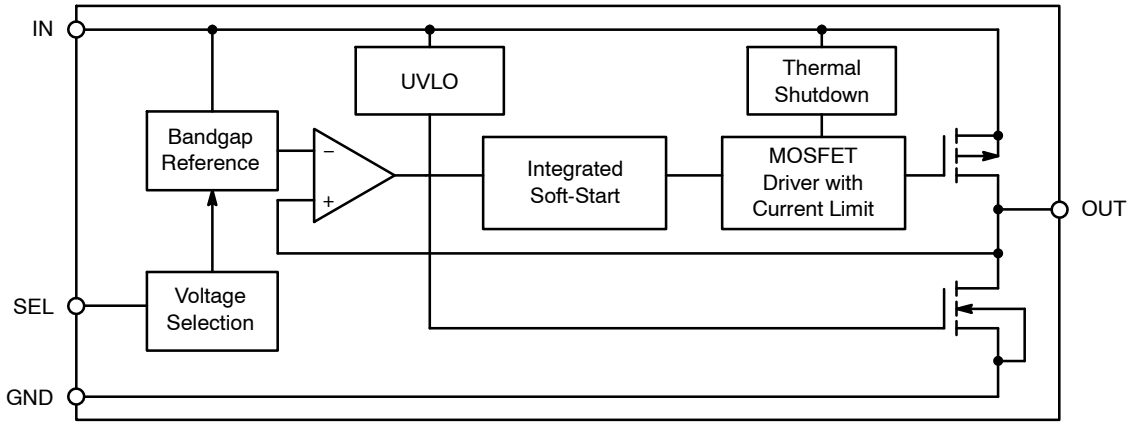


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
A1	IN	Input voltage supply pin
A2	OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor
B1	SEL	Voltage selection: Applying V_{SEL} < 0.2 V chooses lower output voltage, Pulling V_{SEL} > 0.7 V chooses higher output voltage
B2	GND	Common ground connection
–	EPAD	Expose pad can be tied to ground plane for better power dissipation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3, max. 6 V	V
Selection Input	V_{SEL}	−0.3 to 6	V
Output Short Circuit Duration	t_{SC}	unlimited	S
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Characteristics, WLCSP4 (Note 3), Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	108	°C/W

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7.

ELECTRICAL CHARACTERISTICS

($-40°C \le T_J \le 85°C$; $V_{IN} = V_{OUT(NOM)} + 0.3$ V or 1.1 V, whichever is greater; I_{OUT} = 1 mA; $C_{IN} = C_{OUT}$ = 1 μF, unless otherwise noted. Typical values are at T_J = +25°C (Note 4))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.1		5.5	V
Undervoltage Lock−Out	Rising V_{IN}		UVLO	0.85	0.95	1.06	V
	Falling V_{IN}			0.8	0.915	1.03	
Output Voltage Accuracy	$V_{IN} = V_{OUT(NOM)} + 0.3$ V, ($V_{IN} \ge 1.1$V), I_{OUT} = 1 mA to 200 mA		V_{OUT}	−2		+2	%
Line Regulation	$V_{OUT(NOM)} + 0.3$ V ≤ V_{IN} ≤ 5.5 V, ($V_{IN} \ge 1.1$V)		$Line_{Reg}$		0.02		%/V
Load Regulation	I_{OUT} = 1 mA to 200 mA		$Load_{Reg}$		0.001		%/mA
Dropout Voltage (Note 5)	$V_{OUT(NOM)}$ = 2.1 V, I_{OUT} = 100 mA		V_{DO}		37	65	mV
	$V_{OUT(NOM)}$ = 2.4 V, I_{OUT} = 100 mA				33	60	
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	275	350		mA
Short Circuit Current	V_{OUT} = 0 V		I_{SC}		350		
Quiescent Current	I_{OUT} = 0 mA		I_Q		80	95	μA
Shutdown Current	Rising V_{IN} < 0.8 V		I_{SHUT}		0.8	2.4	μA
	Falling V_{IN} < 0.8 V				1.3	3.4	
SEL Pin Threshold Voltage	SEL Input Voltage "H" ≤ V_{OUT2}		V_{SELH}	0.7			V
	SEL Input Voltage "L" ≤ V_{OUT1}		V_{SELL}			0.2	
SEL Pull Down Current	V_{SEL} = 1.1 V		I_{SEL}		0.2	0.5	μA
Transition time	V_{SEL} = H to L, $C_{OUT} \le 4$ μF		t_{TR}		150		μs
Delay Time	From assertion of V_{IN} to V_{OUT} increase		t_{DELAY}		40		μs
Rise Time	V_{OUT} rise from 10% to 90% $V_{OUT(NOM)}$		t_{RISE}		27		
Turn−On Time	From assertion of V_{IN} to 98% $V_{OUT(NOM)}$		t_{ON}		85		
Power Supply Rejection Ratio	I_{OUT} = 20 mA, $V_{IN} = V_{OUT} + 0.3$ V	f = 100 Hz	PSRR		90		dB
		f = 1 kHz			95		
		f = 10 kHz			85		
		f = 100 kHz			55		
Output Voltage Noise	f = 10 Hz to 100 kHz		V_N		8.8		μV_{RMS}
Thermal Shutdown Threshold	Temperature rising		T_{SDH}		160		°C
	Temperature falling		T_{SDL}		140		°C
Active Output Resistance	V_{IN} < 0.8 V, C version only		R_{DIS}		280		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 0.03 · $V_{OUT(NOM)}$ below $V_{OUT(NOM)}$.

TYPICAL CHARACTERISTICS

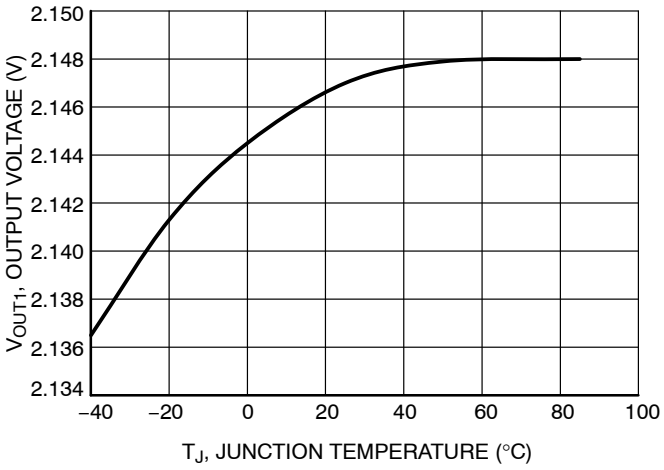


Figure 3. Output Voltage vs. Temperature, $V_{OUT1(NOM)}$ = 2.15 V

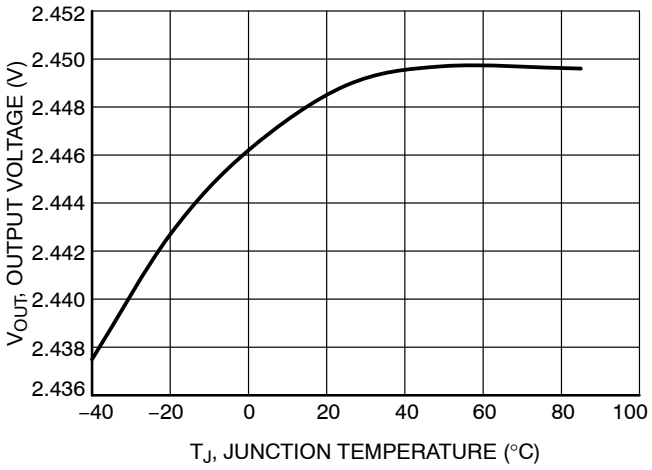


Figure 4. Output Voltage vs. Temperature, $V_{OUT1(NOM)}$ = 2.45 V

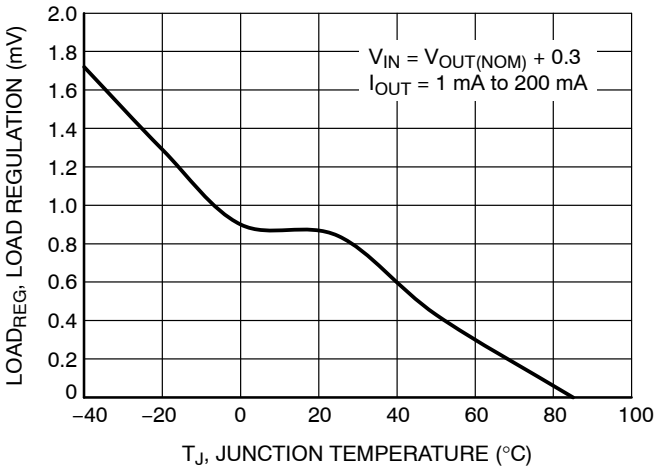


Figure 5. Load Regulation vs. Temperature

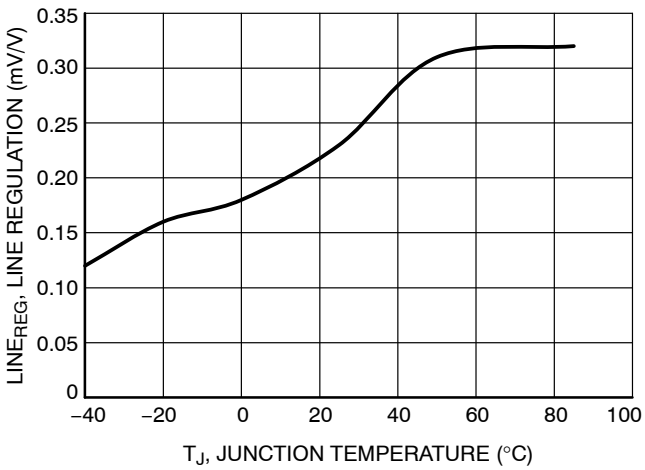


Figure 6. Line Regulation vs. Temperature

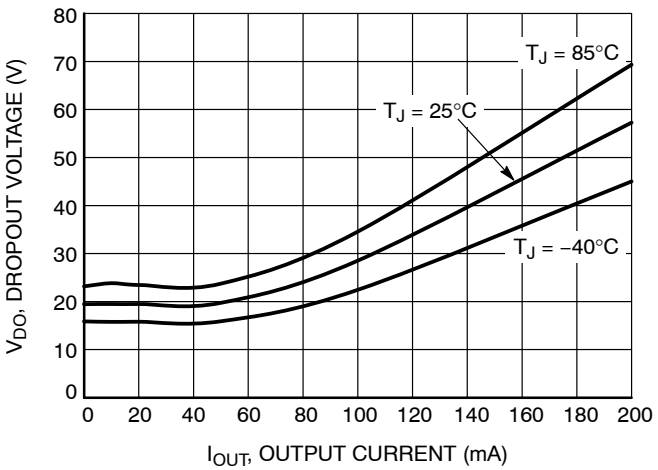


Figure 7. Dropout Voltage vs. Output Current, $V_{OUT1(NOM)}$ = 2.15 V

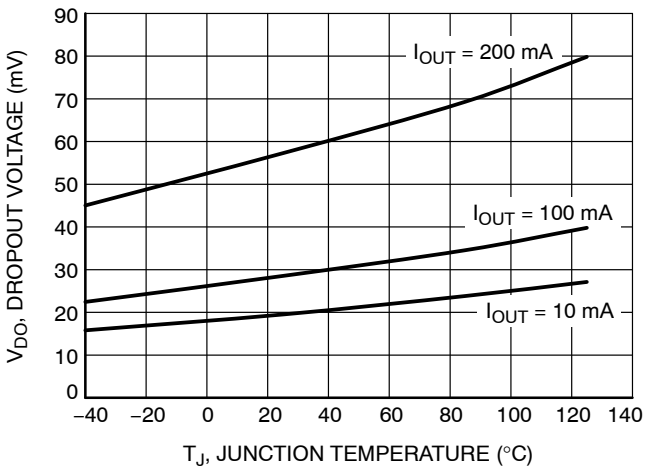


Figure 8. Dropout Voltage vs. Temperature, $V_{OUT1(NOM)}$ = 2.15 V

TYPICAL CHARACTERISTICS

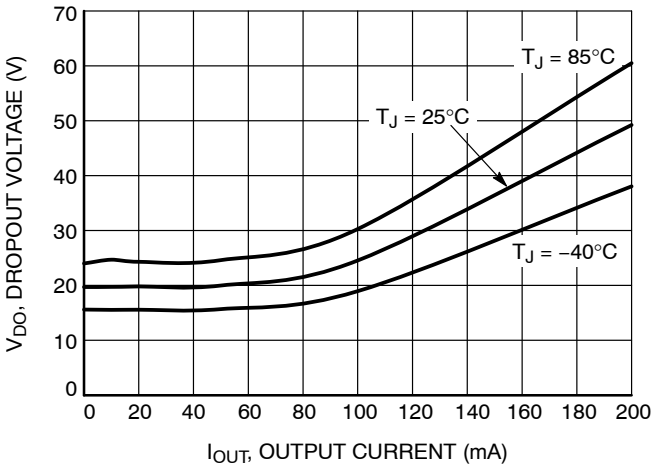


Figure 9. Dropout Voltage vs. Output Current, $V_{OUT1(NOM)}$ = 2.45 V

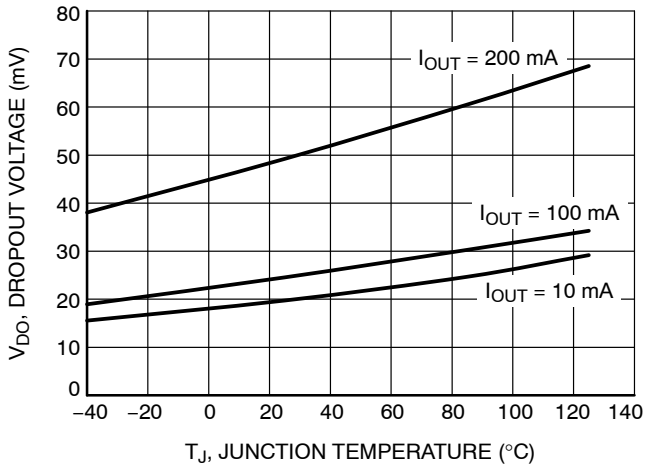


Figure 10. Dropout Voltage vs. Temperature, $V_{OUT1(NOM)}$ = 2.45 V

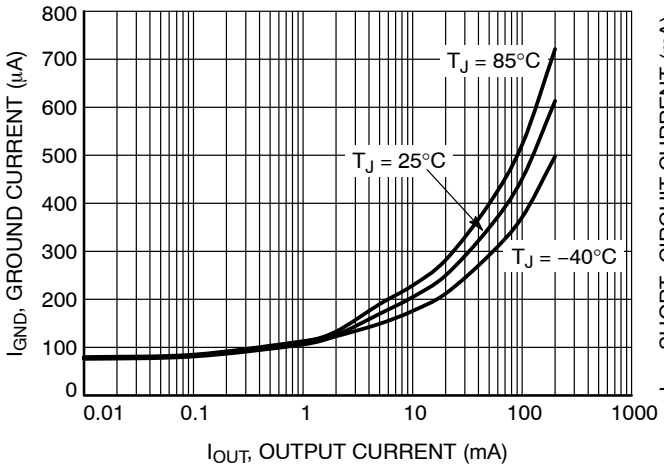


Figure 11. Ground Current vs. Output Current

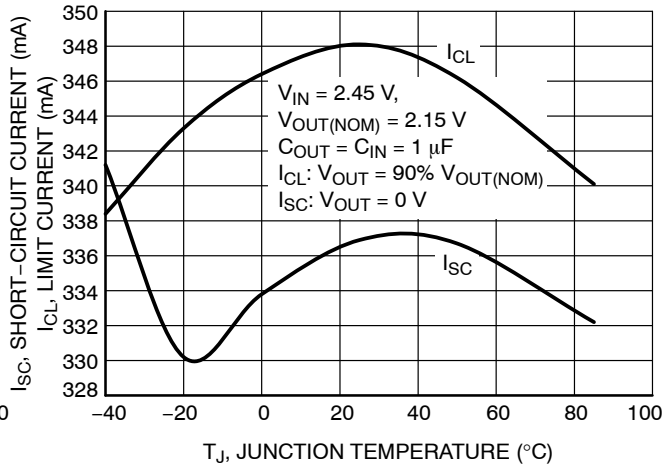


Figure 12. Short−circuit Current, Limit Current vs. Temperature

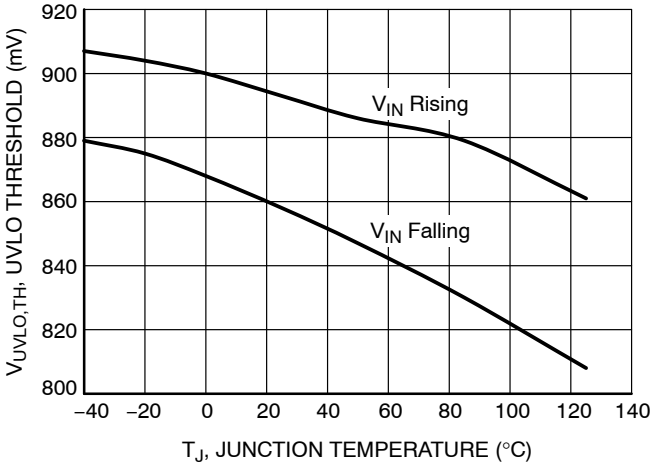


Figure 13. UVLO Threshold vs. Temperature

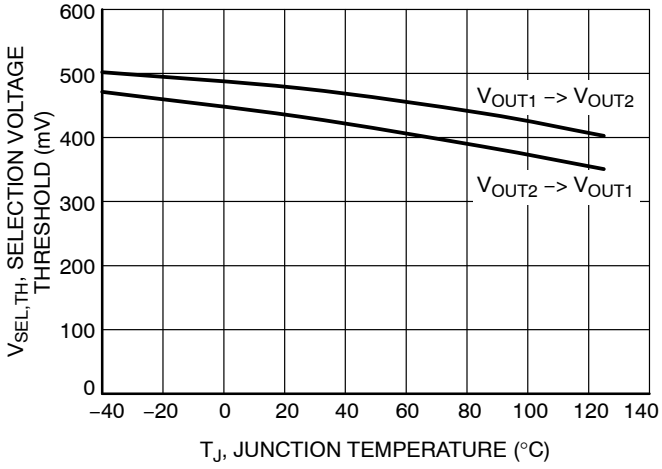


Figure 14. Selection Voltage Threshold vs. Temperature

TYPICAL CHARACTERISTICS

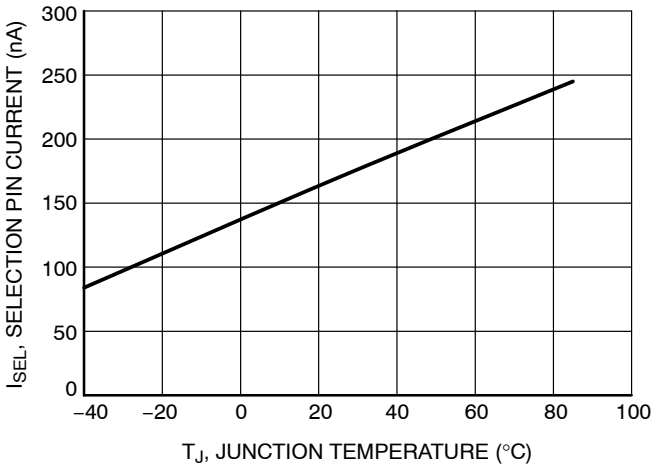


Figure 15. Selection Pin Current vs. Temperature

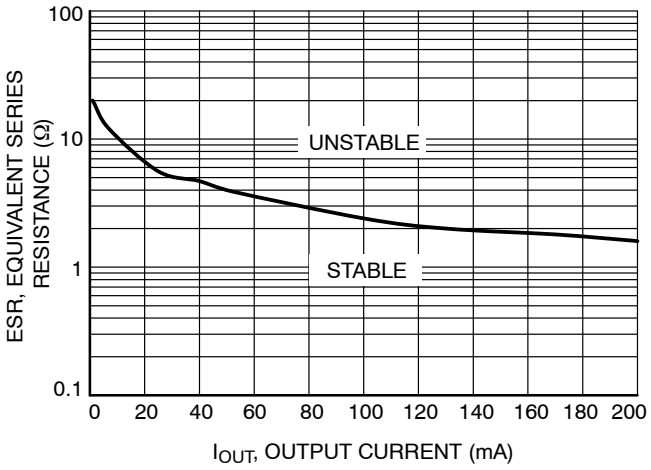


Figure 16. ESR vs. Output Current

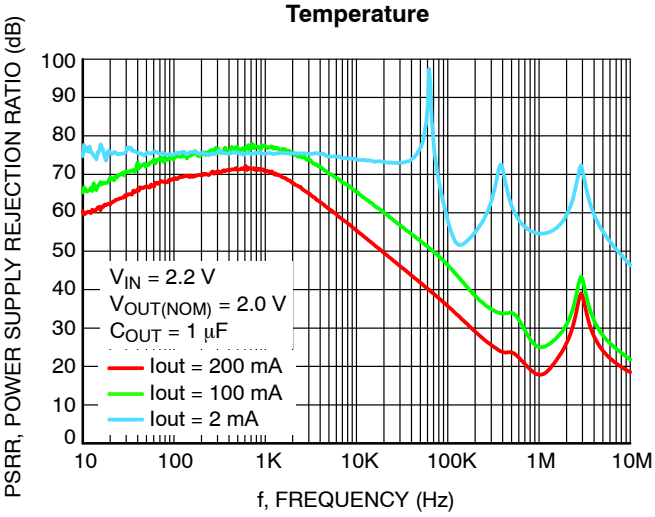


Figure 17. PSRR vs. FREQ, $V_{OUT(NOM)}$ = 2.0 V

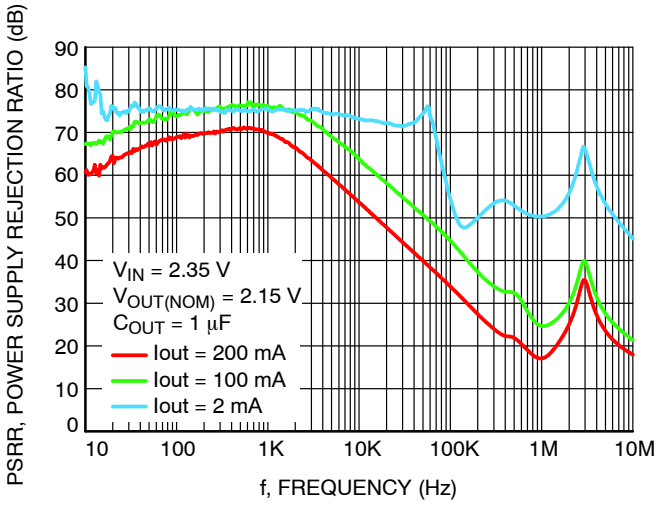


Figure 18. PSRR vs. FREQ, $V_{OUT(NOM)}$ = 2.15 V

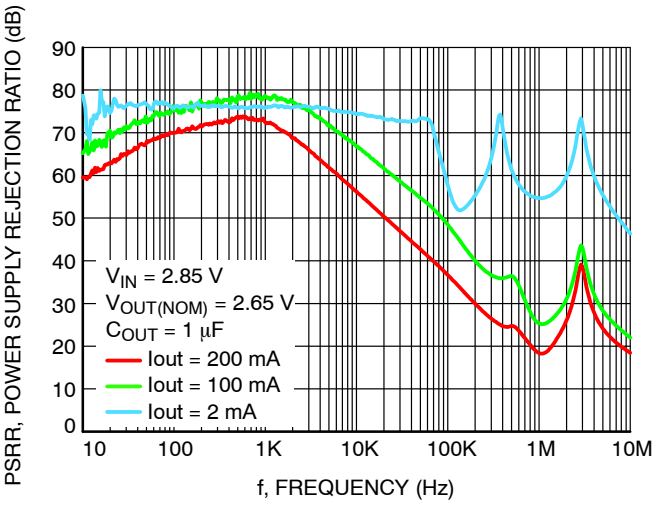


Figure 19. PSRR vs. FREQ, $V_{OUT(NOM)}$ = 2.65 V

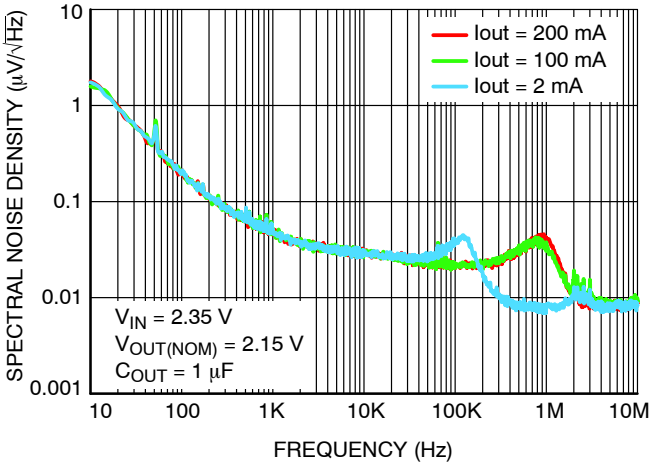


Figure 20. Spectral Noise Density vs. FREQ, $V_{OUT(NOM)}$ = 2.15 V

TYPICAL CHARACTERISTICS

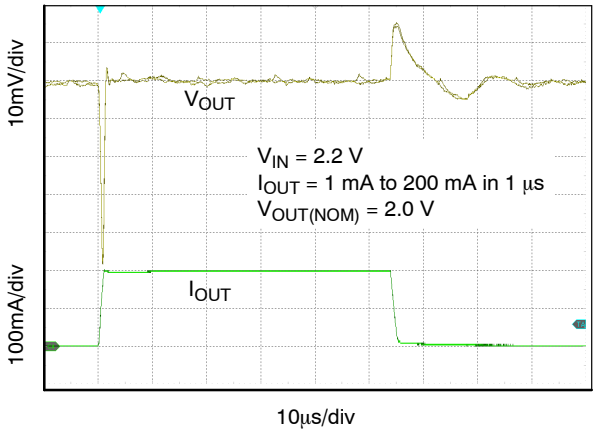


Figure 21. Load Transient Response 1 mA to 200 mA, $V_{OUT(NOM)}$ = 2.0 V

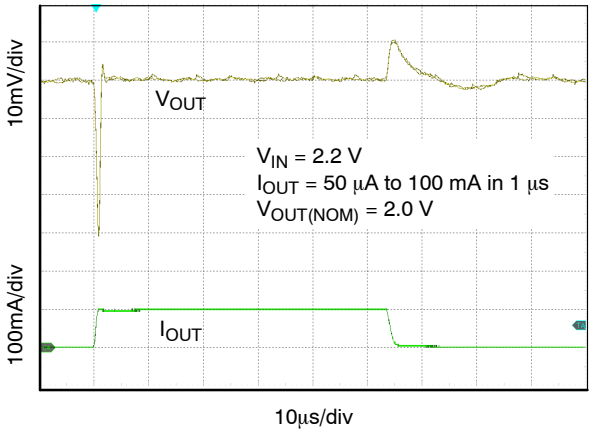


Figure 22. Load Transient Response 50 μA to 100 mA, $V_{OUT(NOM)}$ = 2.0 V

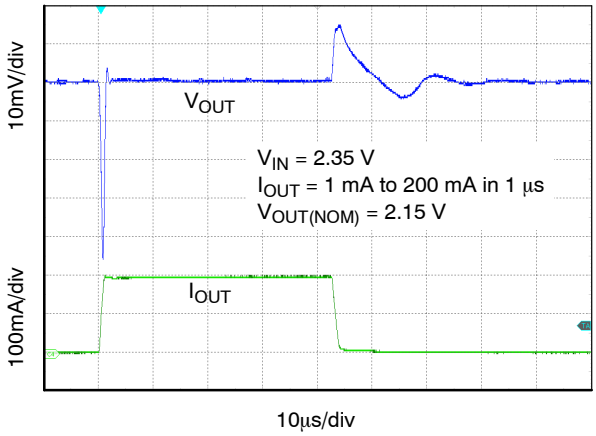


Figure 23. Load Transient Response 1 mA to 200 mA, $V_{OUT(NOM)}$ = 2.15 V

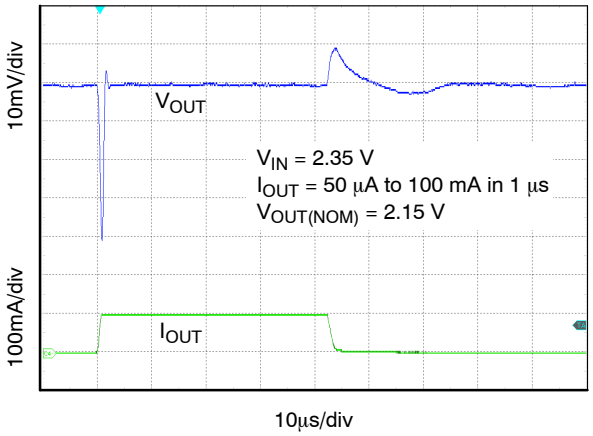


Figure 24. Load Transient Response 50 μA to 100 mA, $V_{OUT(NOM)}$ = 2.15 V

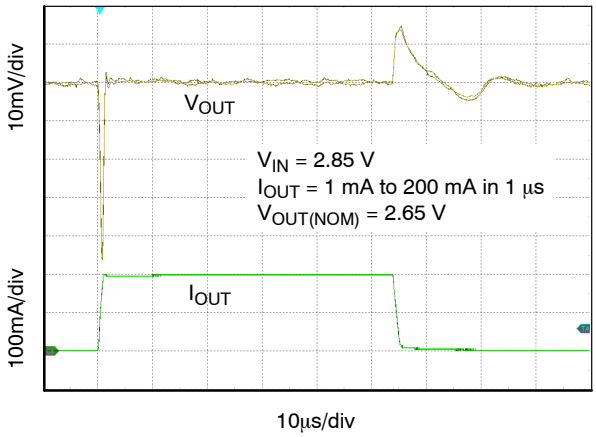


Figure 25. Load Transient Response 1 mA to 200 mA, $V_{OUT(NOM)}$ = 2.65 V

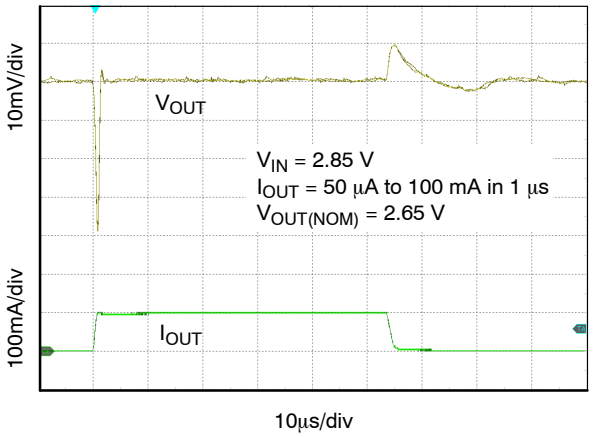


Figure 26. Load Transient Response 50 μA to 100 mA, $V_{OUT(NOM)}$ = 2.65 V

TYPICAL CHARACTERISTICS

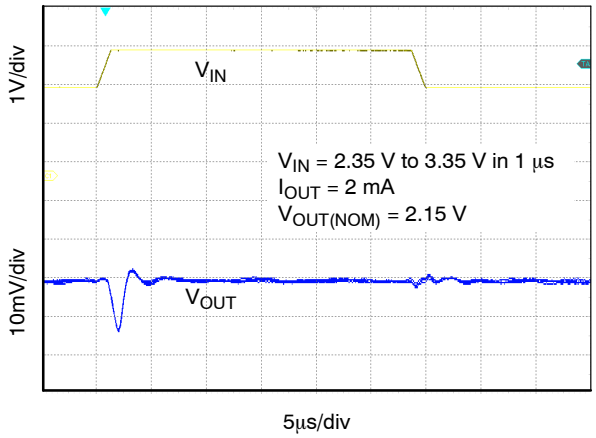


Figure 27. Line Transient Response, I_{OUT} = 2 mA

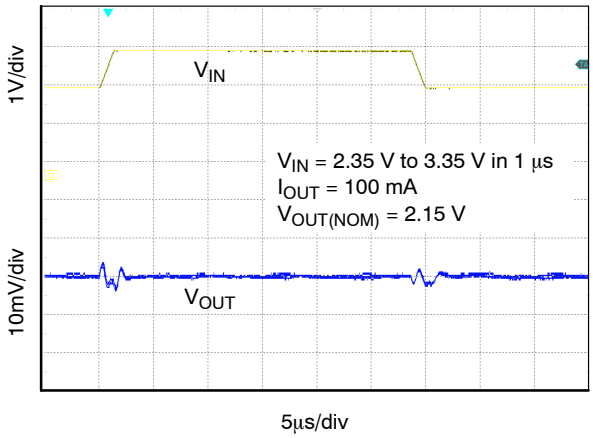


Figure 28. Line Transient Response, I_{OUT} = 100 mA

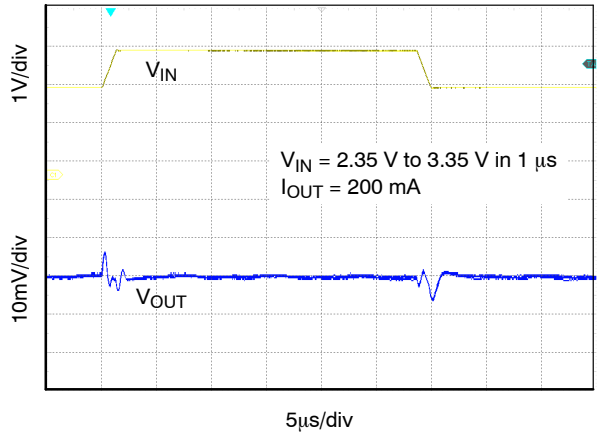


Figure 29. Line Transient Response, I_{OUT} = 200 mA

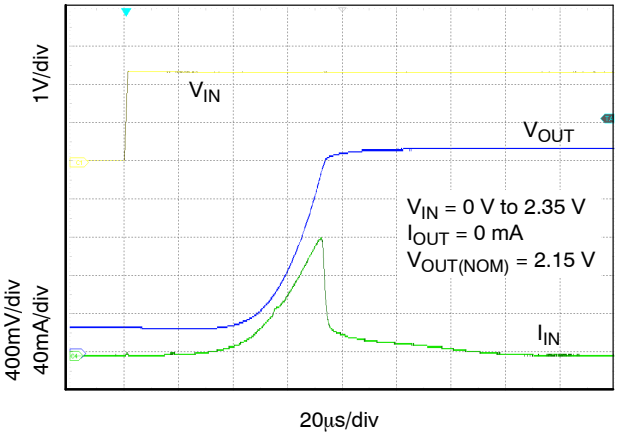


Figure 30. Start−up, I_{OUT} = 0 A

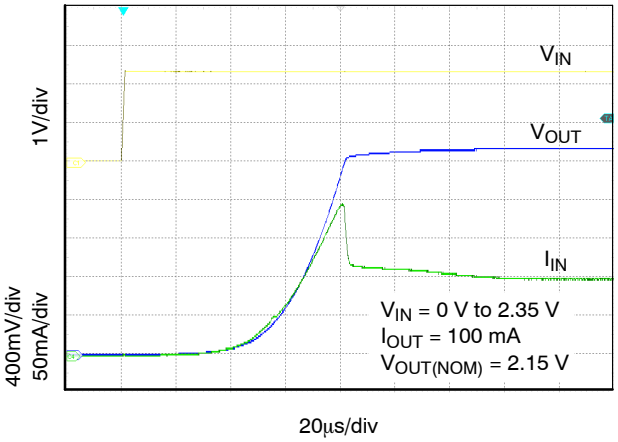


Figure 31. Start−up, I_{OUT} = 100 mA

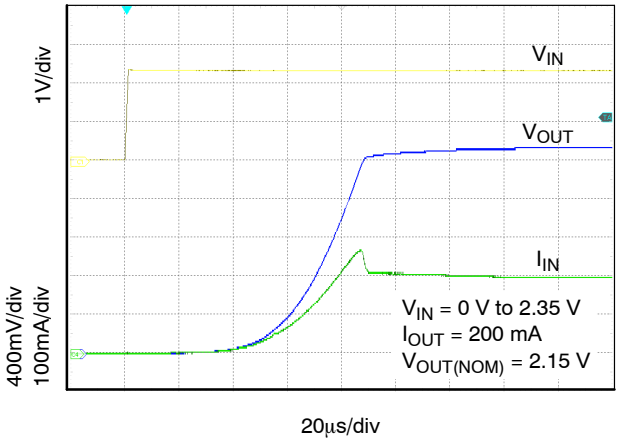


Figure 32. Start−up, I_{OUT} = 200 mA

TYPICAL CHARACTERISTICS

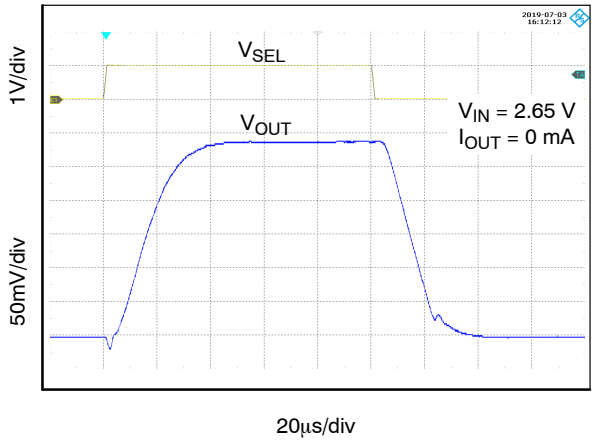


Figure 33. Selection Transient Response, $V_{OUT(NOM)}$ = 2.15 V / 2.45 V, I_{OUT} = 0 A

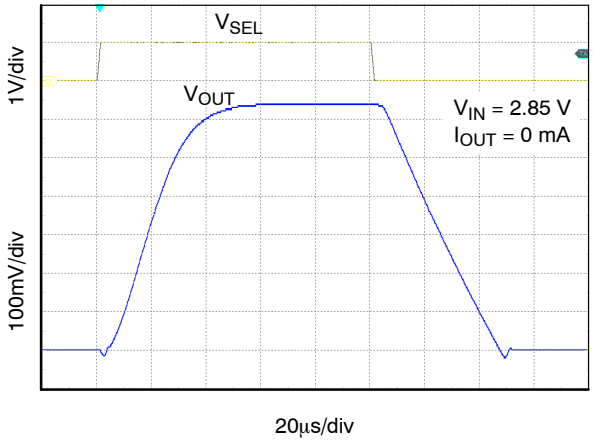


Figure 34. Selection Transient Response, $V_{OUT(NOM)}$ = 2.0 V / 2.65 V, I_{OUT} = 0 A

APPLICATION INFORMATION

General

The SCY99250 is a 200 mA dual selectable output voltage LDO with ultra-low input voltage operation capability. The device also offers superior low noise, Ultra High PSRR performance at very low dropout voltage. The SCY99250 with Ultra Low noise, very high PSRR and excellent dynamic response makes it ideal for Precision Analog and RF applications where Size and Low power are also critical. Always enabled upon valid input voltage eliminates the need for a dedicated EN pin which allows for an ultra-small footprint in a 4-pin WLCSP package. The SCY99250 is fully protected in case of current overload, output short circuit and overheating. The low quiescent current makes this device suitable for battery powered application such as cell phones, tablets and other.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary for ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Decoupling

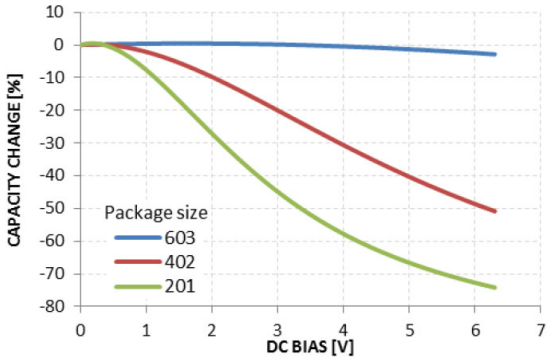


Figure 35. Capacity vs. DC Bias Voltage

The SCY99250 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The SCY99250 is designed to remain stable with minimum effective capacitance of 0.7 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias. Please refer to Figure 35. There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 1.6 Ω.

Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature. It is recommended to not exceed maximum value C_{OUT} = 4 μF for achievement of transition time 150 μs. SCY99250 has also Active Output Discharge which reacts to input voltage. If V_{IN} voltage is lower than 0.8 V Active Discharge is ON. If V_{IN} voltage is higher than 1.06 V Active Discharge is OFF.

Voltage Selection Operation

The SCY99250 uses the SEL pin to select between two output voltages on the Out Pin, V_{OUT1} and V_{OUT2}. If the SEL pin is Low (< 0.2 V) V_{OUT1} is selected and if SEL pin is high (> 0.7 V) V_{OUT2} would be selected at the Output. The output capacitor is internally discharged during transition time between V_{OUT2} to V_{OUT1} upon SEL pin toggling to achieve typically 150 μs with no load present at the output.

Output Current Limit

Output Current is internally limited within the IC to a typical 350 mA. The SCY99250 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 350 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (TSD − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (TSDU − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the SCY99250 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature

rise for the part. The maximum power dissipation the SCY99250 can handle is given by:

$$P_{D(MAX)} = \frac{[85°C - T_A]}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the SCY99250 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \cdot I_{GND} + I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(eq. 2)}$$

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The SCY99250 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad should be tied the shortest path to the GND pin.

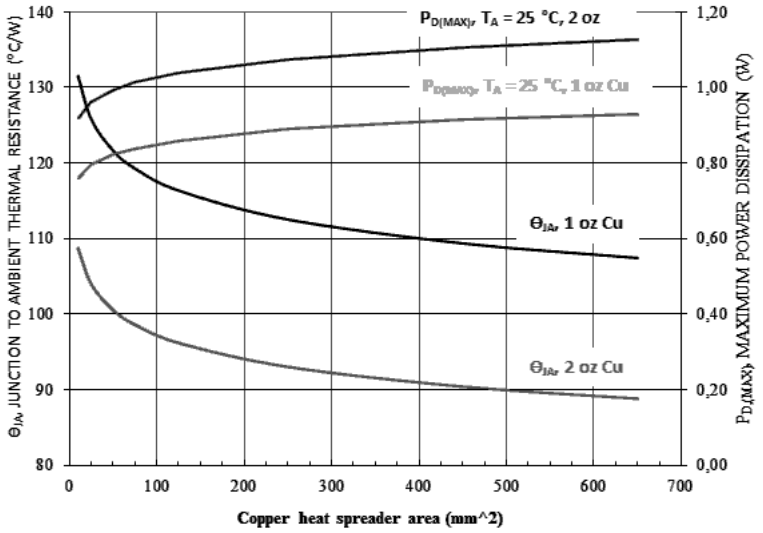


Figure 36. Θ_{JA} and $P_{D(MAX)}$ vs. PCB Cooper Area (CSP4)

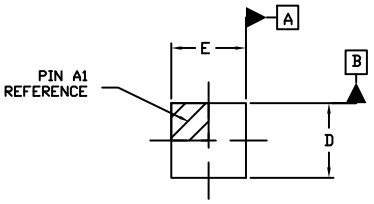
ORDERING INFORMATION

Device	Voltage Option OUT1/OUT2	Marking	Rotation	Description	Package	Shipping†
SCY99250CFCT210240T2G	2.1 V/2.4 V	4	180°	200 mA LDO, with Active Discharge Feature	WLCSP4 Case 567VS (Pb−Free) UBM: 200 μm Bump type: Sn Plate	5000 / Tape & Reel
SCY99250CFCT215245T2G	2.15 V/2.45 V	3				
SCY99250CFCT200265T2G	2.0 V/2.65 V	2				
SCY99250CFCT200280T2G (In Development)	2.0 V/2.8 V	5				
SCY99250CFCT220245T2G	2.2 V/2.45 V	A				
SCY99250CFCT190260T2G (In Development)	1.9 V/2.6 V	TBD	TBD			
SCY99250CFCT195215T2G (In Development)	1.95 V/2.15 V	6	180°			
SCY99250CFCT200220T2G (In Development)	2.0 V/2.2 V	P				
SCY99250CFCT200255T2G	2.0 V/2.55 V	Q				
SCY99250CFCS200265T2G	2.0 V/2.65 V	4	0°	200 mA LDO, with Active Discharge Feature	WLCSP4 Case 567XW (Pb−Free) UBM: 190 μm Bump type: SAC405 Ball drop	5000 / Tape & Reel
SCY99250CFCS200280T2G (In Development)	2.0 V/2.8 V	2	0°			
SCY99250CFCS215245T2G	2.15 V/2.45 V	5	0°			

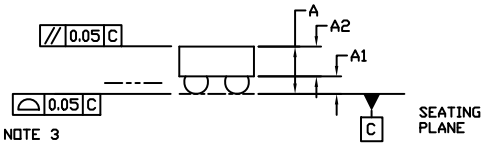
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

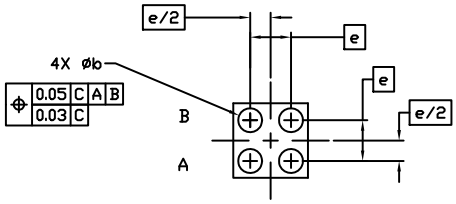
WLCSP4, 0.64x0.64x0.40
CASE 567XW
ISSUE A



TOP VIEW



SIDE VIEW

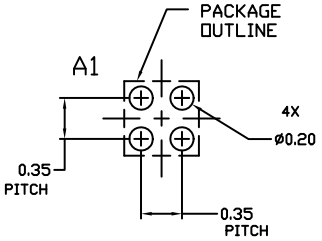


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C..

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.360	0.405	0.450
A1	0.130	0.150	0.170
A2	0.255 REF		
b	0.180	0.210	0.240
D	0.610	0.640	0.670
E	0.610	0.640	0.670
e	0.350 BSC		



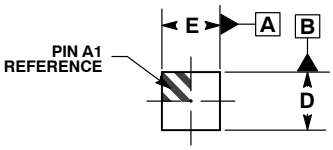
RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

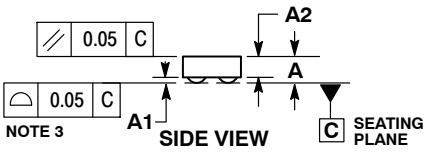
SCY99250

PACKAGE DIMENSIONS

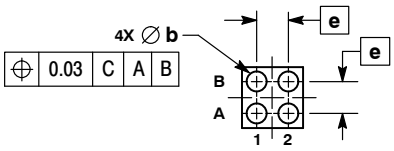
WLCSP4, 0.64x0.64x0.33
CASE 567VS
ISSUE O



TOP VIEW



SIDE VIEW

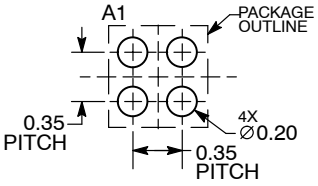


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	---	---	0.33
A1	0.04	0.06	0.08
A2		0.23 REF	
b	0.180	0.200	0.220
D	0.610	0.640	0.670
E	0.610	0.640	0.670
e		0.35 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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