Highly Integrated Secondary-Side Adaptive USB Type-C Charging Controller with USB-PD

FAN6392

The FAN6392 is a highly integrated, secondary−side power adaptor controller supporting USB Type−C, USB Power Delivery 2.0 and 3.0. It is included an autonomous USB PD state machine which is fully compliant with the latest USB PD 3.0 specification, minimizing design time and cost. Support for the latest Programmable Power Supply (PPS) rules allows for control of voltages from 3.3 V to 21 V and current limits from 1 A to 5 A to meet a wide range of applications and power levels.

To minimize BOM count, the FAN6392 includes internal synchronous rectifier (SR) control, an NMOS gate driver for VBUS load switch control, as well as Constant Voltage (CV) and Constant Current (CC) control blocks with adjustable internal references.

To ensure proper operation of the adaptor, various protections are integrated into the controller including output over−voltage protection, under−voltage protection, internal over−temperature protection, CC over voltage protection and VCONN over−current protection.

Features

- Supports USB PD2.0, 3.0 and PPS
- Integrated Synchronous Rectifier Control Circuit
- Constant Voltage (CV) and Constant Current (CC) Regulation with Two Operational Amplifiers of Open−Drain Type for Dual−Loop CV/CC Control
- Charge Pump Circuit to Enhance SR Driving Voltage for High Efficiency
- Small Current Sensing Resistor (5 mΩ) for High Efficiency
- N−Channel back to back MOSFET Control as a Load Switch
- Built−in Output Capacitor Bleeding Function for Fast Discharging
- Auto Re−start Protection Mode to Trigger Primary Controller's Protection
- Support Protections; Output Over−Voltage Protection, Under−Voltage Protection, Internal Over Temperature Protection, E−marked Cable Iconn Over Current Protection and CC lines Over Voltage Protection
- This is a Pb−Free Device

Typical Applications

- Battery Chargers for Smart Phones, Feature Phones and Tablet PCs
- AC−DC Adapters for Portable Devices that Require CV/CC Control

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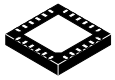
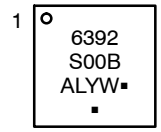


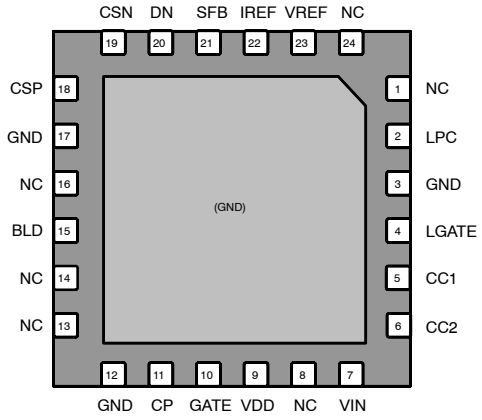
WQFN24, 4x4, 0.5P
CASE 510BE

MARKING DIAGRAM



6392S00B= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Bottom View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

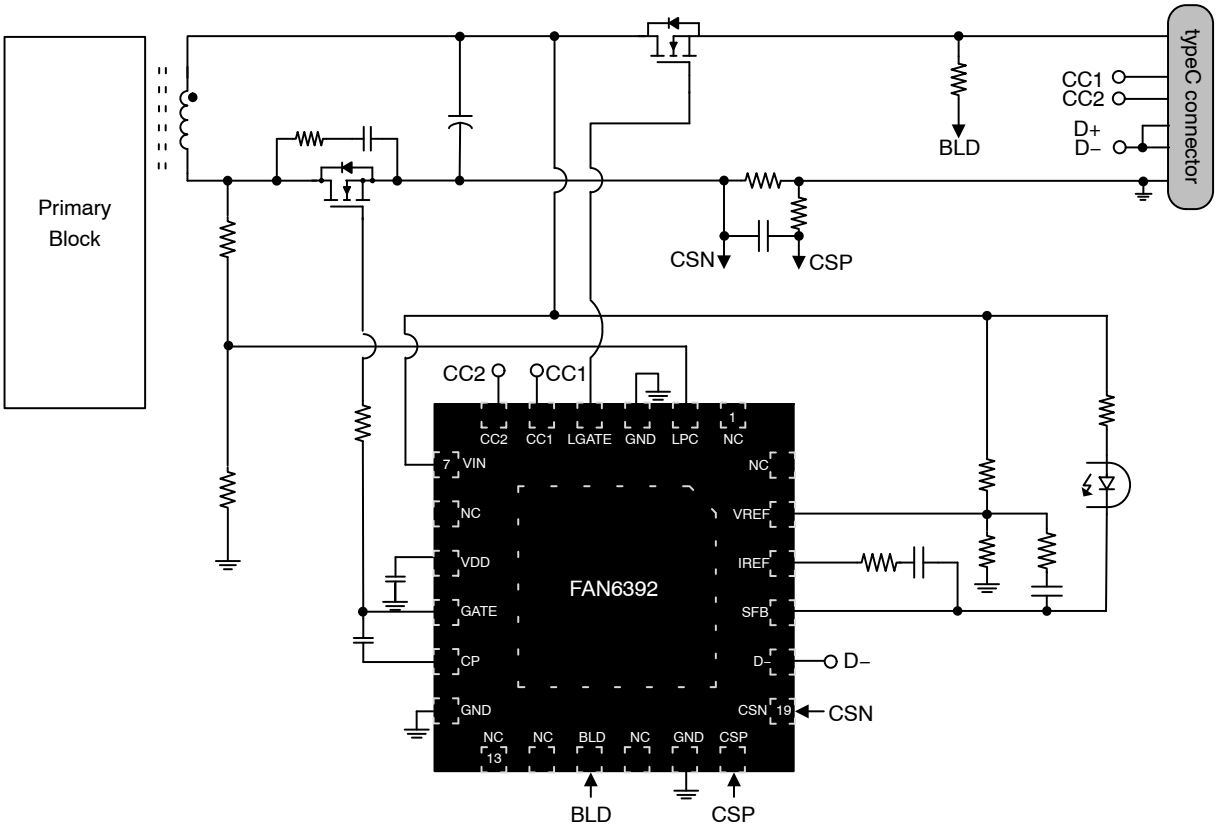


Figure 1. Application Schematic – FAN6392

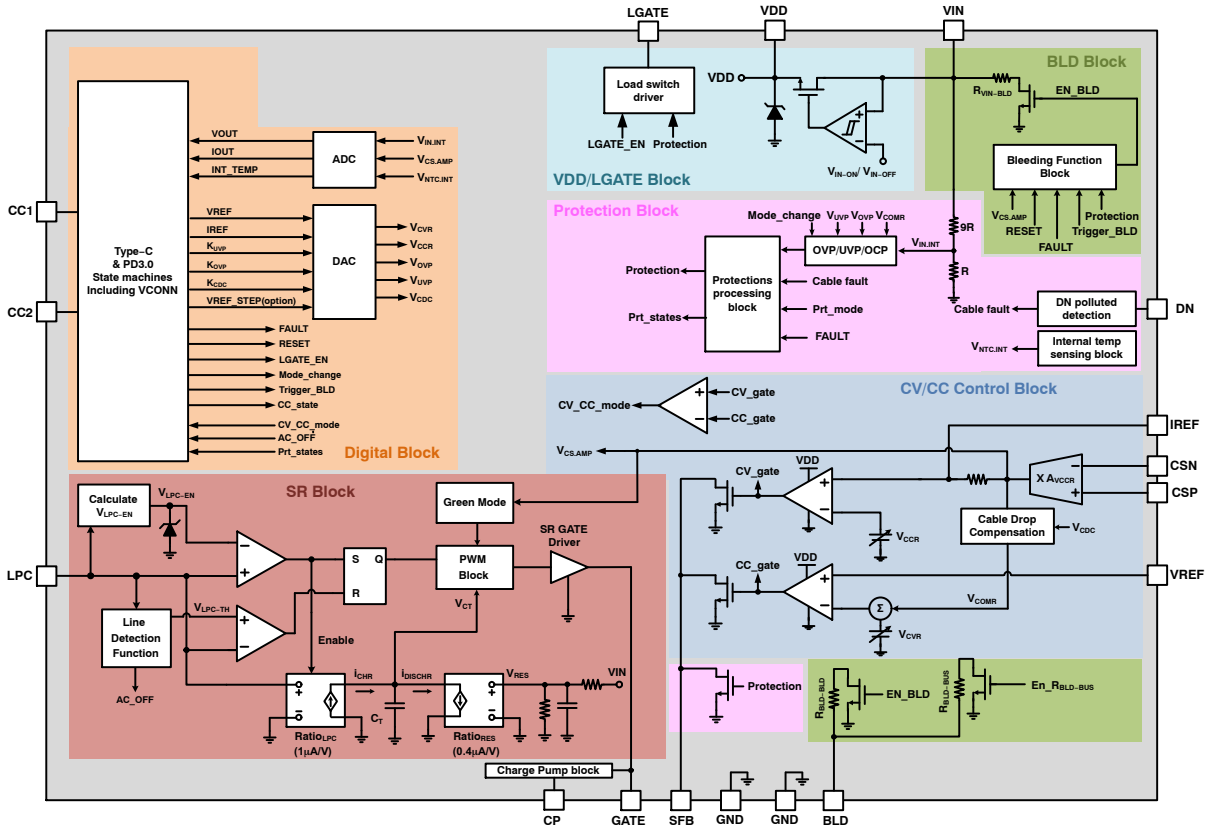


Figure 2. Block Diagram – FAN6392

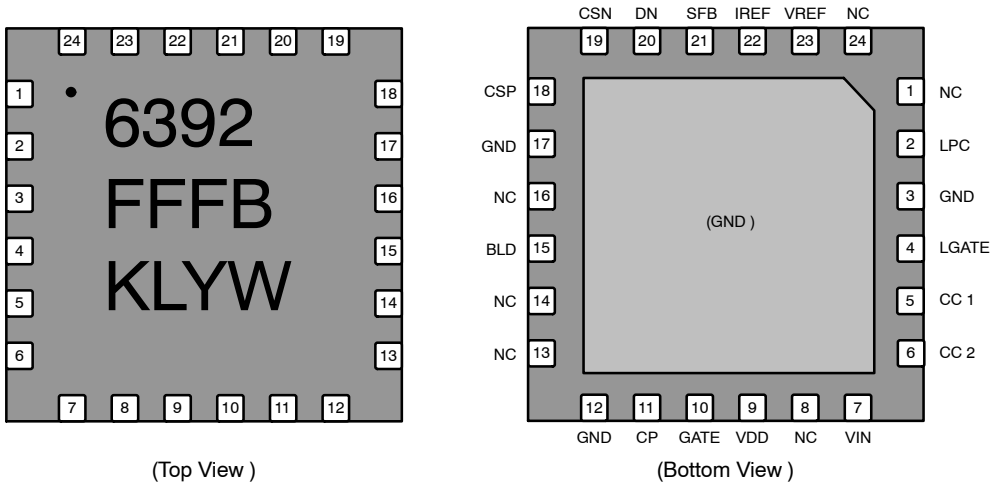


Figure 3. FAN6392 Pin Connections – WQFN24

PIN FUNCTION DESCRIPTION (WQFN24)

Pin No.	Pin Name	Description
1, 8, 13, 14, 16, 24	NC	No connection
2	LPC	SR control input signal. This pin is used to detect the voltage on the secondary winding during the on time period of the primary MOSFET
3	GND	Ground
4	LGATE	Load switch gate drive signal. This pin is tied to the gate of the load switch
5	CC1	Configuration Channel 1. This pin is used to detect USB Type−C devices and communicate over USB PD when applicable.
6	CC2	Configuration Channel 2. This pin is used to detect USB Type−C devices and communicate over USB PD when applicable.
7	VIN	Output voltage (Input voltage to the FAN6392). This pin is tied to the output of the adapter to monitor its output voltage and supply internal bias.
9	VDD	Internal supply voltage. This pin typically need to add 1 μF external capacitor.
10	GATE	Gate drive output. Totem−pole output to drive the external SR MOSFET.
11	CP	SR gate charge pump
12	GND	Ground
15	BLD	Bleeder pin. This pin is tied to VBUS after the load switch to discharge VBUS.
17	GND	Ground
18	CSP	Current sensing amplifier positive terminal. Connect this pin directly to the positive end of the current sense resistor with a short PCB trace.
19	CSN	Current sensing amplifier negative terminal. Connect this pin directly to the negative end of the current sense resistor with a short PCB trace.
20	DN	USB receptacle DN pin terminal connection.
21	SFB	Secondary Feedback. Common output of the dual OTA open drain operation amplifiers. Typically an opto−coupler is connected to this pin to provide feedback signal to the primary side PWM controller
22	IREF	Constant Current Amplifying Signal. The voltage level on this point is the amplified current sense signal. This pin is tied to the internal CC loop amplifier's non−inverting input terminal
23	VREF	Output Voltage Sensing Voltage. This pin is used for CV regulation, and it is tied to the internal CV loop amplifier non−inverting input terminal. It is tied to the output voltage resistor divider.

MAXIMUM RATINGS (Note 1, 2)

Symbol	Rating	Value	Unit
V_{IN}	VIN Pin Input Voltage	−0.3 to 26	V
V_{SFB}	SFB Pin Input Voltage	−0.3 to 26	V
V_{BLD}	BLD Pin Input Voltage	−0.3 to 26	V
V_{LGATE}	LGATE Pin Input Voltage	−0.3 to 31	V
V_{DD}	VDD Pin Input Voltage	−0.3 to 6	V
V_{IREF}	IREF Pin Input Voltage	−0.3 to 6	V
V_{VREF}	VREF Pin Input Voltage	−0.3 to 6	V
V_{CSP}	CSP Pin Input Voltage	−0.3 to 6	V
V_{CSN}	CSN Pin Input Voltage	−0.3 to 6	V
V_{LPC}	LPC pin Input Voltage	−0.3 to 6.5	V
V_{GATE}	GATE Pin Input Voltage	−0.3 to 6.5	V
V_{DN}	DN Pin Input Voltage	−0.3 to 6	V
V_{CC1}	CC1 Pin Input Voltage	−0.3 to 6	V
V_{CC2}	CC2 Pin Input Voltage	−0.3 to 6	V
V_{CP}	CP Pin Input Voltage	−0.3 to 6	V
P_D	Power Dissipation (T_A = 25°C)	0.86	W
T_J	Operating Junction Temperature	−40 to 150	°C
T_{STG}	Storage Temperature Range	−40 to 150	°C
TL	Lead Temperature, (Soldering, 10 Seconds)	260	°C
ESD_{HBM}	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012 (Note 3)	2.0	kV
ESD_{CDM}	Charged Device Model, JESD22−C101 (Note 3)	0.5	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to the GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS−001−2012 and JESD 22−C101.

THERMAL CHARACTERISTICS (Note 4)

Symbol	Rating	Value	Unit
	Thermal Characteristics,		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Air	122	
$R_{\psi JT}$	Thermal Reference, Junction−to−Top	5	

4. T_A = 25°C unless otherwise specified.

RECOMMENDED OPERATING CONDITIONS

Symbol	Rating	Min	Max	Unit
V_{in}	Input Voltage	−	20	V
I_{out}	Output Current	−	5	A
V_{out}	Adjustable Output Voltage (Adjustable Version Only)	−	20	V
T_A	Ambient Temperature	−	80	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDD SECTION						
$V_{DD-valid}$	Turn−On Valid Threshold Voltage (Note 5)		2.6	–	–	V
V_{DD}	VIN Operating Voltage at 20 V	V_{IN} = 20 V, I_{VDD} = 0 mA, Vconn enable	4.750	5.125	5.500	V
I_{DD}	VDD Source Current	V_{IN} = 3.3 V, V_{DD} = 2.9 V	10	–	–	mA
VIN SECTION						
V_{IN-OP}	Continuous Operating Voltage (Note 5)		–	–	22.5	V
$I_{IN-OP-5V}$	Operating Supply Current at 5 V	V_{IN} = 5 V, V_{CS} = −25 mV, Rcs = 5 mΩ	–	8	–	mA
$I_{IN-OP-20V}$	Operating Supply Current at 20 V (Note 5)	V_{IN} = 20 V, V_{CS} = −25 mV, Rcs = 5mΩ	–	8	–	mA
V_{IN-ON}	Turn−On Threshold Voltage	V_{IN} Increases	3.1	3.3	3.5	V
V_{IN-OFF}	Turn−Off Threshold Voltage	V_{IN} Decreases after V_{IN} = V_{IN-ON}	2.896	2.992	3.088	V
$V_{IN-OFF-HYS}$	Hysteresis of Turn−Off Threshold Voltage (Note 5)	V_{IN} Decreases after V_{IN} = V_{IN-ON}	–	0.3	–	V
$I_{IN-Green}$	Green Mode Operating Supply Current	V_{IN} = 5.2 V(default), V_{CS} = 0 mV excluding I_{P-CC1} and I_{P-CC2} when ambient temp = 25°C	–	–	1.3	mA
VIN−UVP SECTION						
K_{IN-UVP}	Ratio V_{IN} Under−Voltage−Protection to V_{IN}		73.87	76.14	78.4	%
$t_{D-VIN-UVP}$	CC Mode UVP Debounce Time		12	15	18	ms
$t_{BNK-UVP}$	UVP Blanking Time during Mode Change from Lower Vout to Higher Vout	Whenever does mode change from lower Vout to higher Vout	160	200	240	ms
VIN−OVP SECTION						
K_{IN-OVP}	Ratio V_{IN} Over−Voltage−Protection to V_{IN}		112.7	114.9	117.0	%
$V_{IN-OVP-MAX}$	V_{IN} Maximum Over−Voltage−Protection (Note 5)		23.5	24.5	25.5	V
t_{D-OVP}	OVP Debounce Time		18	29	40	μs
$t_{BNK-OVP1}$	OVP Blanking Time during Mode Change from Higher Vout to Lower Vout 1 (Note 5)	Disabling OVP & SR Gate. Vstep ≤ 0.5 V, Vbus ≥ 13 V	–	7	–	ms
$t_{BNK-OVP2}$	OVP Blanking Time during Mode Change from Higher Vout to Lower Vout 2 (Note 5)	Disabling OVP & SR Gate. Vstep ≤ 0.5 V, Vbus < 13 V	–	19	–	ms
$t_{BNK-OVP3}$	OVP Blanking Time during Mode Change from Higher Vout to Lower Vout 3 (Note 5)	Disabling OVP & SR Gate. Vstep > 0.5 V, Vbus ≥ 13 V	–	56	–	ms
$t_{BNK-OVP4}$	OVP Blanking Time during Mode Change from Higher Vout to Lower Vout 4	Disabling OVP & SR Gate. Vstep > 0.5 V, Vbus < 13 V	160	200	240	ms
CONSTANT CURRENT SENSING SECTION						
A_{V-CCR}	Current−Sense Amplifier Gain (Note 5)	R_{CS} = 5 mΩ	–	40	–	V/V
$I_{CS-3.00A\_PDO}$	Current threshold on sensing resistor between CSP and CSN at $I_{OUT.CC}$ = 3.0 A	VIN = 5 V, USB PD PDO mode	3.09	3.21	3.33	A
$I_{CS-2.77A\_PDO}$	Current threshold on sensing resistor between CSP and CSN at $I_{OUT.CC}$ = 2.77 A	VIN = 9 V, USB PD PDO mode	2.84	2.96	3.08	A

ELECTRICAL CHARACTERISTICS (V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
CONSTANT CURRENT SENSING SECTION						
$I_{CS-3.00A\_APDO}$	Current threshold on sensing resistor \ between CSP and CSN at $I_{OUT.CC}$ = 3.00 A	VIN = 3.3 V and 5.0 V, USB PD APDO mode	2.88	3.00	3.12	A
$I_{CS-2.77A\_APDO}$	Current threshold on sensing resistor between CSP and CSN at $I_{OUT.CC}$ = 2.77 A	VIN = 9 V, USB PD APDO mode	2.66	2.77	2.88	A
$I_{CS-STEP}$	Current threshold on sensing resistor between CSP and CSN at $\Delta I_{OUT.CC}$ = 50 mA (Note 5)	ΔI_{OTYP} = 50 mA	48	50	52	mA
$T_{OCP-Debounce}$	OCP Debounce Time (Note 5)		50	60	70	ms
OUTPUT CURRENT SENSING SECTION						
$I_{CS-EN-BLD}$	Current threshold on sensing resistor between CSP and CSN for enabling bleeding during mode change		–	–	450	mA
$T_{CS-EN-BLD}$	Debounce time for enabling bleeding during mode change		–	0.6	1.0	ms
CONSTANT VOLTAGE SENSING SECTION						
$V_{CVR-3.3V}$	Reference Voltage at 3.3 V	V_{IN} = 3.3 V, V_{CS} = 0 V	0.317	0.327	0.337	V
$V_{CVR-5.2V}$	Reference Voltage at 5.2 V	V_{IN} = 5.2 V, V_{CS} = 0 V	0.495	0.511	0.527	V
V_{CVR-9V}	Reference Voltage at 9 V	V_{IN} = 9 V, V_{CS} = 0 V	0.854	0.881	0.908	V
$V_{CVR-STEP-20mV}$	Reference Voltage of 20 mV step	ΔV_{IN} = 20 mV, V_{CS} = 0 V	1.885	1.945	2.005	mV
CABLE DROP COMPENSATION SECTION						
$V_{COMR-CDC}$	Cable Compensation Voltage on V_{CVR} for V_{OUT} = 110 mV/A	R_{CS} = 5 mΩ, V_{CS} = −5 mV	10.0	11.0	12.0	mV
FEEDBACK SECTION						
$I_{SFB-Sink-MAX}$	SFB Pin Maximum Sink Current		2	–	–	mA
BLEEDER SECTION						
$I_{VIN\ -Sink}$	VIN Pin Sink Current when Bleeding (Note 5)	Bleeding current on VIN at VIN = 20 V	300	–	–	mA
$I_{BLD\ -Sink}$	BLD Pin Sink Current through when Bleeding (Note 5)	Bleeding current on BLD at VIN = 20 V	250	–	–	mA
t_{BLD1}	Enable bleeder time 1 (Note 5)	Disabling OVP & SR Gate. Vstep ≤ 0.5 V, Vbus ≥ 13	–	7	–	ms
t_{BLD2}	Enable bleeder time 2 (Note 5)	Disabling OVP & SR Gate. Vstep ≤ 0.5 V, Vbus < 13	–	19	–	ms
t_{BLD3}	Enable bleeder time 3 (Note 5)	Disabling OVP & SR Gate. Vstep > 0.5 V, Vbus ≥ 13	–	56	–	ms
t_{BLD4}	Enable bleeder time 4	Disabling OVP & SR Gate. Vstep > 0.5 V, Vbus < 13	160	200	240	ms
PROTECTION OPERATION SPECIFICATION SECTION						
$V_{LATCH-OFF}$	Output Voltage Releasing Latch Mode	V_{IN} < $V_{LATCH-OFF}$, at −5°C and 85°C	–	–	1.55	V
$t_{TwoSecondAR.}$	Time Duration Disabling Load Switch (Design in digital core)	OVP, UVP, OCP, Cable Fault, CC OVP	1.8	2	2.2	sec

ELECTRICAL CHARACTERISTICS (V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DN POLLUTE DETECTION(CABLE FAULT)						
$V_{IN-EN-DN-POL}$	Enable DN Pollution Detection VIN Voltage	Increasing V_{IN}	–	4.4	–	V
$I_{POL-DET}$	D− Line Pollution Detection Current Source (Note 5)	At 3.5 V ≥ V_{DN} ≥ 0 V	–	500	–	μA
$R_{POL(max)}$	Detectable Maximum D− Line Impedance	At 3.5 V ≥ V_{DN} ≥ 0 V, R_{DN-GND} = 1 kΩ & R_{BUS-DN} = 1 kΩ. Find $R_{POL(max)}$ with decreasing R_{DN-GND}	200	–	410	Ω
$t_{POL-DET}$	Pollution Detection Time	After V_{IN} > V_{IN-ON}	10	–	–	μs
$t_{POL-DET-Period1}$	Period of Pollution Detection when TA alone	VCC1 / VCC2 > V_{RD} (2.6 V)	1.8	2.2	2.6	sec
$t_{POL-DET-Period2}$	Period of Pollution Detection during tCC−Debounce	VCC1 / VCC2 within V_{RA} and V_{RD} during tCC−Debounce	7.2	8.0	8.8	ms
V_{DN-OVP}	DN Pin Over Voltage Protection	Excepting $T_{POL-DET}$	4.1	4.35	4.6	V
$t_{DN-DP-OVP-Debounce}$	DP/DN Pin OVP Debounce Time	V_{DN} > V_{DN-SD}	1.05	3.0	4.15	ms
TYPE−C SECTION						
$I_{P-CC1-330}$	330 μA Source Current on CC1 Pin	V_{IN} = 5 V, V_{CC1} = 0 V	302	330	358	μA
$I_{P-CC1-180}$	180 μA source current on CC1 pin	V_{IN} = 5 V, V_{CC1} = 0 V	164	180	196	μA
$I_{P-CC2-330}$	330 μA Source Current on CC2 Pin	V_{IN} = 5 V, V_{CC2} = 0 V	302	330	358	μA
$I_{P-CC2-180}$	180 μA source current on CC2 pin	V_{IN} = 5 V, V_{CC2} = 0 V	164	180	196	μA
$Z_{OPEN-CC1}$	Input Impedance on CC1 Pin	V_{IN} = 0 V, Sourcing 330 μA on CC1	126	–	–	kΩ
$Z_{OPEN-CC2}$	Input Impedance on CC2 Pin	V_{IN} = 0 V, Sourcing 330 μA on CC2	126	–	–	kΩ
V_{RA-CC1}	Ra Impedance Detection Threshold on CC1 Pin	V_{IN} = 5 V, V_{CC2} = 0 V, Decreasing V_{CC1}	0.75	0.80	0.85	V
V_{RA-CC2}	Ra Impedance Detection Threshold on CC2 Pin	V_{IN} = 5 V, V_{CC1} = 0 V, Decreasing V_{CC2}	0.75	0.80	0.85	V
V_{RD-CC1}	Rd Impedance Detection Threshold on CC1 Pin	V_{IN} = 5 V, V_{CC2} = 0 V, Increasing V_{CC1}	2.45	2.60	2.75	V
V_{RD-CC2}	Rd Impedance Detection Threshold on CC2 Pin	V_{IN} = 5 V, V_{CC1} = 0 V, Increasing V_{CC2}	2.45	2.60	2.75	V
R_{a-CC1}	Discharging resistor on CC1 pin (Note 5)		–	–	5.1	kΩ
R_{a-CC2}	Discharging resistor on CC2 pin (Note 5)		–	–	5.1	kΩ
$t_{CCDebounce}$	UFP Attachment Debounce Time	V_{IN} = 5 V, V_{CC2} = 0 V, Increasing V_{CC1}	100	150	200	ms
$V_{LGATE-3.3V}$	Load SW Gate High Voltage at 3.3 V	V_{IN} = 3.3 V	5.3	–	–	V
$V_{LGATE-5V}$	Load SW Gate High Voltage at 5 V (Note 5)	V_{IN} = 5 V	8.5	–	–	V
$V_{LGATE-9V}$	Load SW Gate High Voltage at 9 V (Note 5)	V_{IN} = 9 V	12.5	–	–	V
$V_{LGATE-11V}$	Load SW Gate High Voltage at 11 V (Note 5)	V_{IN} = 11 V	14.5	–	–	V
V_{CONN}	V_{CONN} supply voltage		2.4	–	5.5	V
I_{CONN_OCP}	V_{CONN} OCP current		50	–	–	mA
t_{VCONN_OCP}	V_{CONN} OCP debounce time		2.1	3.63	5.15	ms
Iv_{CONN}	V_{CONN} supply current	VIN = 4.75 V, Vconn = 3 V	34	–	–	mA
$V_{CC1-OVP}$	CC_1 Pin Over−Voltage Protection		5.6	5.8	6.0	V

ELECTRICAL CHARACTERISTICS (V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
TYPE−C SECTION						
$V_{CC2-OVP}$	CC_2 Pin Over−Voltage Protection		5.6	5.8	6.0	V
$t_{CC-OVP-Debounce}$	CC_1/CC_2 OVP Debounce Time		−	−	100	μs
Vsafe0V	Vsafe0V safe operating voltage at “zero volts”		0.66	0.73	0.80	V
SR GATE OUTPUT DRIVER SECTION						
V_{OL}	Output Voltage Low	V_{IN} = 5 V, I_{GATE} = 50 mA	−	0.16	0.25	V
V_{OH}	Output Voltage High (Note 5)	V_{IN} = 3.3 V, C_{iss} = 4.7 nF, C_p = 4.7 nF	4.0	−	−	V
V_{CP-EN}	VIN Threshold to Enable Charge Pump (Note 5)		−	4.2	−	V
t_R	Rising Time (Note 5)	V_{IN} = 5 V, C_{iss} = 4.7 nF, C_p= 2.2 nF GATE = 1 V~4 V	−	41	−	ns
t_F	Falling Time (Note 5)	V_{IN} = 5 V, C_{iss} = 4.7 nF, C_p = 2.2 nF GATE = 4 V~1 V	−	31	−	ns
$t_{PD-HIGH-LPC}$	Propagation Delay to OUT High (LPC Trigger) (Note 5)	V_{IN} = 5 V, GATE = 1 V	−	44	−	ns
$t_{PD-LOW-LPC}$	Propagation Delay to OUT Low (LPC Trigger) (Note 5)	V_{IN} = 5 V, GATE = 4 V	−	30	−	ns
$t_{INHIBIT}$	Gate Inhibit Time (Note 5)		−	1.4	−	μs
INTERNAL RES SECTION						
K_{RES}	Internal RES Ratio (Note 5)	V_{IN} = V_{IN-OFF}~11 V	−	0.180	−	V/V
$Ratio_{LPC-RES}$	Ratio between V_{LPC} & V_{RES}	V_{IN} = 5 V, F_{LPC} = 50 kHz, K_{RES} = 0.180	3.30	3.47	3.64	
$K_{VIN-DROP}$	VIN Dropping Protection Ratio with Two Cycle	LPC Width = 5 μs, V_{IN} = 5 V to 3.5 V	60	70	80	%
$t_{VIN-Debounce}$	Debounce time for noise immunity on VIN (Note 5)		1	2	3	μs
t_{SR-OFF}	Debounce Time for Disable SR when VIN Dropping Protection		3.0	6.5	10.0	ms
LPC SECTION						
V_{LPC}	Linear Operation Range of LPC Pin Voltage (Note 5)	V_{IN-OFF} < V_{IN} ≤ 5 V	0.4	−	3.6	V
$I_{LPC-SINK}$	LPC Sink Current (Note 5)	V_{LPC} = 1 V	−	100	−	nA
$V_{LPC-HIGH-H-5V}$	SR Enabled Threshold Voltage @ High−Line	$V_{LPC-HIGH-H-5V}$ = $V_{LPC-TH-H-5V}$ / 0.875	0.942	1.069	1.197	V
$V_{LPC-HIGH-H-9V}$	SR Enabled Threshold Voltage @ High−Line	$V_{LPC-HIGH-H-9V}$ = $V_{LPC-TH-H-9V}$ / 0.875	1.061	1.196	1.332	V
$V_{LPC-HIGH-L-5V}$	SR Enabled Threshold Voltage @ Low−Line	$V_{LPC-HIGH-L-5V}$ = $V_{LPC-TH-L-5V}$ / 0.875	0.442	0.496	0.550	V
$V_{LPC-HIGH-L-9V}$	SR Enabled Threshold Voltage @ Low−Line	$V_{LPC-HIGH-L-9V}$ = $V_{LPC-TH-L-9V}$ / 0.875	0.561	0.584	0.685	V
$V_{LINE-H-5V}$	Low−to−High Line Threshold Voltage on LPC Pin	Spec. = (0.70 + 0.02 * V_{IN}) * 2, V_{IN} = 5 V	1.46	1.60	1.74	V
$V_{LINE-L-5V}$	High−to−Low Line Threshold Voltage on LPC Pin	Spec. = (0.65 + 0.02 * V_{IN}) * 2, V_{IN} = 5 V	1.37	1.50	1.63	V
$V_{LINE-HYS-5V}$	Line Change Threshold Hysteresis	$V_{LINE-HYS-5V}$ = $V_{LINE-H-5V}$ − $V_{LINE-L-5V}$		0.1		V
$V_{LINE-H-9V}$	Low−to−High Line Threshold Voltage on LPC Pin	Spec. = (0.70 + 0.02 * V_{IN}) * 2, V_{IN} = 9 V	1.62	1.76	1.90	V

ELECTRICAL CHARACTERISTICS (V_{IN} = 5 V, LPC = 1.25 V, LPC width = 2 μs at T_J = −40~125°C, F_{LPC} = 100 kHz, unless otherwise specified.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
LPC SECTION						
$V_{LINE-L-9V}$	High−to−Low Line Threshold Voltage on LPC Pin	Spec. = (0.65 + 0.02 * V_{IN}) * 2, V_{IN} = 9 V	1.53	1.66	1.79	V
$V_{LINE-HYS-9V}$	Line Change Threshold Hysteresis	$V_{LINE-HYS-9V}$ = $V_{LINE-H-9V}$ − $V_{LINE-L-9V}$	−	0.1	−	V
$V_{LPC-CLAMP-H}$	Higher Clamp Voltage		5.4	6.2	7.0	V
$V_{LPC-DIS}$	LPC Threshold Voltage to Disable SR Gate Switching	V_{IN} = 5 V, LPC = 3 V ↑	V_{IN} − 0.6	−	−	V
$t_{LPC-LH-debounce}$	Line Change Debounce Time from Low−Line to High−Line	Counts for LPC falling < $V_{LPC-TH-L-5V}$	9	21	33	ms
$t_{LPC-HL-debounce}$	Line Change Debounce from High−Line to Low−Line (Note 5)		−	15		μs
$t_{LPC-EN-H}$	Minimum LPC Time to Enable the SR Gate @ High−Line	V_{LPC} = 2.5 V	210	285	360	ns
$t_{LPC-EN-L}$	Minimum LPC Time to Enable the SR Gate @ Low−Line	V_{LPC} = 1.25 V	540	705	870	ns
$T_{reverse-debounce}$	Reverse Current Mode Entry Debounce Time	V_{IN} = 5 V, V_{LPC} = 0 V	210	400	590	ms
$I_{OP.reverse}$	Operating Current during Reverse Current Mode	V_{IN} = 5 V, V_{LPC} = 0 V	−	−	2.4	mA
BMC TRANSMITTER						
t_{UI}	Unit internal	1 / fBitRate	3.03	3.33	3.70	μs
$t_{Rise-TX}$	Rise time	C_{VDD} = 4.7 μF	300	500	700	ns
$t_{Fall-TX}$	Fall time	C_{VDD} = 4.7 μF	300	500	700	ns
zDriver	Transmitter output impedance	Transmitter output impedance at Niquist frequency of USB2.0 low speed (750 kHz) while Source driving the CC line	33	−	75	Ω
$n_{TransitionCount}$	Transitions for signal detect		3	−	−	
$t_{TransitionWindow}$	Time window for detecting non−idle		12	−	20	μs
$t_{RxFilter}$	Rx bandwidth limiting filter		100	−	−	ns
zBmcRx	Receiver Input Impedance		1	−	−	MΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by Design

TYPICAL CHARACTERISTICS

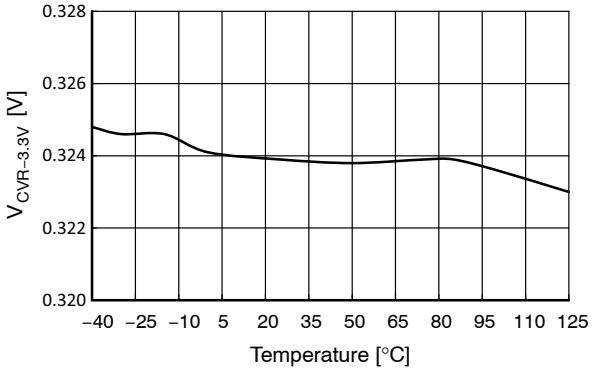


Figure 4. $V_{CVR-3.3V}$ vs. Temperature

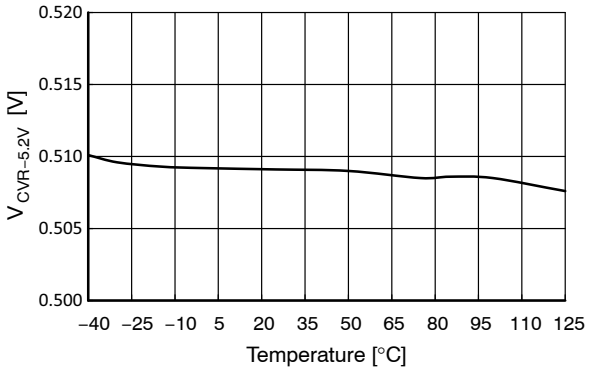


Figure 5. $V_{CVR-5.2V}$ vs. Temperature

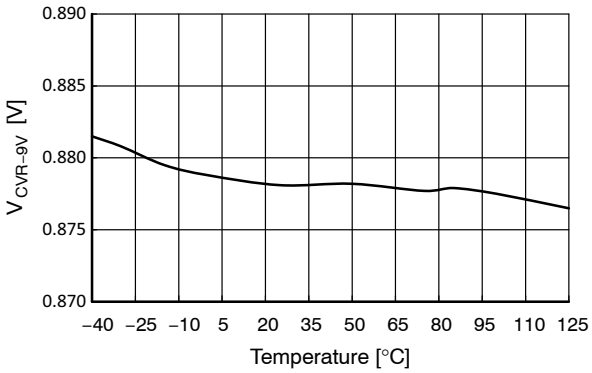


Figure 6. V_{CVR-9V} vs. Temperature

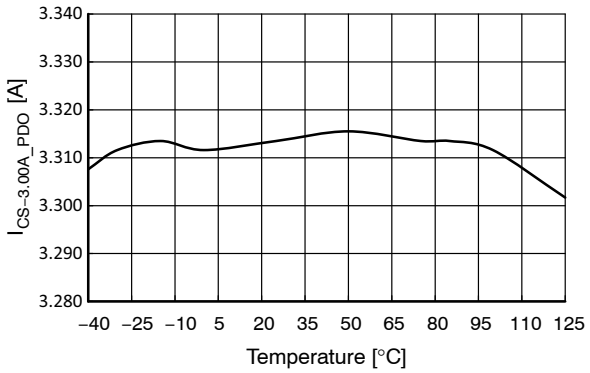


Figure 7. $I_{CS-3.00A\_PDO}$ vs. Temperature

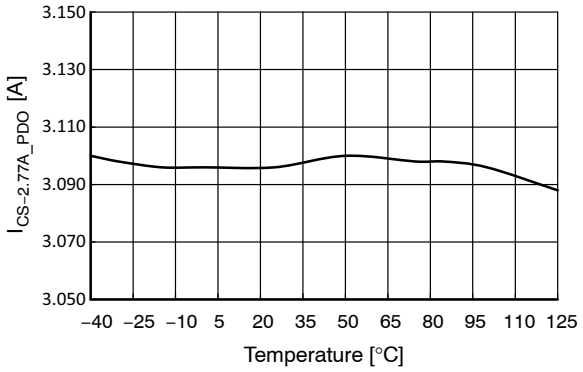


Figure 8. $I_{CS\_2.77A\_PDO}$ vs. Temperature

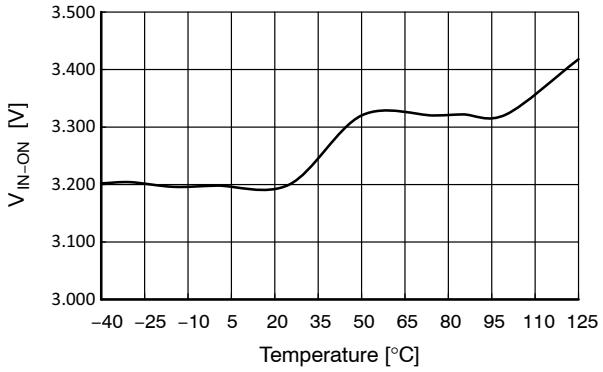


Figure 9. V_{IN-ON} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

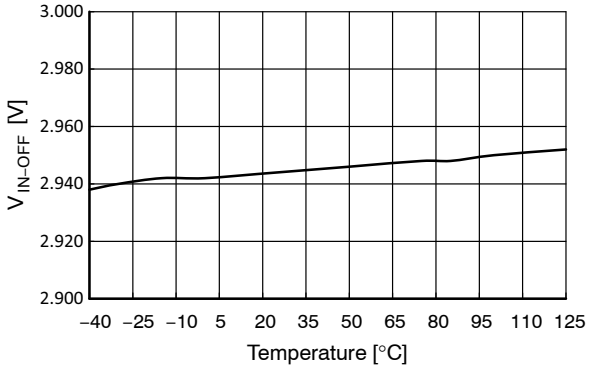


Figure 10. V_{IN-OFF} vs. Temperature

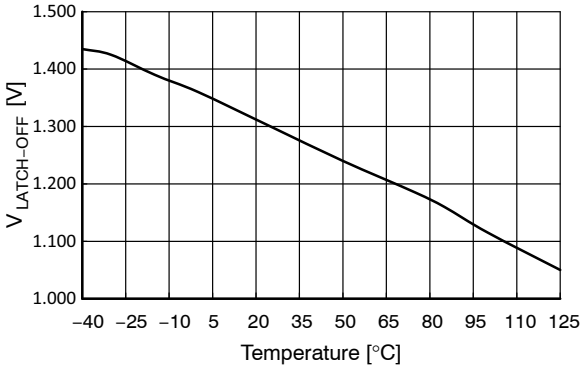


Figure 11. $V_{LATCH-OFF}$ vs. Temperature

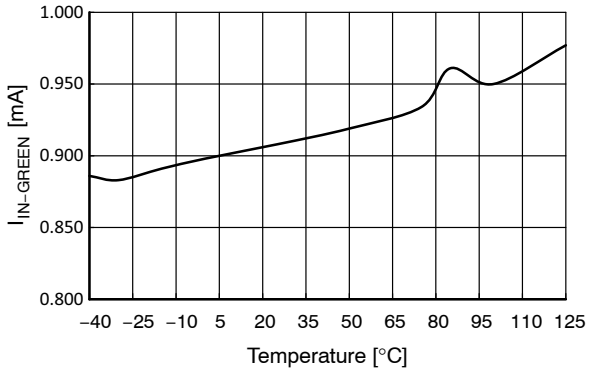


Figure 12. I_{IN_GREEN} vs. Temperature

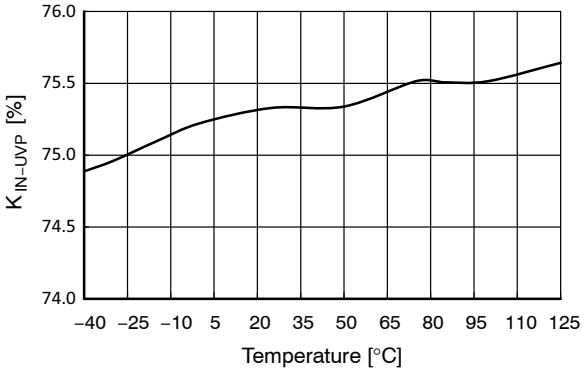


Figure 13. K_{IN-UVP} vs. Temperature

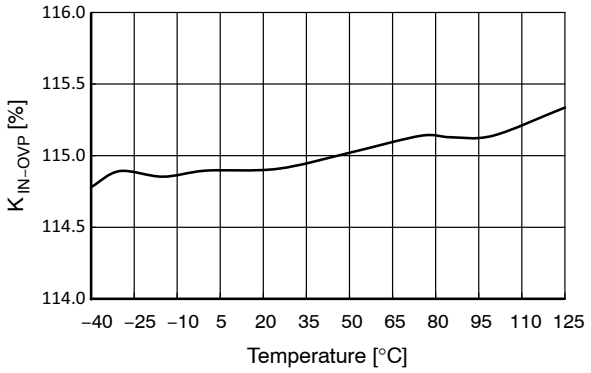


Figure 14. K_{IN-OVP} vs. Temperature

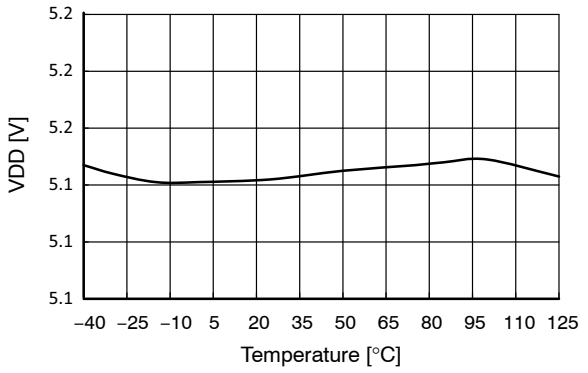


Figure 15. V_{DD} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

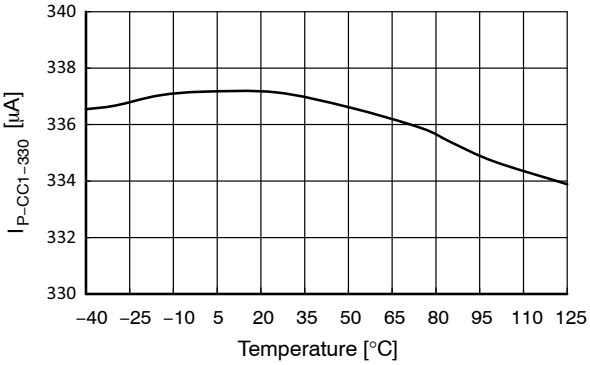


Figure 16. $I_{P-CC1-330}$ vs. Temperature

APPLICATIONS INFORMATION

USB Type−C Support

The USB Type−C specification defines CC lines (CC1 and CC2) to detect the orientation and roles of a USB Port pair (Source and Sink roles). A source device will provide pull−up currents on the CC lines and the sink will provide a pull−down resistance in order to allow detection of the other when the two are attached. When there is no device attached to either the source or sink device, VBUS must not be powered and should be under 0.8 V (Max). The FAN6392 operates as a source−only device and provides control of an NMOS load switch to isolate VIN from VBUS to ensure that VBUS can be discharged completely when required.

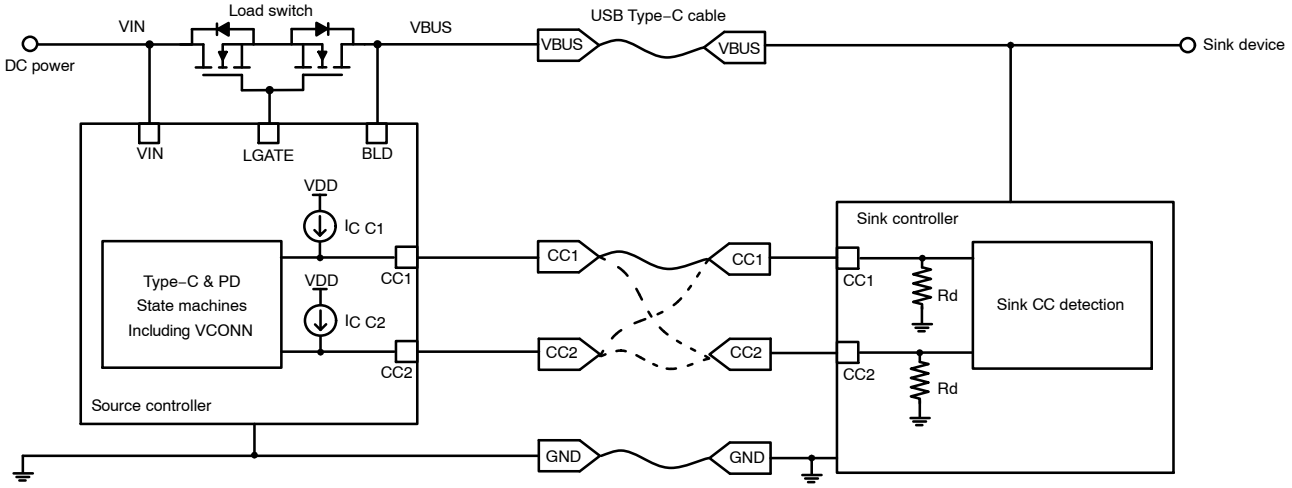


Figure 17. Source only Device Connecting to Sink Device through Type C Cable

Figure 17 shows a USB Source connected to a USB Sink with a USB Type−C cable. Since there is only one CC signal in a standard USB Type−C cable, one of pull−ups in the USB Source (I_{P-CC1} and I_{P-CC2}) will be terminated with the Rd to ground in the USB Sink, causing a fixed voltage to be developed across the 5.1 kΩ pull−down. The FAN6392 monitors the CC line voltages to decide if a Sink is attached or not and the orientation of the USB Type−C cable. If the V_{Rd} voltage is within the attach threshold for $t_{CCDebonce}$ according to the thresholds defined in Table 1, the load switch will be enabled to provide vSafe5V on VBUS. The FAN6392 advertises support for 3A current at the vSafe5V output voltage level.

Table 1. CC VOLTAGES ON SOURCE SIDE – 3.0 A @ 5 V

Detection	Min Voltage	Max Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.75 V	0.80 V
Sink (vRd)	0.85 V	2.45 V	2.60 V
No connect (vOPEN)	2.75 V	–	–

Figure 18 shows the signal levels and timing for a typical USB Type−C attach on CC1. The Source pull−up currents are enabled on both CC1 and CC2 and the USB cable connects the Rd resistor on the CC1 signal in the Sink device which pulls down the CC1 voltage into the vRd range. Once the FAN6392 detects the voltage on CC1 within the vRd range for $t_{CCDebounce}$, the load switch is enabled and vSafe5V is applied on VBUS.

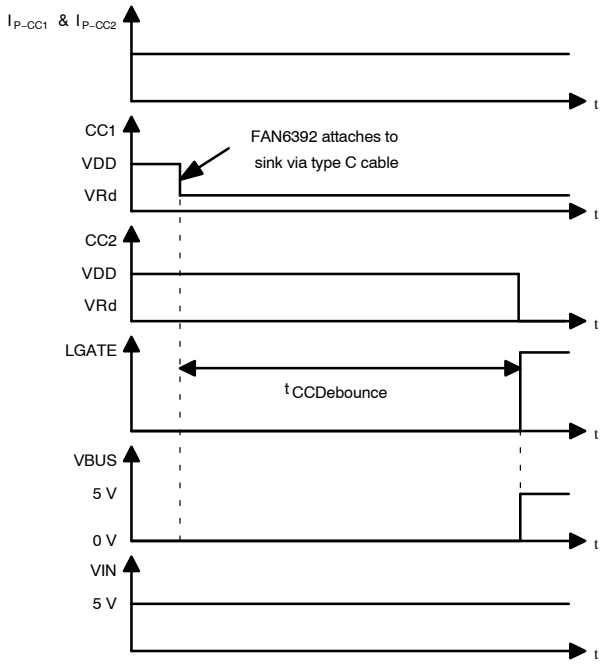


Figure 18. Attach to Sink Device via USB Type−C Cable

USB PD Support

USB Power Delivery (PD) provides a way for a Source and Sink device to negotiate output power settings, allowing for increased power delivery up to 100 W. USB PD uses the CC signal that is passed through the USB cable to provide the link between a Source device and a Sink device. In order to communicate properly over the CC signal, all USB PD−capable devices include four major communication components, the Physical Layer, Protocol Layer, Policy Engine and Device Policy Manager as shown in Figure 19.

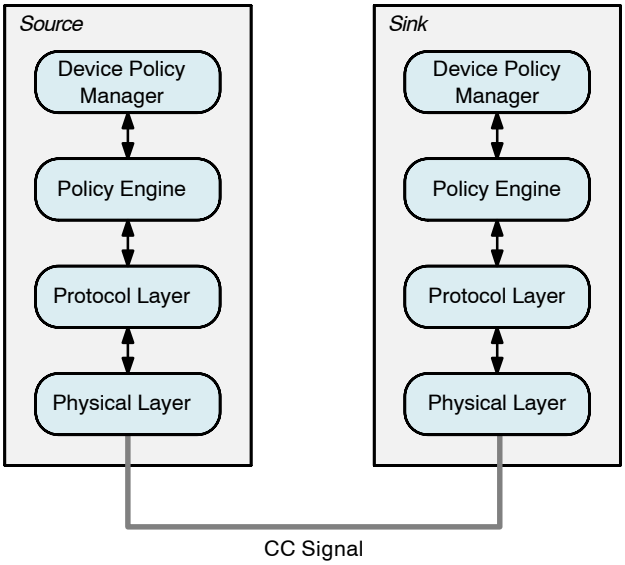


Figure 19. USB PD Communications Stack

The Physical Layer handles the transmission and reception of the bits on the CC signal. All data is first encoded using a 4b5b line code and then transmitted across the CC signal using Biphase Mark Coding (BMC). A 32−bit CRC is also used to protect the data integrity of the data payload.

The Protocol Layer defines how USB PD messages are constructed and used between a Source device and a Sink device. All USB PD messages must follow a strict packet definition and may also include timing requirements based on the type of message. The Protocol Layer is responsible for verifying the timing parameters and handling any communication errors as they arise.

The Policy Engine is responsible for executing the device Local Policy to control its power delivery behavior. The Policy Engine defines a set of message sequences that must be followed for proper operation. All power negotiations are handled by the Policy Engine.

The Device Policy Manager is responsible for overseeing the power supply and managing changes to the Local Policy, including handling of alert and fault conditions. It is also responsible for managing VCONN and the Discover Identity messaging to determine the full capabilities of the cabling.

The FAN6392 implements all four components of the Source communication stack in hardware to provide a USB PD 3.0 fully−compliant solution without the need for firmware interaction. Control of the Constant Voltage and Constant Current DAC's is integrated into the Policy Engine to provide seamless power transitions between different contracts.

USB PD Power Profiles

The USB PD 3.0 specification defines Power Data Objects (PDO) and Augmented Power Data Objects (APDO) as a way for the Source device to advertise its' power capabilities. Power Data Objects are used to describe well−regulated fixed voltage supplies, poorly regulated power supplies and battery supplies that can be directly connected to VBUS. Augmented Power Data Objects are used to describe a power supply whose output voltage can be programmatically adjusted over the advertised voltage range (Programmable Power Supply or PPS). A Source can advertise a combination of PDO's and APDO's, up to a maximum of 7 total Data Objects. In order to provide a consistent experience across Source devices with the same power rating (PDP), a set of Power Rules was introduced into the USB PD 3.0 specification. The Power Rules provide a set of minimum requirements (PDO's and APDO's) that must be met for a Source device based on the advertised PDP.

The FAN6392's default power profile option is 25 W option as shown in Table 2.

Table 2. FAN6392 DEFAULT POWER PROFILE

Data Object	Output Voltage	Max Current w/ 3 A Cable	Current Mode
PDO1	5 V	3.0 A	CC
PDO2	9 V	2.78 A	CC
APDO1	5 V (3.3~5.9 V)	3.0 A	CC
APDO2	9 V (3.3~11 V)	2.78 A	CC

Constant Voltage Control

In order to regulate adaptive output voltages, the constant voltage control (CV) is implemented. The output voltage is sensed through an external resistor divider. The sensed output voltage is connected to the VREF pin, and it is input the non−inverting input terminal of the internal operational amplifier. The inverting input terminal is connected to the internal voltage reference (V_{CVR}) which can be adjusted according to the requested output voltage. The amplifier and an internal switch operate as a shunt regulator, and the output of the shunt regulator is connected to the external opto−coupler via SFB pin. To compensate output voltage regulation, typically, two capacitors and one resistor are connected between SFB and VREF pins as Figure 20. The

output voltage can be derived as calculated by the equation (1), and the ratio of the resistor divider is 10. The reference (V_{CVR}) for the output voltage is generated by a 10−bit DAC. The minimum resolution is 20 mV to meet PD3.0 compliance spec.

$$V_O = V_{CVR} \cdot \frac{R_{F1} + R_{F2}}{R_{R_{F2}}} \quad \text{(eq. 1)}$$

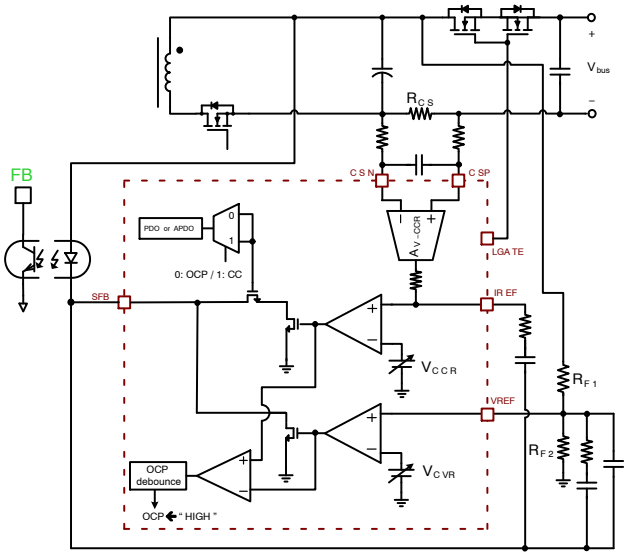


Figure 20. Voltage and Current Sensing Circuits

Constant Current Control

Constant current (CC) control is enabled during USB PD APDO and PDO contracts (PPS modes). When CC mode is enabled, the supply will foldback the output voltage as the load increases in order to maintain a fixed output current as shown in Figure 21. Output current is sensed via a current−sense resistor RCS, which is connected between the CSP and CSN pins. The sensed signal is internally amplified, and this amplified voltage is connected to the non−inverting input of the internal operational amplifier. Similar to the constant voltage amplifier circuit, it also plays a role as a shunt regulator to regulate the constant output current. In order to compensate output current regulation, one capacitor and one resistor are connected between the IREF and SFB pins as shown in Figure 20. The constant output current can be calculated using equation 2. 5 mΩ is typically used for the sense resistor.

$$I_{O\_CC} = \frac{1}{A_{V-CCR}} \cdot \frac{V_{CCR}}{R_{CS}} \quad \text{(eq. 2)}$$

Since the voltage across the CSP and CSN pins is small, the sensing resistor should be positioned as close as possible to the pins. An RC filter can be added to the pins to reduce the noise seen on the circuit.

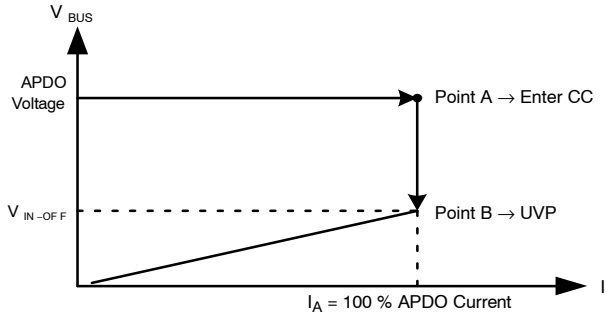


Figure 21. APDO/PDO CC Operation

Green Mode Operation

The FAN6392 implements green mode operation in order to reduce power consumption during light−load conditions. Green Mode is enabled when there is no valid Sink attached to the Type−C port. During Green Mode operation the Synchronous Rectifier and other block are disabled, reducing the operating current to $I_{IN-Green}$. Green Mode operation is disabled when there is valid Type−C Sink device attached.

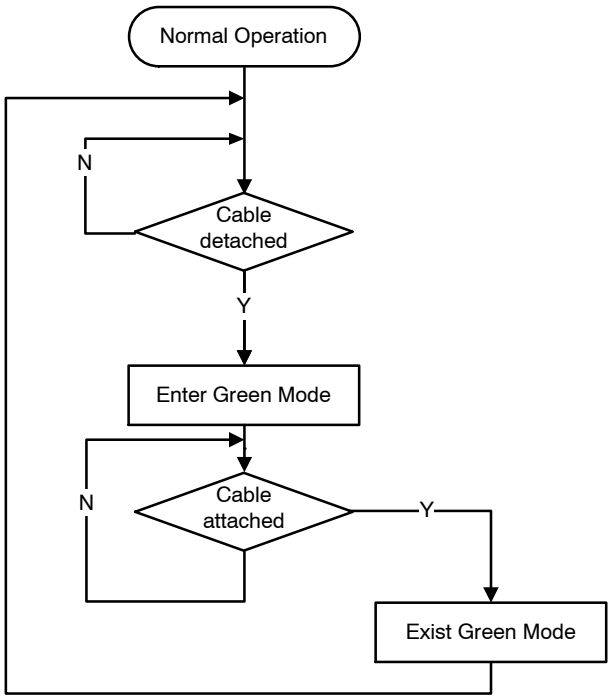


Figure 22. Green Mode Operation

Bleeder Functionality

Bleeder circuits are implemented on the VIN and BLD pins to discharge the output capacitors quickly during mode transitions and to fully discharge VBUS when required. The bleeder circuits in the FAN6392 are sized to meet the timing requirements in the USB PD 3.0 specification. Since the

output load can discharge the load sufficiently during heavy loads, the bleeder circuits are only enabled during light load conditions ($I_{CS} < I_{CS-EN-BLD}$). The operation of the bleeder circuits is shown in Table 3, Table 4 and Table 5.

Table 3. MODE TRANSITION BLEEDER OPERATION

Step Size	New VBUS	t_{BLD} (typ)	BLD pin Bleeder	VIN pin Bleeder	LGATE
≤0.5 V	≥13 V	7 ms	Enabled	Disabled	Enabled
	<13 V	19 ms			
>0.5 V	≥13 V	56 ms			
	<13 V	224 ms			

Table 4. DETACH & HARD RESET BLEEDER OPERATION

While VBUS	Final VBUS	t_{BLD} (typ)	BLD pin bleed	VIN pin Bleeder	LGATE
>vSafe5V	vSafe5V	224 ms	Enabled	Disabled	Enabled
≤vSafe5V	vSafe0V			Enabled	Disabled

Table 5. PROTECTION MODE BLEEDER OPERATION

Condition	Final VBUS	t_{BLD} (typ)	BLD pin bleed	VIN pin Bleeder	LGATE
Standard Protection	vSafe0V	224 ms	Enabled	Enabled	Disabled

Device Protections and Auto Restart Operation

The FAN6392 provides Output Over−Voltage Protection, Under−Voltage Protection, internal Over Temperature Protection, VCONN Over Current Protection, CC line Over Voltage Protection and DN pin Over Voltage Protection.

When a protection is triggered, the load switch is disabled and the VIN and BLD bleeder circuits are enabled to protect the Sink device. During this time, the CC pull−up currents ($I_{p-cc1-330}$ and $I_{p-cc2-330}$) are disabled to indicate to the Sink device that the Source is not ready to provide power.

This is the first operation to notify and protect the connected Sink devices and the later more operation follows to protect primary power side. FAN6392 keep activates VIN bleeder and pull down the SFB pin until VIN voltage falls below $V_{LATCH-OFF}$. These are only two remained operations even though input voltage for FAN6392 is less than normal operating voltage of V_{IN-OFF}. Figure 24 illustrates the whole operation. The primary side controller immediately stops switching when a protection at secondary side is triggered because FAN6392 pulling down the SFB (Secondary Feed Back) current and thru the current transferring of opto−coupler primary FB (Feed Back) voltage is pulled down either and restarts switching once VIN falls below $V_{LATCH-OFF}$. Until this timing as long as primary V_{DD} is keep supplied thru auxiliary winding primary controller does not know what is happened at secondary side and FB voltage is restored once no secondary current is pulling down.

When primary controller starts switching operation secondary voltage is much lower than conventional operating voltage and it triggers primary VS UVP (Under Voltage Protection) thru the detection of auxiliary winding voltage. When paired with primary controller of FAN6080, FAN6080 enters 3 AR (Auto Restart) protection mode at low line and 6 AR protection mode at high line once triggered VS UVP. 3 AR time will be variable depend on primary V_{DD} capacitance and primary V_{DD} charging configuration but if system is designed in a typical way then it is around 6 seconds. After 6 seconds primary controller starts switching again and output voltage will be raised to restart the secondary operation, this could be regarded as a Power ON Reset in view point of secondary controller.

If secondary condition is the same as before then the same secondary protection is triggered and the operation repeats until the protection condition is resolved. The advantage of this operation is that once any protection is triggered then output voltage is keeping the low level, average is less than 1 V, as long as protection condition exist. Accordingly regardless of output load Switch exist or not total primary and secondary side is well protected and extremely in safe condition, prohibit any kind of thermal stress, excessive power consumption and degradation of component lifetime.

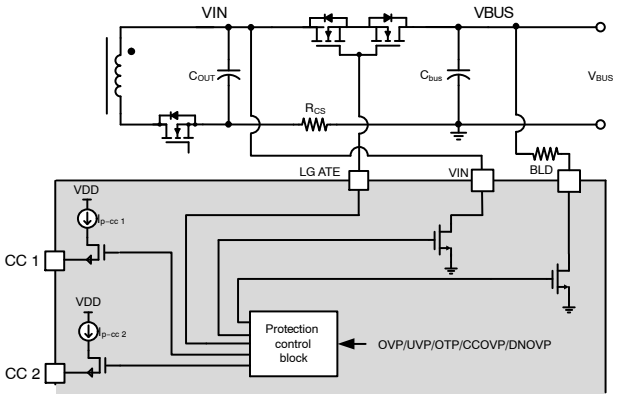


Figure 23. Protection Block Diagram

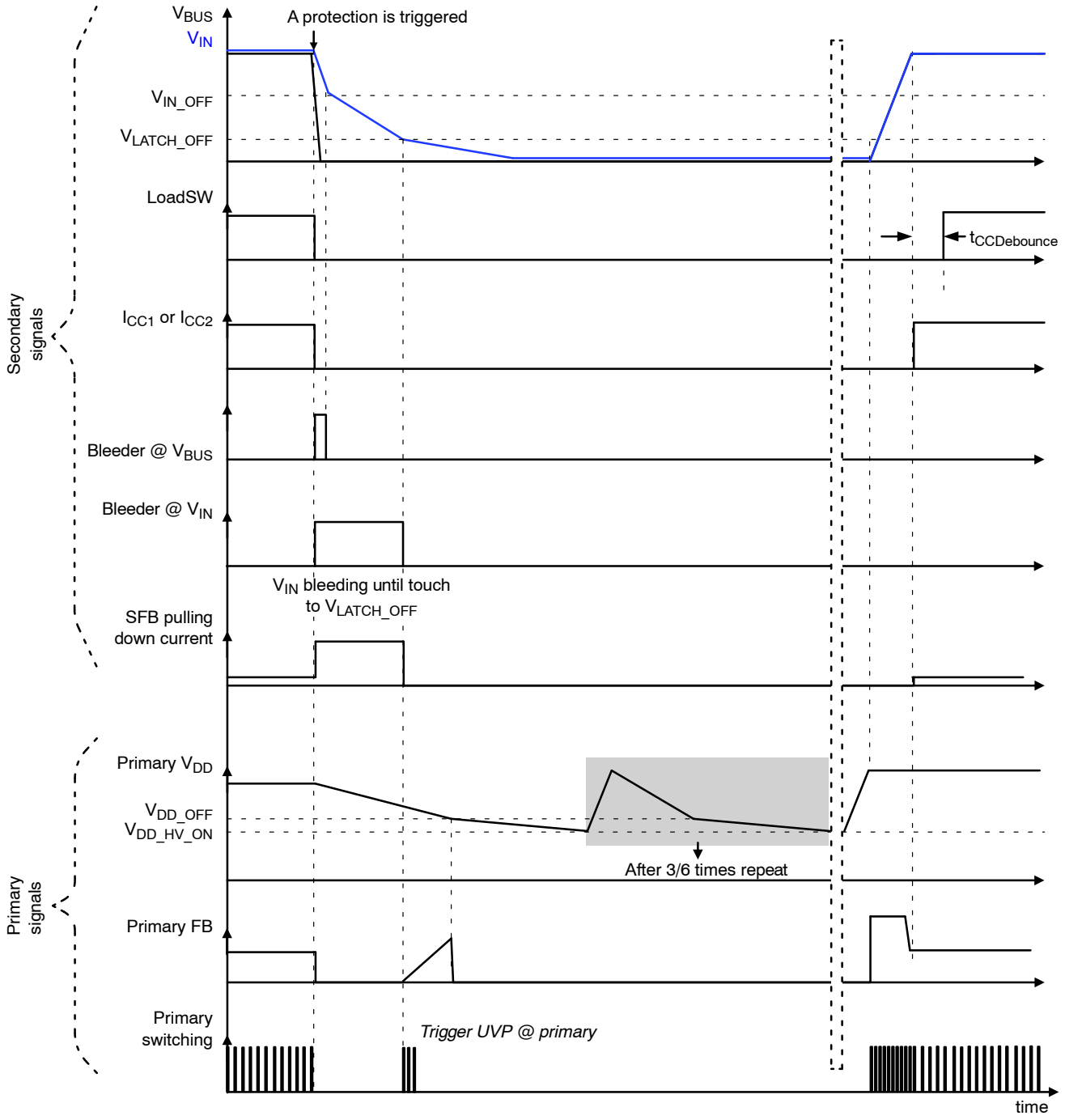


Figure 24. Primary and Secondary Auto Restart Mode Operation

Output Over−Voltage Protection

Over Voltage Protection (OVP) protects the system of any unexpected high voltage on the VBUS terminals. An OVP fault is triggered when the output voltage exceeds the OVP threshold for longer than t_{D-OVP}. Since the output voltage can change with different USB PD requests, the OVP thresholds will move with the selected contact as shown in Figure 25. In order to avoid mis−triggering an OVP condition during voltage transitions, the OVP circuitry is blanked for $t_{BNK-OVP}$. The maximum OVP threshold is limited to $V_{IN-OVP-MAX}$ regardless of the settings in the table to ensure the voltages stay within the operating range of the FAN6392.

Table 6. OVER−VOLTAGE PROTECTION THRESHOLD

Protocol	PDO or APDO	OVP Threshold
PD2.0	All PDOs	K_{IN-OVP} * PDO
PD3.0	All APDOs	K_{IN-OVP} * APDO

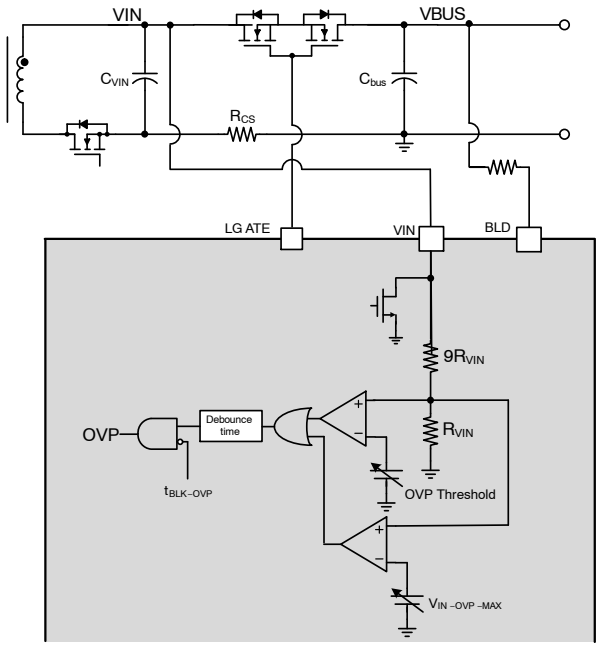


Figure 25. Output Over Voltage Sense Block

Under Voltage Lockout Protection

Under Voltage Lockout (UVLO) protects the system when the output is short−circuited with small impedance. When VIN falls below V_{IN-OFF} threshold, the FAN6392 enters UVLO protection, it could be also called as VIN−OFF protection, by disabling the load switch, enabling the VIN bleeder and pulling SFB low until VIN falls below $V_{LATCH-OFF}$. The sequence is the same as explained and illustrates in the Figure 24 and system is fully protected from any kind of thermal stress, excessive power consumption and degradation of component lifetime.

Internal Over Temperature Protection

The FAN6392 also implements internal over temperature protection through an internal temperature sensing circuit. Once the internal temperature exceeds the fault protection threshold of 140°C, the FAN6392 sends an Alert indicating an Fault and the device will enter Auto Restart Mode .

VCONN Over Current Protection

A VCONN supply is implemented in the FAN6392 in order to power the E−Marker inside USB Type−C cables designed for currents exceeding 3 A. In order to protect the operation of the FAN6392, an Over−Current Protection circuit is implemented for the VCONN supply. If the current on the CC pin rises above I_{CONN_OCP} for longer than t_{VCONN_OCP}, the FAN6392 will disable the VCONN supply and abort the cable marker interrogation.

CC Signal Over−Voltage Protection

The USB Type−C CC pins are located physically close to VBUS on the connector and could be shorted to VBUS via conductive materials as shown in Figure 26. This not only impacts PD protocol communication, but possibly damages the CC pins because of high VBUS voltages. The FAN6392 attempts to protect against damaging the CC pins by implementing Over−Voltage−Protection on the CC pins. The voltage on the CC1 and CC2 pins is continuously monitored, if the voltage increases above $V_{CC1-OVP}$ or $V_{CC2-OVP}$ for longer than $t_{CC-OVP-Debounce}$, the CC Over−Voltage Protection is triggered and the device enters Auto Restart Mode.

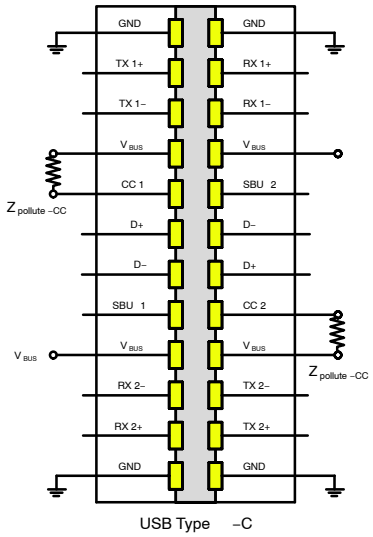


Figure 26. CC1/CC2 Short−circuited with Impedance

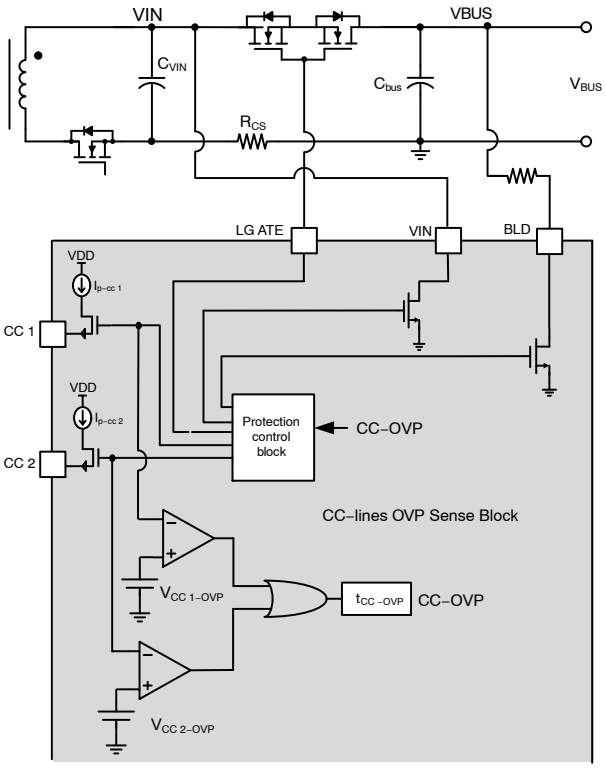


Figure 27. CC OVP Sensing Block Diagram

D− pollution Protection and Over−Voltage Protection

With the similar manner as CC pins D− (D negative) pin is also possible to be shorted to VBUS via conductive materials and possibly damages the D− pin because of high VBUS voltages. FAN6392 has two protections for D− pin, one is pollution protection and the other is Over−Voltage−Protection.

Pollution protection is checking the impedance of D− pin repeatedly with $t_{POL-DET-PERIOD1}$ intervals and if checked the impedance is less than $R_{POL(MAX)}$ then enter Auto Restart Mode. This repetition continues until FAN6392 identifies SINK attachment. The voltage on the D− pin is continuously monitored except $t_{POL-DET}$, if the voltage increases above V_{DN-OVP} for longer than $t_{DN-OVP-Debounce}$, the DN Over−Voltage Protection is triggered and the device enters Auto Restart Mode.

Charge Pump for Synchronous Rectifier (SR)

Generally, SR driving voltage is powered from V_{DD} derived from system V_{BUS} which drives internal circuits and SR MOSFET through GATE pin. The GATE driving voltage can't be higher than V_{BUS}. In order to achieve adapter charging high efficiency at low output voltage and high output current application, a new way to boosting GATE pin voltage for Low Side SR is implemented as Figure 28.

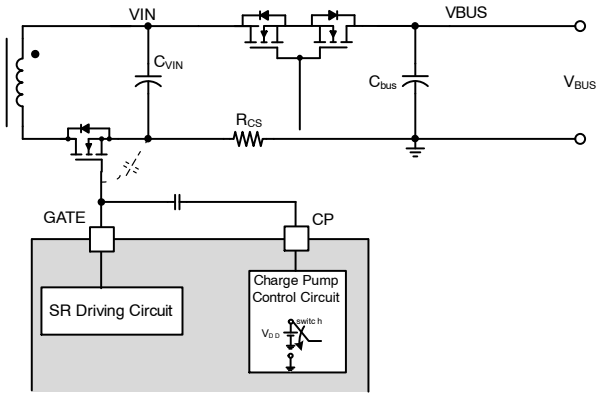


Figure 28. Charge Pump Control Circuit

When input voltage is less than V_{CP-EN}, FAN6392 enable charge pump circuit to have higher driving voltage up to V_{OH}. During a short period time when gate driver becomes high switch inside Charge Pump Control Circuit switches to GND and after the short period of time switch connects to V_{DD} to boost V_{OH}. V_{OH} will be clamped to ensure the voltage no higher than maximum rating to ensure driving circuit safe operation as Figure 29. Basically, proper CP capacitance is needed to achieve better system efficiency. This capacitance value should be less than 10 nF and should be adjusted depending on the MOSFET's parasitic input capacitance.

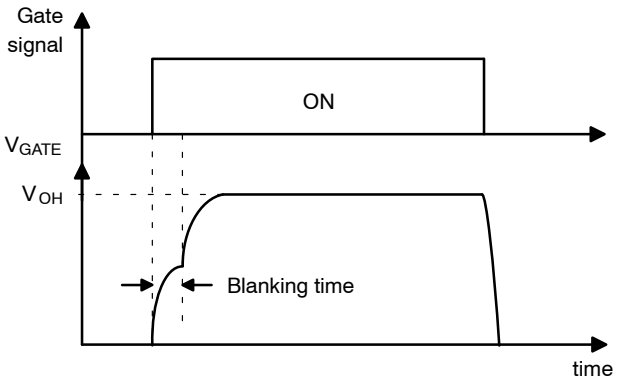


Figure 29. Timing Flow of Charge Pump

Table 7. OVERVIEW OF PROTECTIONS

Protection	PDO Threshold	APDO Threshold
Under Voltage Lockout(UVLO)	V_{IN-OFF}	
Output Over−Voltage Protection (OVP)	115% (typ.)	
Output Under−Voltage Protection (UVP)	76% (typ.)	V_{IN-OFF}
Output Over−Current Protection (OCP)	None	None
CC Lines Over−Voltage Protection (CC−OVP)	5.80 V (typ.)	
DN Line Over−Voltage Protection (DN−OVP)	4.35 V (typ.)	
DN Line Impedance Detection (DN−POL)	410 Ω (max.)	
Internal Over Temperature Protection	140°C	
Vconn OCP	50 mA (min.)	

NOTE: APDO/PDO always works in CC mode

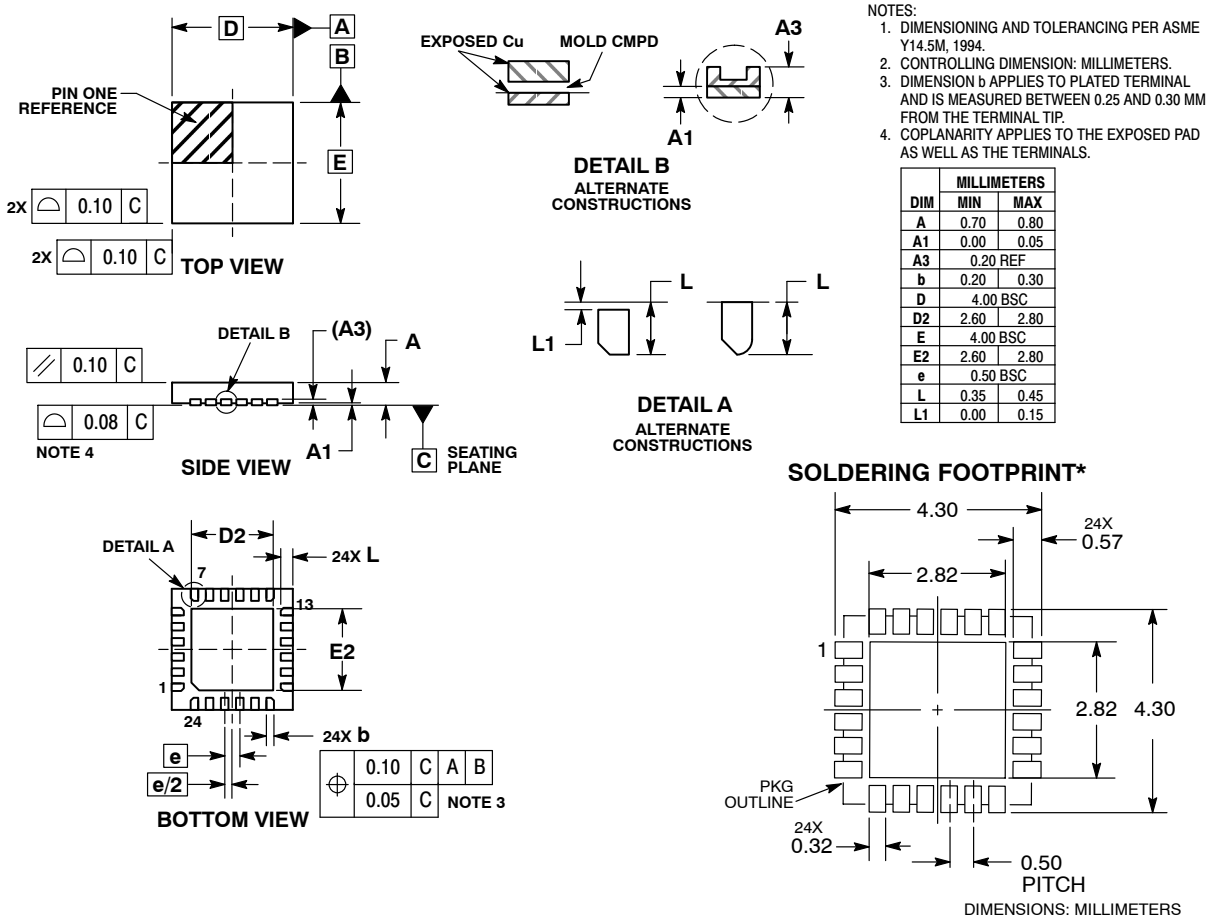
ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
FAN6392MPX	−40°C to +125°C	WQFN24 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

Â
WQFN24, 4x4, 0.5P
CASE 510BE
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.80
E	4.00 BSC	
E2	2.60	2.80
e	0.50 BSC	
L	0.35	0.45
L1	0.00	0.15

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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