

# MOSFET - Power, Single N-Channel

100 V, 3.6 mΩ, 131 A

## NTMFS3D6N10MCL

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- Primary DC–DC MOSFET
- Synchronous Rectifier in DC–DC and AC–DC
- Motor Drive
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain–to–Source Voltage		$V_{DSS}$	100	V
Gate–to–Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	131
		$T_C = 100^\circ\text{C}$		93
		$T_C = 25^\circ\text{C}$	$P_D$	136
Power Dissipation $R_{\theta JC}$ (Note 1)				
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	19.5
		$T_A = 25^\circ\text{C}$	$P_D$	3.0
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)				
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	1674	A
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Single Pulse Drain–to–Source Avalanche Energy ( $L = 3 \text{ mH}, I_{AS} = 14 \text{ A}$ )		$E_{AS}$	294	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction–to–Case – Steady State	$R_{\theta JC}$	1.1	$^\circ\text{C}/\text{W}$
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	50	

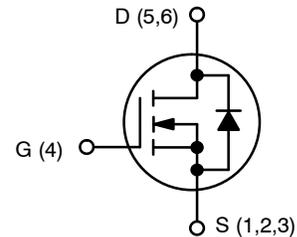
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface–mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



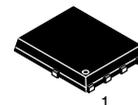
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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	3.6 mΩ @ 10 V	131 A
	5.8 mΩ @ 4.5 V	

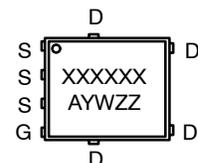


N-CHANNEL MOSFET



DFN5  
CASE 488AA  
STYLE 1

### MARKING DIAGRAM



XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 3 of this data sheet.

# NTMFS3D6N10MCL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			60		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

## ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 270\ \mu\text{A}$	1	1.5	3	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-5.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 48\text{ A}$	3.0	3.6	m $\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 39\text{ A}$	4.4	5.8	
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 48\text{ A}$		163		S

## CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		4411		pF
Output Capacitance	$C_{OSS}$			1808		
Reverse Transfer Capacitance	$C_{RSS}$			29		
Gate Resistance	$R_G$		0.1	0.7	3	$\Omega$
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 50\text{ V}; I_D = 48\text{ A}$		29		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}; I_D = 48\text{ A}$		60		nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}; I_D = 48\text{ A}$		6		nC
Gate-to-Source Charge	$Q_{GS}$			10		
Gate-to-Drain Charge	$Q_{GD}$			7		
Plateau Voltage	$V_{GP}$			3		V
Output Charge	$Q_{OSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		119		nC
Total Gate Charge Sync	$Q_{SYNC}$	$V_{GS} = 0\text{ to }10\text{ V}, V_{DS} = 0\text{ V}$		51		nC

## SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 48\text{ A}, R_G = 6.0\ \Omega$		14		ns
Rise Time	$t_r$			11		
Turn-Off Delay Time	$t_{d(OFF)}$			42		
Fall Time	$t_f$			8		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Source to Drain Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 7)		0.65	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 48\text{ A}$ (Note 7)		0.83	1.3	
Reverse Recovery Time	$t_{rr}$	$I_F = 24\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		34		ns
Reverse Recovery Charge	$Q_{rr}$			73		nC
Reverse Recovery Time	$t_{rr}$	$I_F = 24\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$		28		ns
Reverse Recovery Charge	$Q_{rr}$			183		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

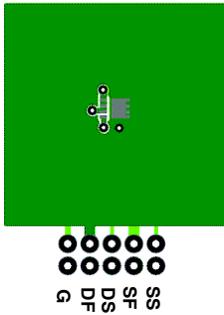
4. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

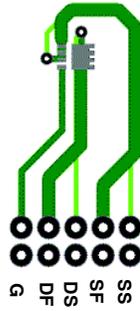
# NTMFS3D6N10MCL

**NOTES:**

6.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a) 50°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

7. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

8.  $E_{AS}$  of 294 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 3\text{ mH}$ ,  $I_{AS} = 14\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

9. Pulsed  $I_D$  please refer to Figure 11 SOA graph for more details.

10. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

## DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS3D6N10MCLT1G	3D6L10	DFN5 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMFS3D6N10MCL

## TYPICAL CHARACTERISTICS

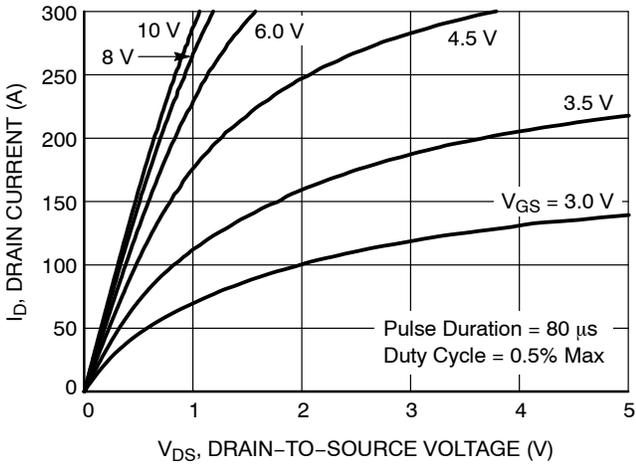


Figure 1. On-Region Characteristics

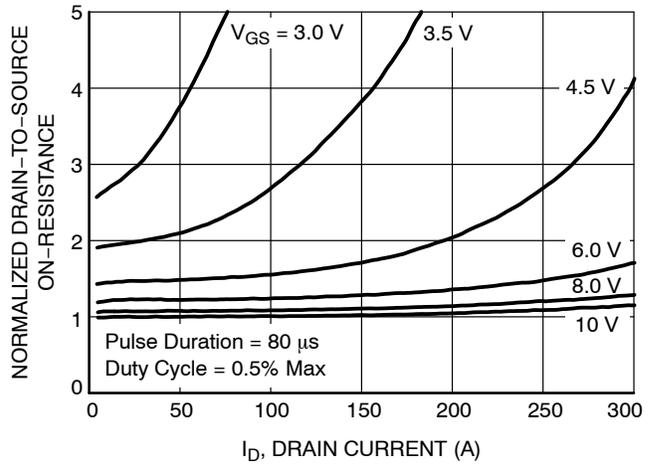


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

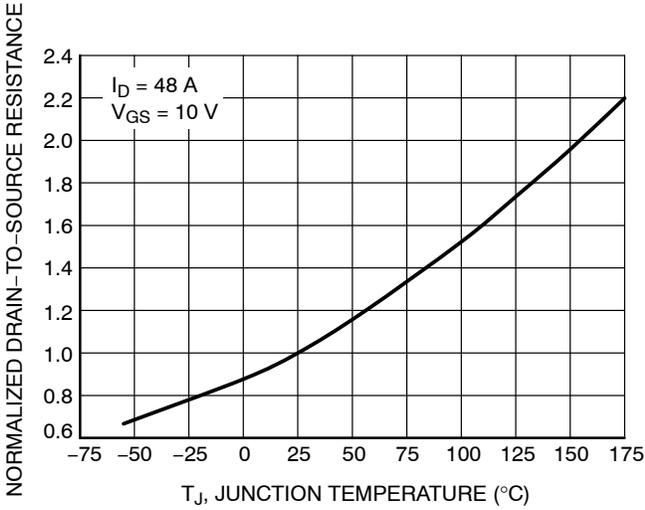


Figure 3. Normalized On-Resistance vs. Junction Temperature

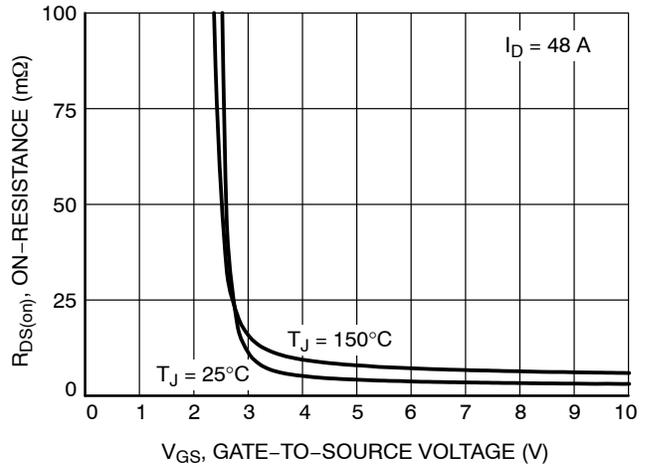


Figure 4. On-Resistance vs. Gate-to-Source Voltage

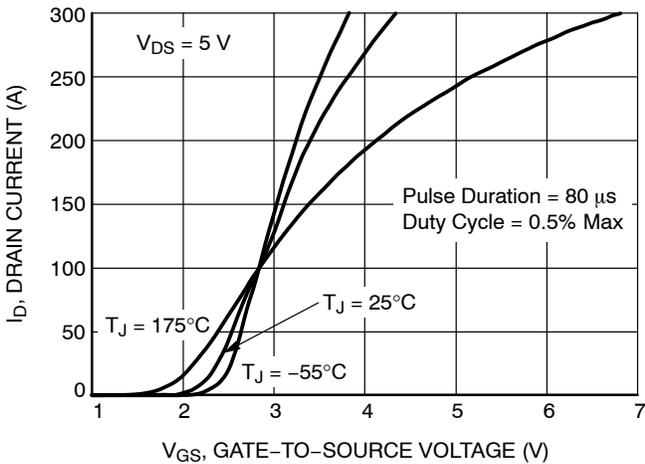


Figure 5. Transfer Characteristics

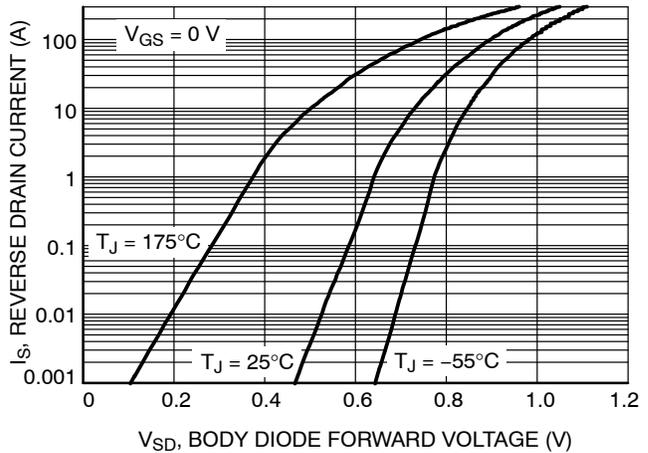


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

# NTMFS3D6N10MCL

## TYPICAL CHARACTERISTICS

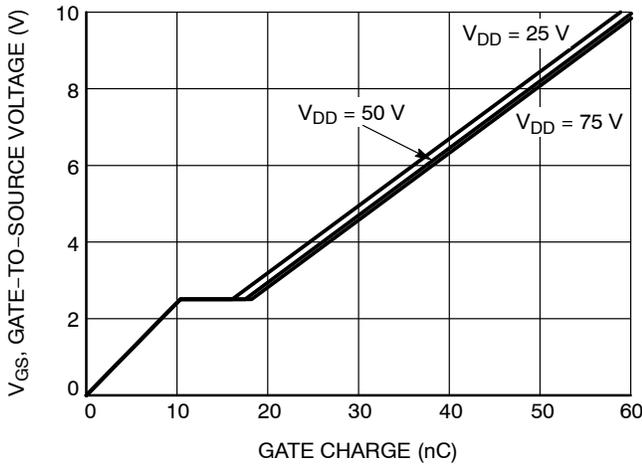


Figure 7. Gate Charge Characteristics

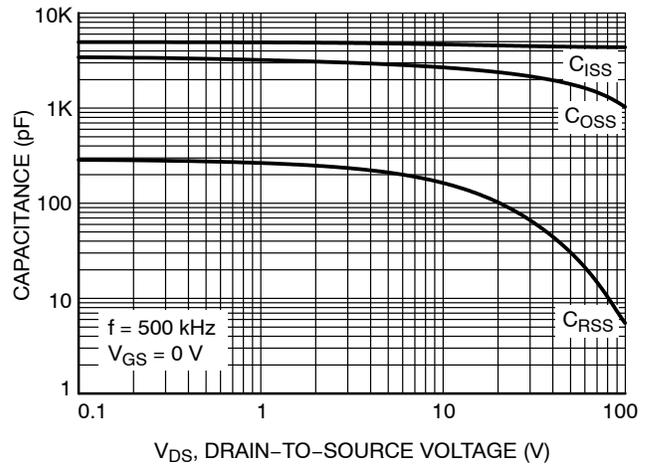


Figure 8. Capacitance vs. Drain-to-Source Voltage

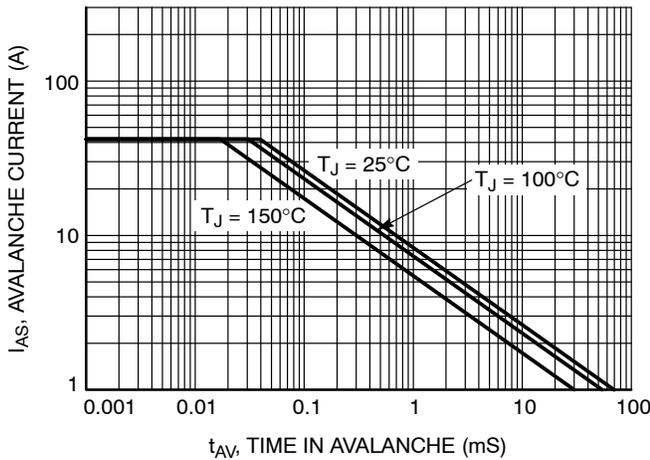


Figure 9. Unclamped Inductive Switching Capability

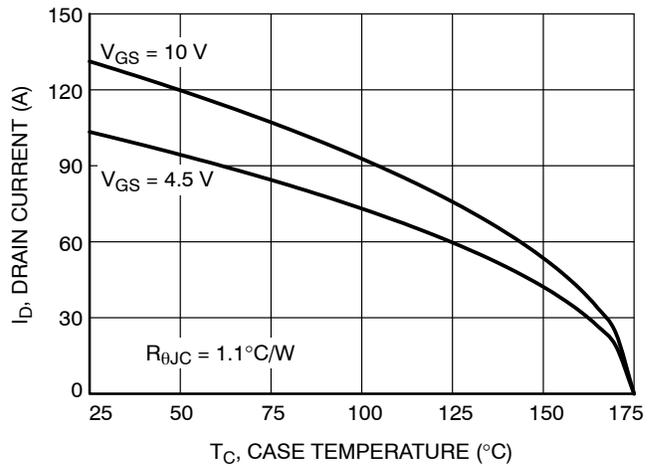


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

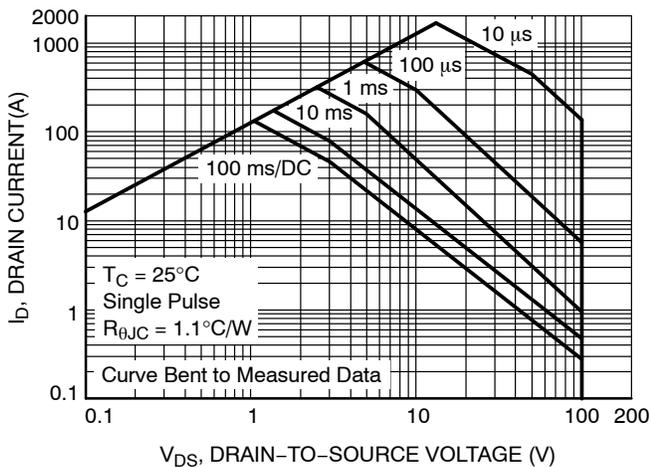


Figure 11. Forward Bias Safe Operating Area

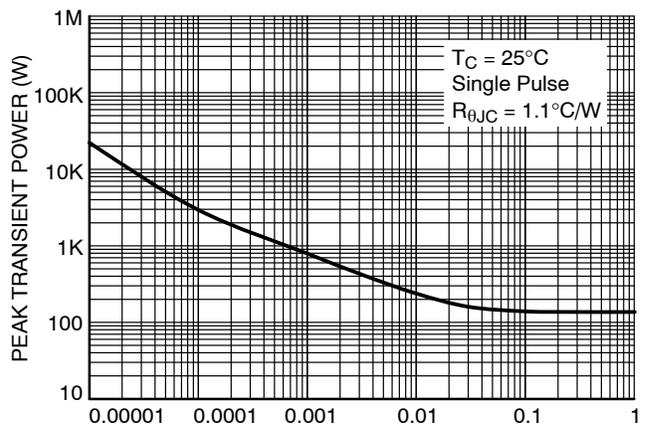


Figure 12. Single Pulse Maximum Power Dissipation

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## TYPICAL CHARACTERISTICS

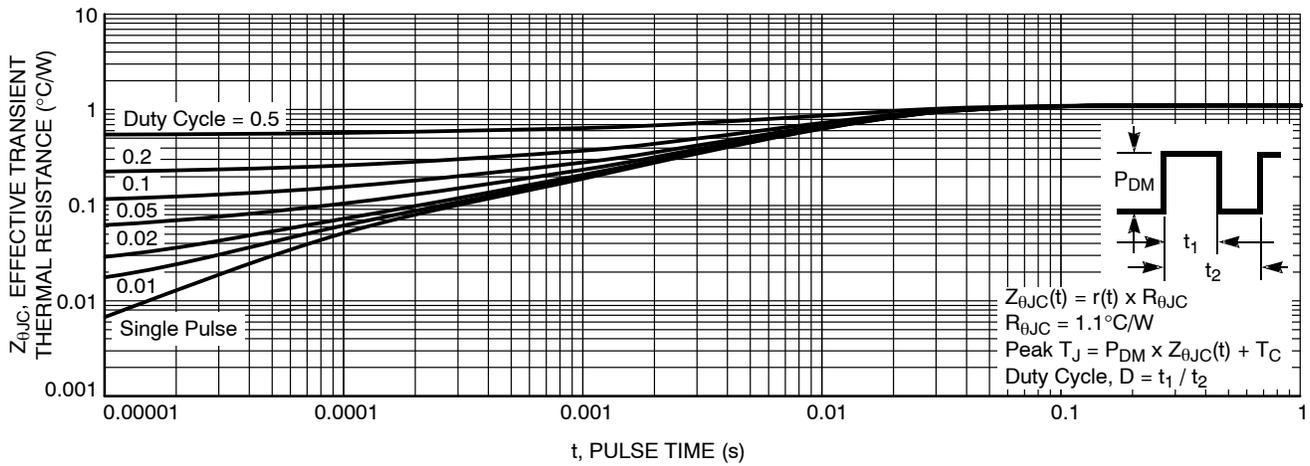


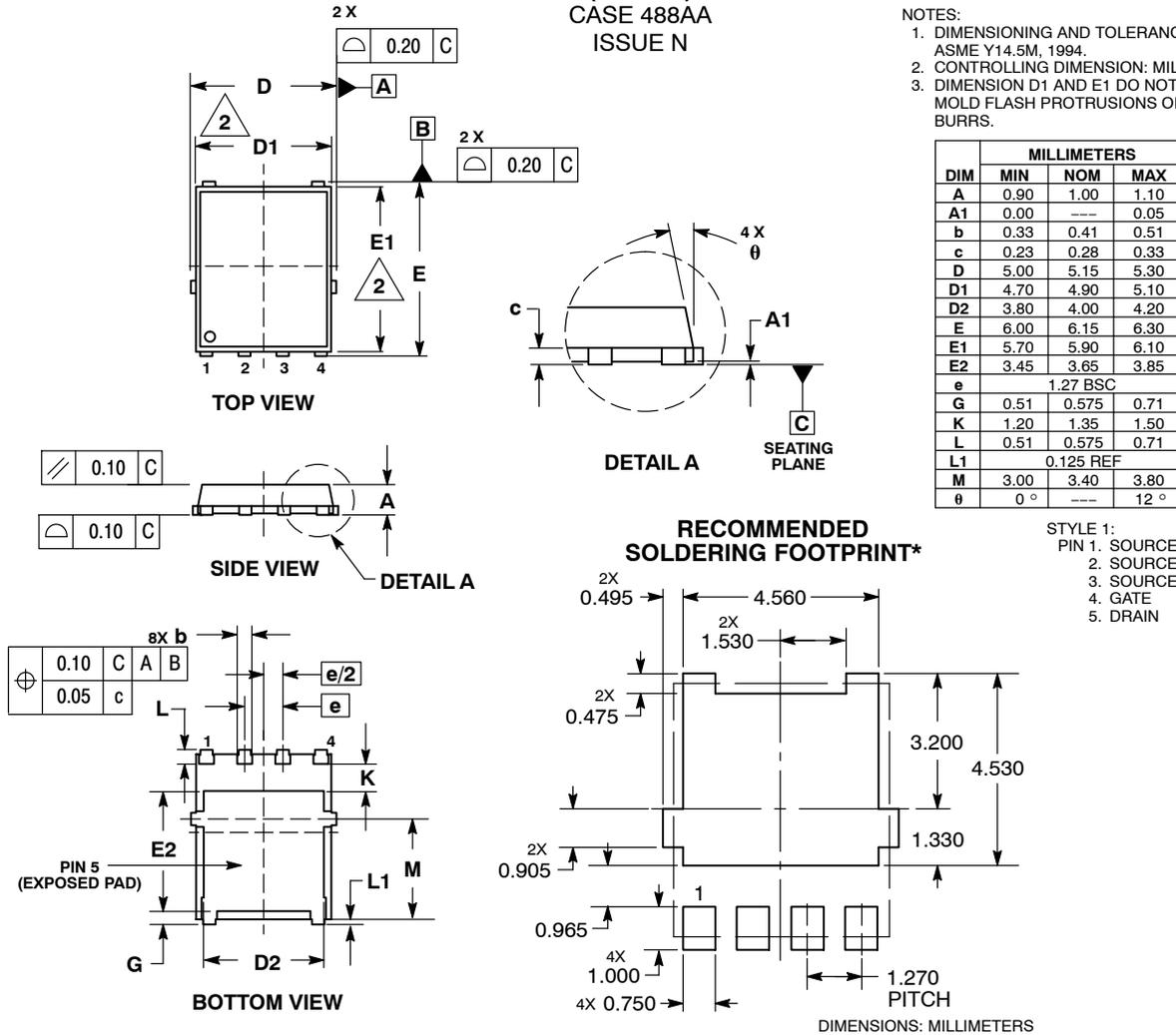
Figure 13. Junction-to-Case Transient Thermal Response Curve

# NTMFS3D6N10MCL

## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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