

# NCP170

## LDO Regulator, 150 mA, Ultra-Low I<sub>Q</sub>, CMOS

The NCP170 series of CMOS low dropout regulators are designed specifically for portable battery-powered applications which require ultra-low quiescent current. The ultra-low consumption of typ. 500 nA ensures long battery life and dynamic transient boost feature improves device transient response for wireless communication applications. The device is available in small 1 × 1 mm XDFN4, SOT-563 and TSOP-5 packages.

### Features

- Operating Input Voltage Range: 2.2 V to 5.5 V
- Output Voltage Range: 1.2 V to 3.6 V (0.1 V Steps)
- Ultra-Low Quiescent Current Typ. 0.5  $\mu$ A
- Low Dropout: 170 mV Typ. at 150 mA
- High Output Voltage Accuracy  $\pm 1\%$
- Stable with Ceramic Capacitors 1  $\mu$ F
- Over-Current Protection
- Thermal Shutdown Protection
- NCP170A for Active Discharge Option
- Available in Small 1 × 1 mm XDFN4, SOT-563 and TSOP-5 Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Battery Powered Equipments
- Portable Communication Equipments
- Cameras, Image Sensors and Camcorders

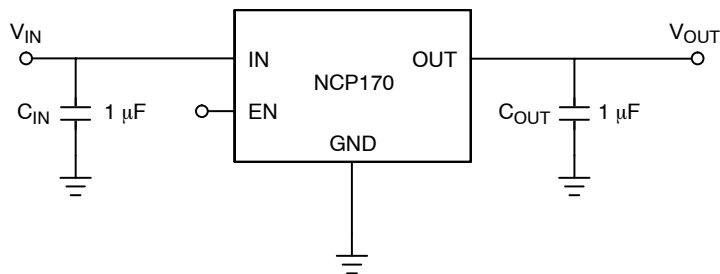


Figure 1. Typical Application Schematic

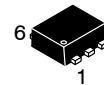


**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)



**XDFN4**  
**MX SUFFIX**  
**CASE 711AJ**



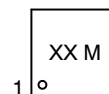
**SOT-563**  
**XV SUFFIX**  
**CASE 463A**



**TSOP-5**  
**SN SUFFIX**  
**CASE 483**

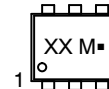
### MARKING DIAGRAMS

#### XDFN4



XX = Specific Device Code  
M = Date Code

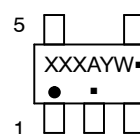
#### SOT-563



XX = Specific Device Code  
M = Month Code  
▪ = Pb-Free Package

\*Pb-Free indicator, "G" or microdot "▪", may or may not be present.

#### TSOP-5



XXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 21 of this data sheet.

# NCP170

## PIN FUNCTION DESCRIPTION

Pin No. XDFN4	Pin No. SOT-563	Pin No. TSOP-5	Pin Name	Description
4	1	1	IN	Power Supply Input Voltage
2	2	2	GND	Power Supply Ground
3	6	3	EN	Chip Enable Pin (Active “H”)
1	3	5	OUT	Output Pin
EPAD	–	–	EPAD	Internally Connected to GND
–	4	4	NC	No Connect
–	5	–	GND	Power Supply Ground

## ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
$V_{IN}$	Input Voltage (Note 1)	6.0	V
$V_{OUT}$	Output Voltage	$-0.3$ to $V_{IN} + 0.3$	V
$V_{CE}$	Chip Enable Input	$-0.3$ to $6.0$	V
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
$T_{STG}$	Storage Temperature	$-55$ to $150$	°C
$ESD_{HBM}$	ESD Capability, Human Body Model (Note 2)	2000	V
$ESD_{MM}$	ESD Capability, Machine Model (Note 2)	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

2. This device series incorporates ESD protection and is tested by the following methods:

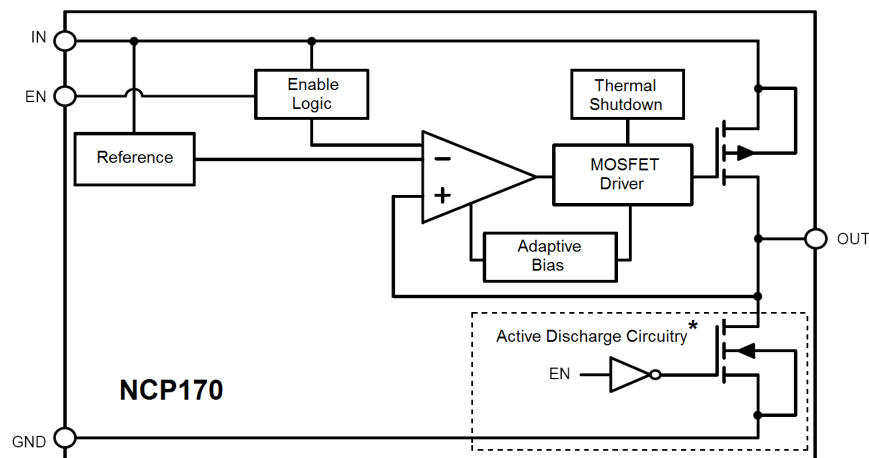
ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)

ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)

Latchup Current Maximum Rating tested per JEDEC standard: JESD78

## THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
$R_{\theta JA}$	Thermal Characteristics, Thermal Resistance, Junction-to-Air XDFN4 $1 \times 1$ mm SOT-563 TSOP-5	250 200 250	°C/W



\* Active discharge feature is present only in NCP170AxxvvvTyG devices.

Figure 2. Simplified Block Diagram

# NCP170

## ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 1.2 V

( $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ;  $V_{IN} = 2.5\text{ V}$ ;  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}\text{C}$ .) (Note 3)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IN}$	Operating Input Voltage		2.2	–	5.5	V
$V_{OUT}$	Output Voltage	$T_A = +25^{\circ}\text{C}$	1.188	1.2	1.212	V
		$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$	1.176	1.2	1.224	
$\text{Line}_{\text{Reg}}$	Line Regulation	$2.5\text{ V} < V_{IN} \leq 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$	–	0.05	0.20	%/V
$\text{Load}_{\text{Reg}}$	Load Regulation	$0\text{ mA} < I_{OUT} \leq 150\text{ mA}$ , $V_{IN} = 2.5\text{ V}$	–20	1	20	mV
$V_{DO}$	Dropout Voltage	(Note 4)	–	–	–	mV
$I_{OUT}$	Output Current	(Note 5)	150	–	–	mA
$I_{SC}$	Short Circuit Current Limit	$V_{OUT} = 0\text{ V}$	–	225	–	mA
$I_Q$	Quiescent Current	$I_{OUT} = 0\text{ mA}$	–	0.5	0.9	$\mu\text{A}$
$I_{STB}$	Standby Current	$V_{EN} = 0\text{ V}$ , $T_J = 25^{\circ}\text{C}$	–	0.1	0.5	$\mu\text{A}$
$V_{ENH}$	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
$V_{ENL}$	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
$I_{EN}$	EN Pin Current	$V_{EN} \leq V_{IN} \leq 5.5\text{ V}$ (Note 6)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	$f = 1\text{ kHz}$ , $V_{IN} = 2.2\text{ V} + 200\text{ mVpp}$ Modulation	–	57	–	dB
		$I_{OUT} = 150\text{ mA}$ $I_{OUT} = 10\text{ mA}$	– 63	– –	– –	
$V_{NOISE}$	Output Noise Voltage	$V_{IN} = 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$ , $f = 100\text{ Hz}$ to $1\text{ MHz}$ , $C_{OUT} = 1\text{ }\mu\text{F}$	–	85	–	$\mu\text{V}_{\text{rms}}$
$R_{\text{LOW}}$	Active Output Discharge Resistance (A option only)	$V_{IN} = 5.5\text{ V}$ , $V_{EN} = 0\text{ V}$ (Note 6)	–	100	–	$\Omega$
$T_{SD}$	Thermal Shutdown Temperature	Temperature Increasing from $T_J = +25^{\circ}\text{C}$ (Note 6)	–	175	–	$^{\circ}\text{C}$
$T_{SDH}$	Thermal Shutdown Hysteresis	Temperature Falling from $T_{SD}$ (Note 6)	–	25	–	$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at  $T_J = T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

4. Not Characterized at  $V_{IN} = 2.2\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $I_{OUT} = 150\text{ mA}$ .

5. Respect SOA.

6. Guaranteed by design and characterization.

# NCP170

## ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 1.5 V

( $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ;  $V_{IN} = 2.5\text{ V}$ ;  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}\text{C}$ .) (Note 7)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IN}$	Operating Input Voltage		2.2	–	5.5	V
$V_{OUT}$	Output Voltage	$T_A = +25^{\circ}\text{C}$	1.485	1.5	1.515	V
		$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$	1.470	1.5	1.530	
$\text{Line}_{\text{Reg}}$	Line Regulation	$4.3\text{ V} < V_{IN} \leq 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$	–	0.05	0.20	%/V
$\text{Load}_{\text{Reg}}$	Load Regulation	$0\text{ mA} < I_{OUT} \leq 150\text{ mA}$ , $V_{IN} = 4.3\text{ V}$	–20	–	20	mV
$V_{DO}$	Dropout Voltage	$I_{OUT} = 150\text{ mA}$ (Note 8)	–	–	–	mV
$I_{OUT}$	Output Current	(Note 9)	150	–	–	mA
$I_{SC}$	Short Circuit Current Limit	$V_{OUT} = 0\text{ V}$	–	225	–	mA
$I_Q$	Quiescent Current	$I_{OUT} = 0\text{ mA}$	–	0.5	0.9	$\mu\text{A}$
$I_{STB}$	Standby Current	$V_{EN} = 0\text{ V}$ , $T_J = 25^{\circ}\text{C}$	–	0.1	0.5	$\mu\text{A}$
$V_{ENH}$	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
$V_{ENL}$	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
$I_{EN}$	EN Pin Current	$V_{EN} \leq V_{IN} \leq 5.5\text{ V}$ (Note 10)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	$f = 1\text{ kHz}$ , $V_{IN} = 2.5\text{ V} + 200\text{ mVpp}$ Modulation $I_{OUT} = 150\text{ mA}$	–	57	–	dB
$V_{NOISE}$	Output Noise Voltage	$V_{IN} = 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$ , $f = 100\text{ Hz}$ to $1\text{ MHz}$ , $C_{OUT} = 1\text{ }\mu\text{F}$	–	90	–	$\mu\text{V}_{\text{rms}}$
$R_{LOW}$	Active Output Discharge Resistance (A option only)	$V_{IN} = 5.5\text{ V}$ , $V_{EN} = 0\text{ V}$ (Note 10)	–	100	–	$\Omega$
$T_{SD}$	Thermal Shutdown Temperature	Temperature Increasing from $T_J = +25^{\circ}\text{C}$ (Note 10)	–	175	–	$^{\circ}\text{C}$
$T_{SDH}$	Thermal Shutdown Hysteresis	Temperature Falling from $T_{SD}$ (Note 10)	–	25	–	$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at  $T_J = T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

8. Not Characterized at  $V_{IN} = 2.2\text{ V}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $I_{OUT} = 150\text{ mA}$ .

9. Respect SOA.

10. Guaranteed by design and characterization.

# NCP170

## ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 1.8 V

( $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ;  $V_{IN} = 2.8\text{ V}$ ;  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}\text{C}$ .) (Note 11)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IN}$	Operating Input Voltage		2.2	–	5.5	V
		$I_{OUT} < 30\text{ mA}$	2.0	–	5.5	
$V_{OUT}$	Output Voltage	$T_A = +25^{\circ}\text{C}$	1.782	1.8	1.818	V
		$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$	1.764	1.8	1.836	
$\text{Line}_{\text{Reg}}$	Line Regulation	$2.8\text{ V} < V_{IN} \leq 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$	–	0.05	0.20	%/V
$\text{Load}_{\text{Reg}}$	Load Regulation	$0\text{ mA} < I_{OUT} \leq 150\text{ mA}$ , $V_{IN} = 2.8\text{ V}$	–20	1	20	mV
$V_{DO}$	Dropout Voltage	$I_{OUT} = 150\text{ mA}$ (Note 12)	–	350	480	mV
$I_{OUT}$	Output Current	(Note 13)	150	–	–	mA
$I_{SC}$	Short Circuit Current Limit	$V_{OUT} = 0\text{ V}$	–	225	–	mA
$I_Q$	Quiescent Current	$I_{OUT} = 0\text{ mA}$	–	0.5	0.9	$\mu\text{A}$
$I_{STB}$	Standby Current	$V_{EN} = 0\text{ V}$ , $T_J = 25^{\circ}\text{C}$	–	0.1	0.5	$\mu\text{A}$
$V_{ENH}$	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
$V_{ENL}$	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
$I_{EN}$	EN Pull Down Current	$V_{EN} \leq V_{IN} \leq 5.5\text{ V}$ (Note 14)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	$f = 1\text{ kHz}$ , $V_{IN} = 2.8\text{ V} + 200\text{ mVpp}$ Modulation $I_{OUT} = 150\text{ mA}$	–	57	–	dB
$V_{\text{NOISE}}$	Output Noise Voltage	$V_{IN} = 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$ $f = 100\text{ Hz}$ to $1\text{ MHz}$ , $C_{OUT} = 1\text{ }\mu\text{F}$	–	95	–	$\mu\text{V}_{\text{rms}}$
$R_{\text{LOW}}$	Active Output Discharge Resistance (A option only)	$V_{IN} = 5.5\text{ V}$ , $V_{EN} = 0\text{ V}$ (Note 14)	–	100	–	$\Omega$
$T_{SD}$	Thermal Shutdown Temperature	Temperature Increasing from $T_J = +25^{\circ}\text{C}$ (Note 14)	–	175	–	$^{\circ}\text{C}$
$T_{SDH}$	Thermal Shutdown Hysteresis	Temperature Falling from $T_{SD}$ (Note 14)	–	25	–	$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at  $T_J = T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

12. Characterized when  $V_{OUT}$  falls 54 mV below the regulated voltage and only for devices with  $V_{OUT} = 1.8\text{ V}$ .

13. Respect SOA.

14. Guaranteed by design and characterization.

# NCP170

## ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 2.5 V

( $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ;  $V_{\text{IN}} = 3.5\text{ V}$ ;  $I_{\text{OUT}} = 1\text{ mA}$ ,  $C_{\text{IN}} = C_{\text{OUT}} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}\text{C}$ .) (Note 15)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{\text{IN}}$	Operating Input Voltage		2.2	–	5.5	V
$V_{\text{OUT}}$	Output Voltage	$T_A = +25^{\circ}\text{C}$	2.475	2.5	2.525	V
		$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$	2.450	2.5	2.550	
$\text{Line}_{\text{Reg}}$	Line Regulation	$3.5\text{ V} < V_{\text{IN}} \leq 5.5\text{ V}$ , $I_{\text{OUT}} = 1\text{ mA}$	–	0.05	0.20	%/V
$\text{Load}_{\text{Reg}}$	Load Regulation	$0\text{ mA} < I_{\text{OUT}} \leq 150\text{ mA}$ , $V_{\text{IN}} = 3.5\text{ V}$	–20	1	20	mV
$V_{\text{DO}}$	Dropout Voltage	$I_{\text{OUT}} = 150\text{ mA}$ (Note 16)	–	240	330	mV
$I_{\text{OUT}}$	Output Current	(Note 17)	150	–	–	mA
$I_{\text{SC}}$	Short Circuit Current Limit	$V_{\text{OUT}} = 0\text{ V}$	–	225	–	mA
$I_{\text{Q}}$	Quiescent Current	$I_{\text{OUT}} = 0\text{ mA}$	–	0.5	0.9	$\mu\text{A}$
$I_{\text{STB}}$	Standby Current	$V_{\text{EN}} = 0\text{ V}$ , $T_J = 25^{\circ}\text{C}$	–	0.1	0.5	$\mu\text{A}$
$V_{\text{ENH}}$	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
$V_{\text{ENL}}$	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
$I_{\text{EN}}$	EN Pull Down Current	$V_{\text{EN}} \leq V_{\text{IN}} \leq 5.5\text{ V}$ (Note 18)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	$f = 1\text{ kHz}$ , $V_{\text{IN}} = 3.5\text{ V} + 200\text{ mVpp}$ Modulation $I_{\text{OUT}} = 150\text{ mA}$	–	57	–	dB
$V_{\text{NOISE}}$	Output Noise Voltage	$V_{\text{IN}} = 5.5\text{ V}$ , $I_{\text{OUT}} = 1\text{ mA}$ $f = 100\text{ Hz}$ to $1\text{ MHz}$ , $C_{\text{OUT}} = 1\text{ }\mu\text{F}$	–	125	–	$\mu\text{V}_{\text{rms}}$
$R_{\text{LOW}}$	Active Output Discharge Resistance (A option only)	$V_{\text{IN}} = 5.5\text{ V}$ , $V_{\text{EN}} = 0\text{ V}$ (Note 18)	–	100	–	$\Omega$
$T_{\text{SD}}$	Thermal Shutdown Temperature	Temperature Increasing from $T_J = +25^{\circ}\text{C}$ (Note 18)	–	175	–	$^{\circ}\text{C}$
$T_{\text{SDH}}$	Thermal Shutdown Hysteresis	Temperature Falling from $T_{\text{SD}}$ (Note 18)	–	25	–	$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

15. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at  $T_J = T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

16. Characterized when  $V_{\text{OUT}}$  falls 75 mV below the regulated voltage and only for devices with  $V_{\text{OUT}} = 2.5\text{ V}$ .

17. Respect SOA.

18. Guaranteed by design and characterization.

# NCP170

## ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 2.8 V

( $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ;  $V_{\text{IN}} = 3.8\text{ V}$ ;  $I_{\text{OUT}} = 1\text{ mA}$ ,  $C_{\text{IN}} = C_{\text{OUT}} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}\text{C}$ .) (Note 19)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{\text{IN}}$	Operating Input Voltage		2.2	–	5.5	V
$V_{\text{OUT}}$	Output Voltage	$T_A = +25^{\circ}\text{C}$	2.772	2.8	2.828	V
		$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$	2.744	2.8	2.856	
$\text{Line}_{\text{Reg}}$	Line Regulation	$3.8\text{ V} < V_{\text{IN}} \leq 5.5\text{ V}$ , $I_{\text{OUT}} = 1\text{ mA}$	–	0.05	0.20	%/V
$\text{Load}_{\text{Reg}}$	Load Regulation	$0\text{ mA} < I_{\text{OUT}} \leq 150\text{ mA}$ , $V_{\text{IN}} = 3.8\text{ V}$	–20	1	20	mV
$V_{\text{DO}}$	Dropout Voltage	$I_{\text{OUT}} = 150\text{ mA}$ (Note 20)	–	210	300	mV
$I_{\text{OUT}}$	Output Current	(Note 21)	150	–	–	mA
$I_{\text{SC}}$	Short Circuit Current Limit	$V_{\text{OUT}} = 0\text{ V}$	–	195	–	mA
$I_{\text{Q}}$	Quiescent Current	$I_{\text{OUT}} = 0\text{ mA}$	–	0.5	0.9	$\mu\text{A}$
$I_{\text{STB}}$	Standby Current	$V_{\text{EN}} = 0\text{ V}$ , $T_J = 25^{\circ}\text{C}$	–	0.1	0.5	$\mu\text{A}$
$V_{\text{ENH}}$	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
$V_{\text{ENL}}$	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
$I_{\text{EN}}$	EN Pull Down Current	$V_{\text{EN}} \leq V_{\text{IN}} \leq 5.5\text{ V}$ (Note 22)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	$f = 1\text{ kHz}$ , $V_{\text{IN}} = 3.8\text{ V} + 200\text{ mVpp}$ Modulation $I_{\text{OUT}} = 150\text{ mA}$	–	40	–	dB
$V_{\text{NOISE}}$	Output Noise Voltage	$V_{\text{IN}} = 5.5\text{ V}$ , $I_{\text{OUT}} = 1\text{ mA}$ $f = 100\text{ Hz}$ to $1\text{ MHz}$ , $C_{\text{OUT}} = 1\text{ }\mu\text{F}$	–	125	–	$\mu\text{V}_{\text{rms}}$
$R_{\text{LOW}}$	Active Output Discharge Resistance (A option only)	$V_{\text{IN}} = 5.5\text{ V}$ , $V_{\text{EN}} = 0\text{ V}$ (Note 22)	–	100	–	$\Omega$
$T_{\text{SD}}$	Thermal Shutdown Temperature	Temperature Increasing from $T_J = +25^{\circ}\text{C}$ (Note 22)	–	175	–	$^{\circ}\text{C}$
$T_{\text{SDH}}$	Thermal Shutdown Hysteresis	Temperature Falling from $T_{\text{SD}}$ (Note 22)	–	25	–	$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

19. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at  $T_J = T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

20. Characterized when  $V_{\text{OUT}}$  falls 84 mV below the regulated voltage and only for devices with  $V_{\text{OUT}} = 2.8\text{ V}$ .

21. Respect SOA.

22. Guaranteed by design and characterization.

# NCP170

## ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 3.0 V

( $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ;  $V_{\text{IN}} = 4.0\text{ V}$ ;  $I_{\text{OUT}} = 1\text{ mA}$ ,  $C_{\text{IN}} = C_{\text{OUT}} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}\text{C}$ .) (Note 23)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{\text{IN}}$	Operating Input Voltage		2.2	–	5.5	V
$V_{\text{OUT}}$	Output Voltage	$T_A = +25^{\circ}\text{C}$	2.97	3.0	3.03	V
		$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$	2.94	3.0	3.06	
$\text{Line}_{\text{Reg}}$	Line Regulation	$4.0\text{ V} < V_{\text{IN}} \leq 5.5\text{ V}$ , $I_{\text{OUT}} = 1\text{ mA}$	–	0.05	0.20	%/V
$\text{Load}_{\text{Reg}}$	Load Regulation	$0\text{ mA} < I_{\text{OUT}} \leq 150\text{ mA}$ , $V_{\text{IN}} = 4\text{ V}$	–20	1	20	mV
$V_{\text{DO}}$	Dropout Voltage	$I_{\text{OUT}} = 150\text{ mA}$ (Note 24)	–	190	260	mV
$I_{\text{OUT}}$	Output Current	(Note 25)	150	–	–	mA
$I_{\text{SC}}$	Short Circuit Current Limit	$V_{\text{OUT}} = 0\text{ V}$	–	195	–	mA
$I_{\text{Q}}$	Quiescent Current	$I_{\text{OUT}} = 0\text{ mA}$	–	0.5	0.9	$\mu\text{A}$
$I_{\text{STB}}$	Standby Current	$V_{\text{EN}} = 0\text{ V}$ , $T_J = 25^{\circ}\text{C}$	–	0.1	0.5	$\mu\text{A}$
$V_{\text{ENH}}$	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
$V_{\text{ENL}}$	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
$I_{\text{EN}}$	EN Pull Down Current	$V_{\text{EN}} \leq V_{\text{IN}} \leq 5.5\text{ V}$ (Note 26)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	$f = 1\text{ kHz}$ , $V_{\text{IN}} = 4.0\text{ V} + 200\text{ mVpp}$ Modulation $I_{\text{OUT}} = 150\text{ mA}$	–	47	–	dB
$V_{\text{NOISE}}$	Output Noise Voltage	$V_{\text{IN}} = 5.5\text{ V}$ , $I_{\text{OUT}} = 1\text{ mA}$ $f = 100\text{ Hz to }1\text{ MHz}$ , $C_{\text{OUT}} = 1\text{ }\mu\text{F}$	–	120	–	$\mu\text{V}_{\text{rms}}$
$R_{\text{LOW}}$	Active Output Discharge Resistance (A option only)	$V_{\text{IN}} = 5.5\text{ V}$ , $V_{\text{EN}} = 0\text{ V}$ (Note 26)	–	100	–	$\Omega$
$T_{\text{SD}}$	Thermal Shutdown Temperature	Temperature Increasing from $T_J = +25^{\circ}\text{C}$ (Note 26)	–	175	–	$^{\circ}\text{C}$
$T_{\text{SDH}}$	Thermal Shutdown Hysteresis	Temperature Falling from $T_{\text{SD}}$ (Note 26)	–	25	–	$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

23. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at  $T_J = T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

24. Characterized when  $V_{\text{OUT}}$  falls 90 mV below the regulated voltage and only for devices with  $V_{\text{OUT}} = 3.0\text{ V}$ .

25. Respect SOA.

26. Guaranteed by design and characterization.



# NCP170

## ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 3.3 V

( $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ;  $V_{IN} = 4.3\text{ V}$ ;  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}\text{C}$ .) (Note 27)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IN}$	Operating Input Voltage		2.2	–	5.5	V
$V_{OUT}$	Output Voltage	$T_A = +25^{\circ}\text{C}$	3.267	3.3	3.333	V
		$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$	3.234	3.3	3.366	
$\text{Line}_{\text{Reg}}$	Line Regulation	$4.3\text{ V} < V_{IN} \leq 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$	–	0.05	0.20	%/V
$\text{Load}_{\text{Reg}}$	Load Regulation	$0\text{ mA} < I_{OUT} \leq 150\text{ mA}$ , $V_{IN} = 4.3\text{ V}$	–20	1	20	mV
$V_{DO}$	Dropout Voltage	$I_{OUT} = 150\text{ mA}$ (Note 28)	–	180	250	mV
$I_{OUT}$	Output Current	(Note 29)	150	–	–	mA
$I_{SC}$	Short Circuit Current Limit	$V_{OUT} = 0\text{ V}$	–	195	–	mA
$I_Q$	Quiescent Current	$I_{OUT} = 0\text{ mA}$	–	0.5	0.9	$\mu\text{A}$
$I_{STB}$	Standby Current	$V_{EN} = 0\text{ V}$ , $T_J = 25^{\circ}\text{C}$	–	0.1	0.5	$\mu\text{A}$
$V_{ENH}$	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
$V_{ENL}$	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
$I_{EN}$	EN Pull Down Current	$V_{EN} \leq V_{IN} \leq 5.5\text{ V}$ (Note 30)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	$f = 1\text{ kHz}$ , $V_{IN} = 4.3\text{ V} + 200\text{ mVpp}$ Modulation $I_{OUT} = 150\text{ mA}$	–	41	–	dB
$V_{NOISE}$	Output Noise Voltage	$V_{IN} = 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$ $f = 100\text{ Hz to }1\text{ MHz}$ , $C_{OUT} = 1\text{ }\mu\text{F}$	–	125	–	$\mu\text{V}_{\text{rms}}$
$R_{LOW}$	Active Output Discharge Resistance (A option only)	$V_{IN} = 5.5\text{ V}$ , $V_{EN} = 0\text{ V}$ (Note 30)	–	100	–	$\Omega$
$T_{SD}$	Thermal Shutdown Temperature	Temperature Increasing from $T_J = +25^{\circ}\text{C}$ (Note 30)	–	175	–	$^{\circ}\text{C}$
$T_{SDH}$	Thermal Shutdown Hysteresis	Temperature Falling from $T_{SD}$ (Note 30)	–	25	–	$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

27. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at  $T_J = T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

28. Characterized when  $V_{OUT}$  falls 99 mV below the regulated voltage and only for devices with  $V_{OUT} = 3.3\text{ V}$ .

29. Respect SOA.

30. Guaranteed by design and characterization.

# NCP170

## ELECTRICAL CHARACTERISTICS – VOLTAGE VERSION 3.6 V

( $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ ;  $V_{IN} = 4.6\text{ V}$ ;  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}\text{C}$ .) (Note 31)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IN}$	Operating Input Voltage		2.2	–	5.5	V
$V_{OUT}$	Output Voltage	$T_A = +25^{\circ}\text{C}$	3.564	3.6	3.636	V
		$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$	3.528	3.6	3.672	
$\text{Line}_{\text{Reg}}$	Line Regulation	$4.6\text{ V} < V_{IN} \leq 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$	–	0.05	0.20	%/V
$\text{Load}_{\text{Reg}}$	Load Regulation	$0\text{ mA} < I_{OUT} \leq 150\text{ mA}$ , $V_{IN} = 4.6\text{ V}$	–20	1	20	mV
$V_{DO}$	Dropout Voltage	$I_{OUT} = 150\text{ mA}$ (Note 32)	–	170	240	mV
$I_{OUT}$	Output Current	(Note 33)	150	–	–	mA
$I_{SC}$	Short Circuit Current Limit	$V_{OUT} = 0\text{ V}$	–	195	–	mA
$I_Q$	Quiescent Current	$I_{OUT} = 0\text{ mA}$	–	0.5	0.9	$\mu\text{A}$
$I_{STB}$	Standby Current	$V_{EN} = 0\text{ V}$ , $T_J = 25^{\circ}\text{C}$	–	0.1	0.5	$\mu\text{A}$
$V_{ENH}$	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2	–	–	V
$V_{ENL}$	EN Pin Threshold Voltage	EN Input Voltage “L”	–	–	0.4	V
$I_{EN}$	EN Pull Down Current	$V_{EN} \leq V_{IN} \leq 5.5\text{ V}$ (Note 34)	–	10	–	nA
PSRR	Power Supply Rejection Ratio	$f = 1\text{ kHz}$ , $V_{IN} = 4.6\text{ V} + 200\text{ mVpp}$ Modulation $I_{OUT} = 150\text{ mA}$	–	30	–	dB
$V_{NOISE}$	Output Noise Voltage	$V_{IN} = 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$ $f = 100\text{ Hz to }1\text{ MHz}$ , $C_{OUT} = 1\text{ }\mu\text{F}$	–	130	–	$\mu\text{V}_{\text{rms}}$
$R_{LOW}$	Active Output Discharge Resistance (A option only)	$V_{IN} = 5.5\text{ V}$ , $V_{EN} = 0\text{ V}$ (Note 34)	–	100	–	
$T_{SD}$	Thermal Shutdown Temperature	Temperature Increasing from $T_J = +25^{\circ}\text{C}$ (Note 34)	–	175	–	$^{\circ}\text{C}$
$T_{SDH}$	Thermal Shutdown Hysteresis	Temperature Falling from $T_{SD}$ (Note 34)	–	25	–	$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

31. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at  $T_J = T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

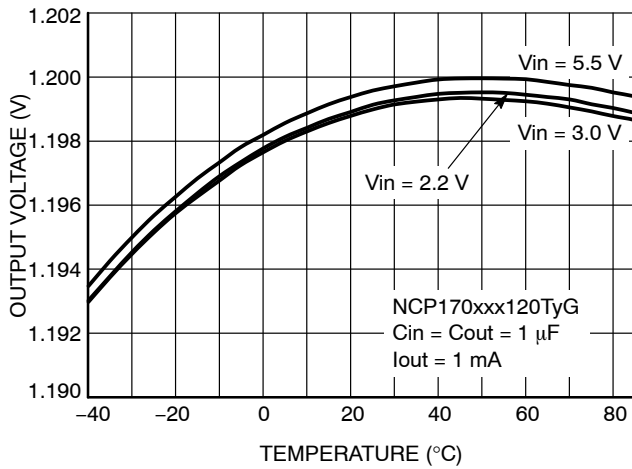
32. Characterized when  $V_{OUT}$  falls 108 mV below the regulated voltage and only for devices with  $V_{OUT} = 3.6\text{ V}$ .

33. Respect SOA.

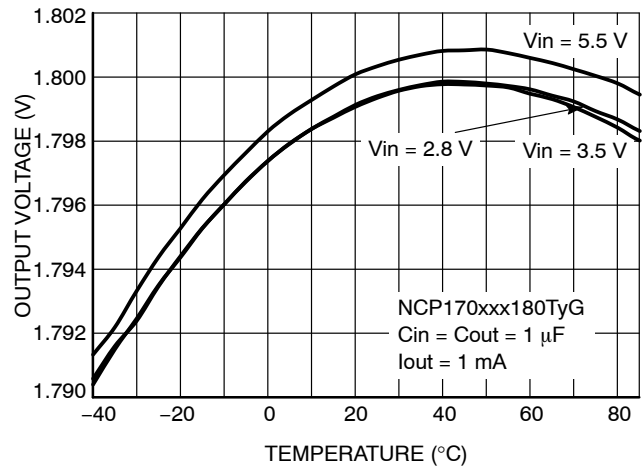
34. Guaranteed by design and characterization.

# NCP170

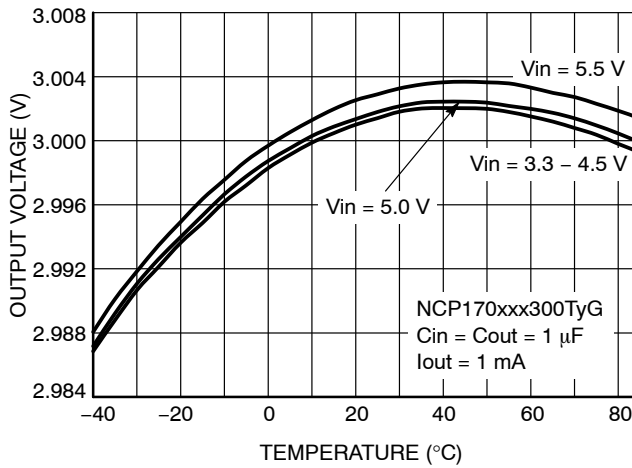
## TYPICAL CHARACTERISTICS



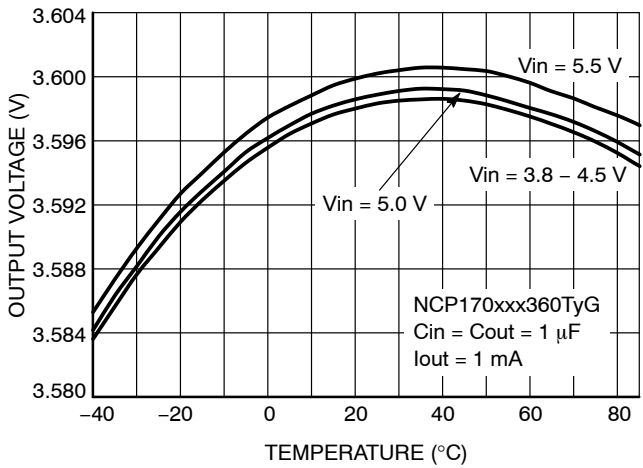
**Figure 3. Output Voltage vs. Temperature,  
 $V_{out} = 1.2\text{ V}$**



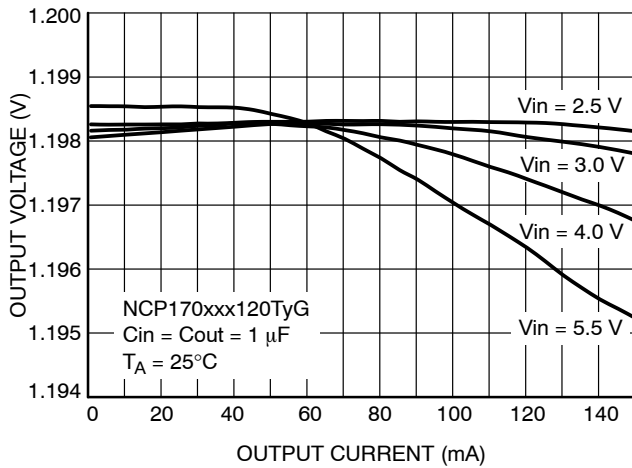
**Figure 4. Output Voltage vs. Temperature,  
 $V_{out} = 1.8\text{ V}$**



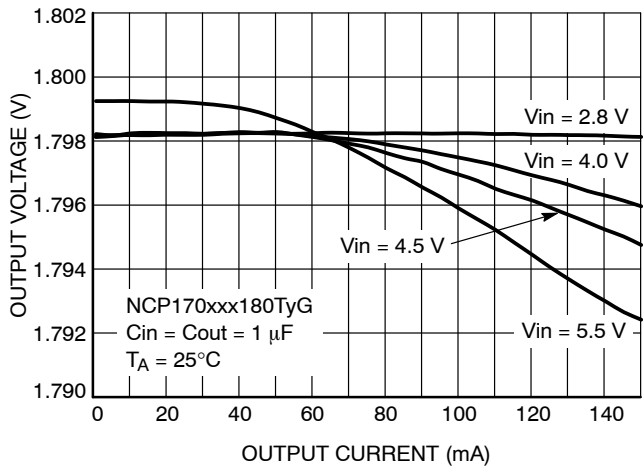
**Figure 5. Output Voltage vs. Temperature,  
 $V_{out} = 3.0\text{ V}$**



**Figure 6. Output Voltage vs. Temperature,  
 $V_{out} = 3.6\text{ V}$**



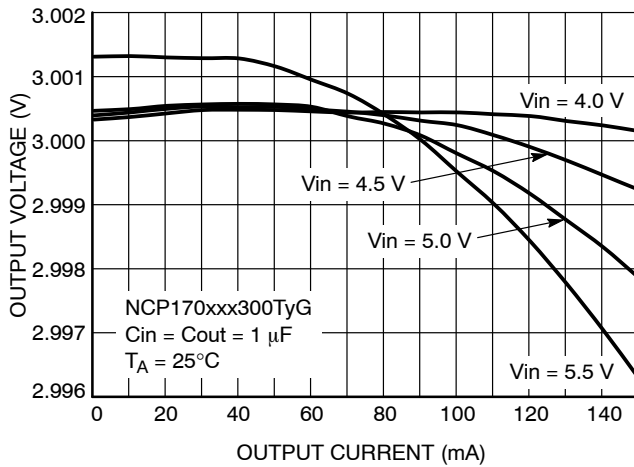
**Figure 7. Output Voltage vs. Output Current,  
 $V_{out} = 1.2\text{ V}$**



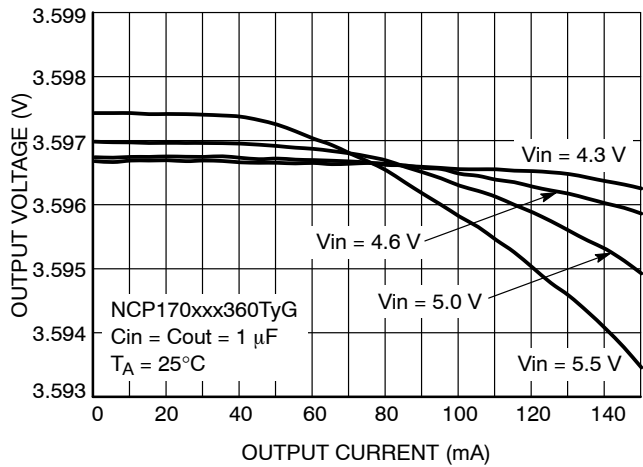
**Figure 8. Output Voltage vs. Output Current,  
 $V_{out} = 1.8\text{ V}$**

# NCP170

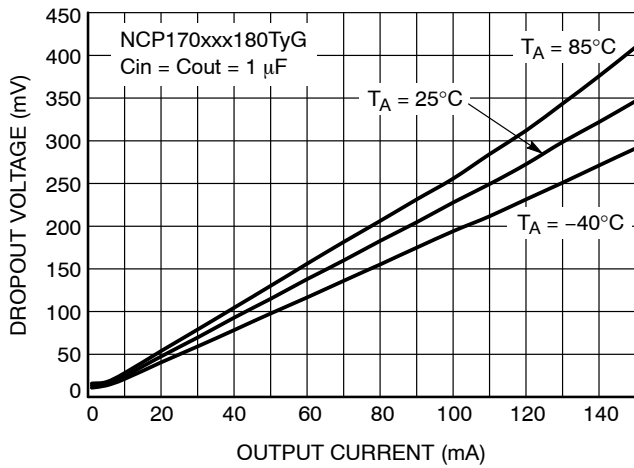
## TYPICAL CHARACTERISTICS



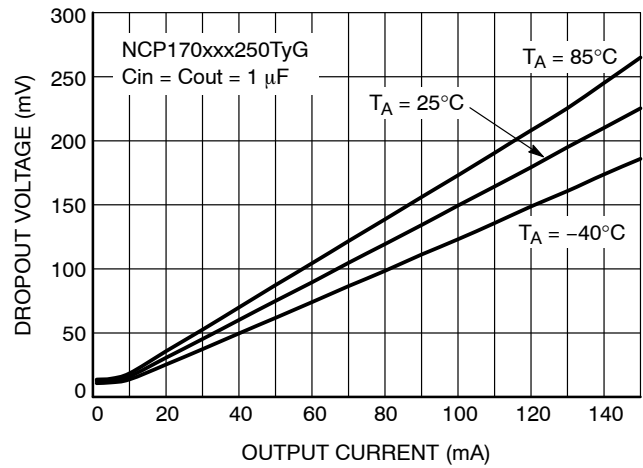
**Figure 9. Output Voltage vs. Output Current,  
Vout = 3.0 V**



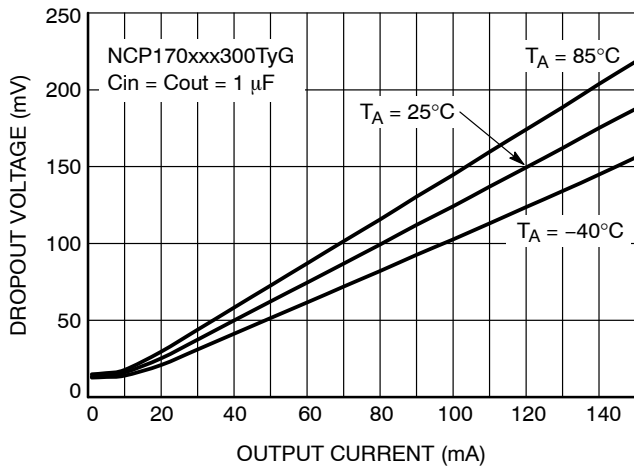
**Figure 10. Output Voltage vs. Output Current,  
Vout = 3.6 V**



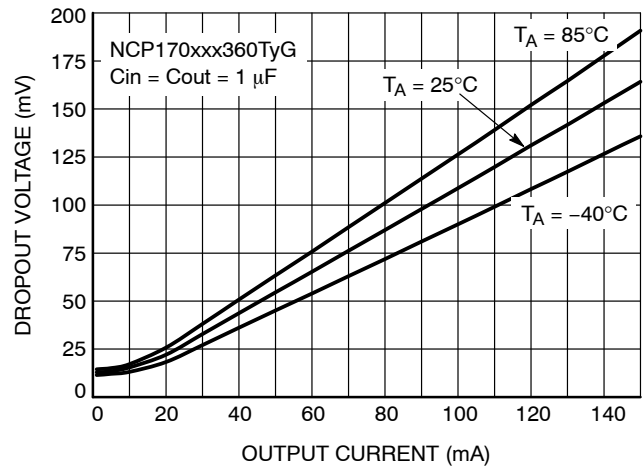
**Figure 11. Dropout Voltage vs. Output Current,  
Vout = 1.8 V**



**Figure 12. Dropout Voltage vs. Output Current,  
Vout = 2.5 V**



**Figure 13. Dropout Voltage vs. Output Current,  
Vout = 3.0 V**



**Figure 14. Dropout Voltage vs. Output Current,  
Vout = 3.6 V**

TYPICAL CHARACTERISTICS

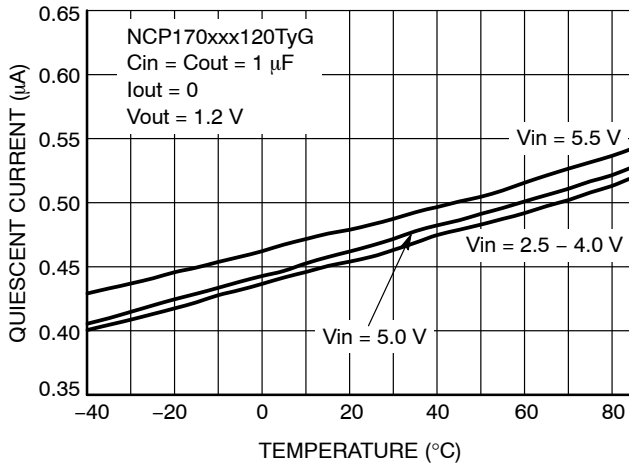


Figure 15. Quiescent Current vs. Temperature, Vout = 1.2 V

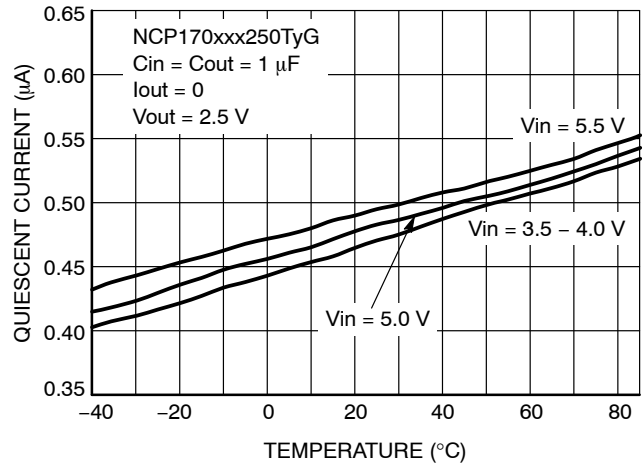


Figure 16. Quiescent Current vs. Temperature, Vout = 2.5 V

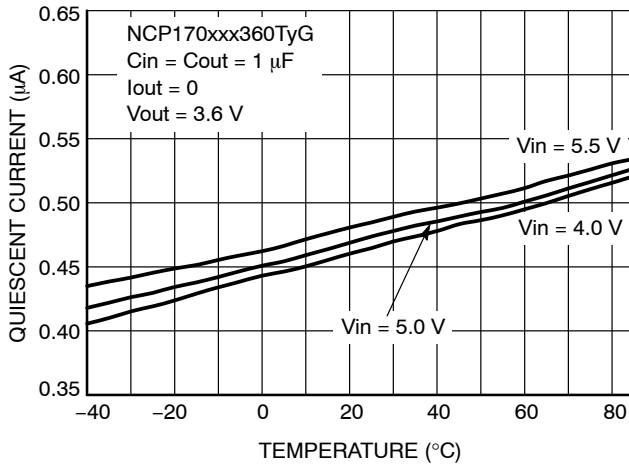


Figure 17. Quiescent Current vs. Temperature, Vout = 3.6 V

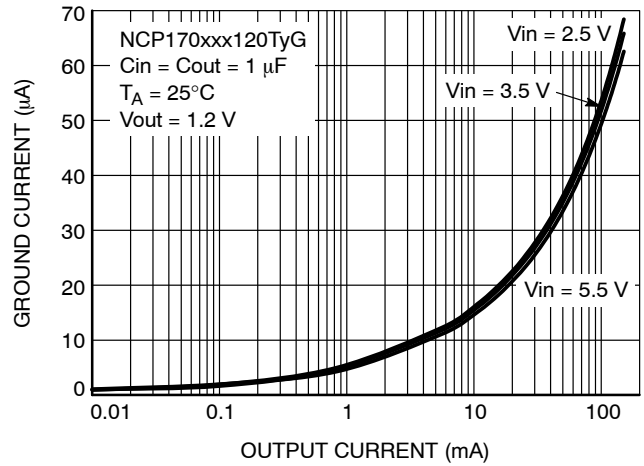


Figure 18. Ground Current vs. Output Current, Vout = 1.2 V

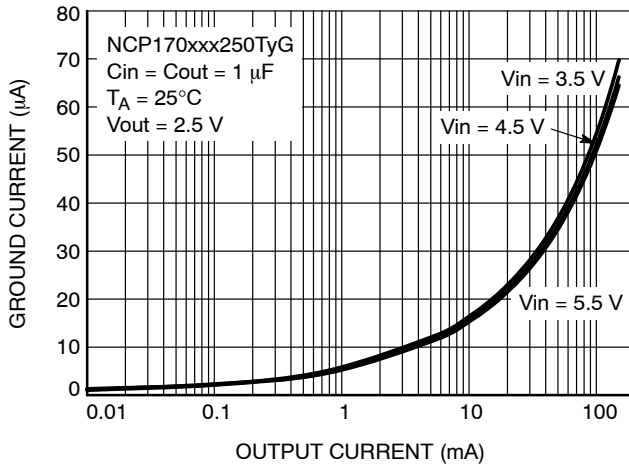


Figure 19. Ground Current vs. Output Current, Vout = 2.5 V

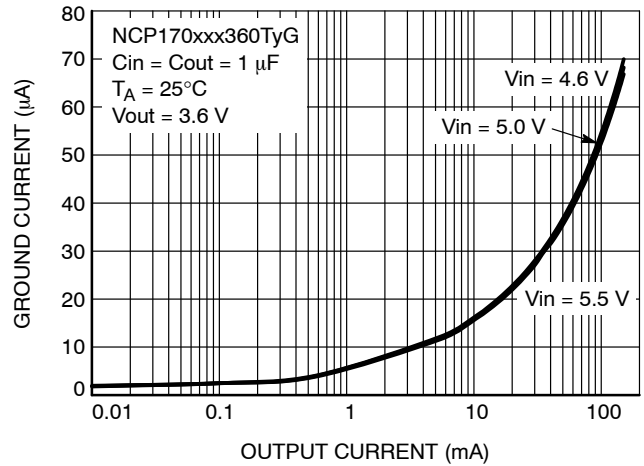


Figure 20. Ground Current vs. Output Current, Vout = 3.6 V

# NCP170

## TYPICAL CHARACTERISTICS

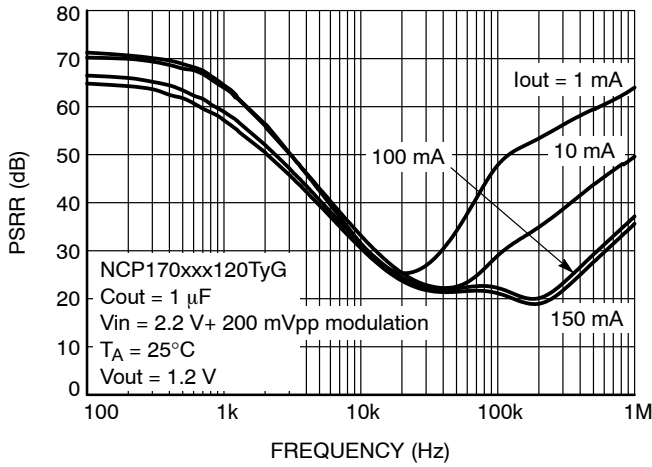


Figure 21. PSRR vs. Frequency,  $V_{out} = 1.2 V$

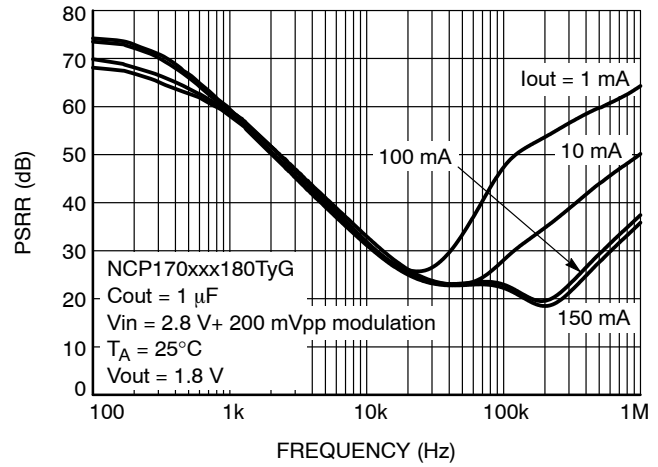


Figure 22. PSRR vs. Frequency,  $V_{out} = 1.8 V$

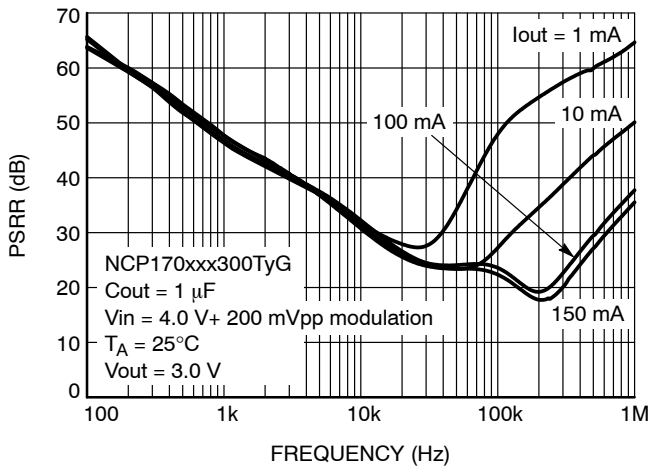


Figure 23. PSRR vs. Frequency,  $V_{out} = 3.0 V$

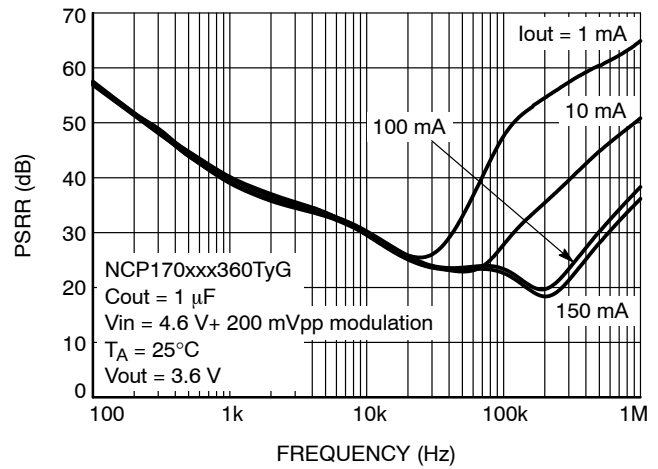


Figure 24. PSRR vs. Frequency,  $V_{out} = 3.6 V$

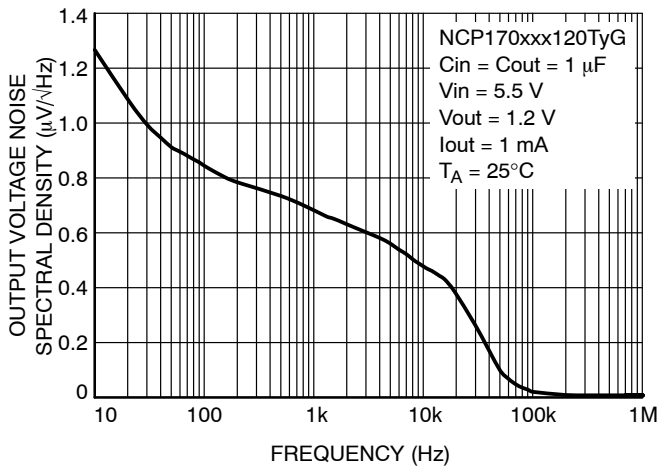


Figure 25. Output Voltage Noise Spectral Density,  $V_{out} = 1.2 V$

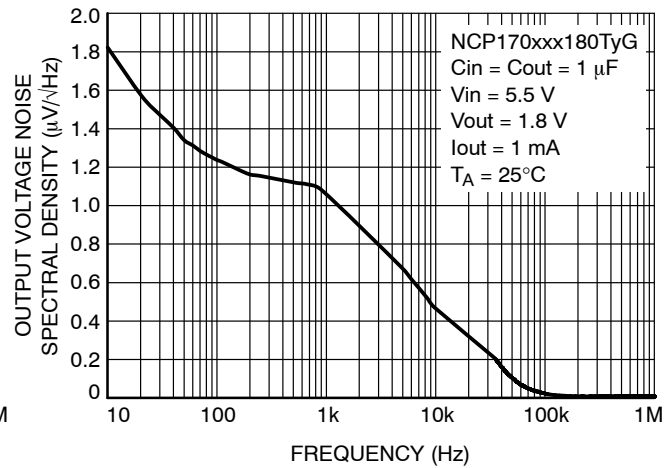
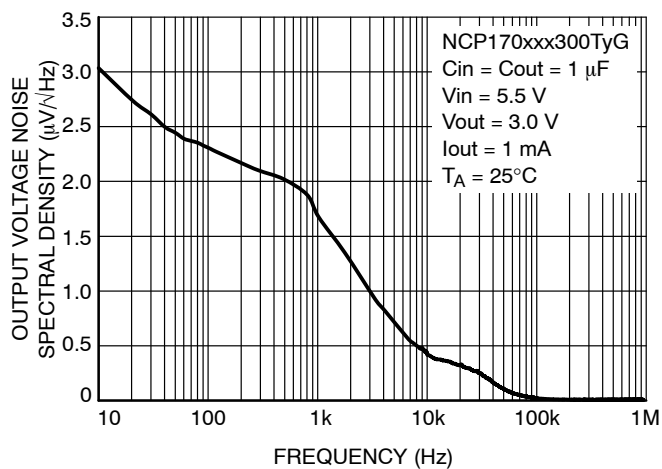


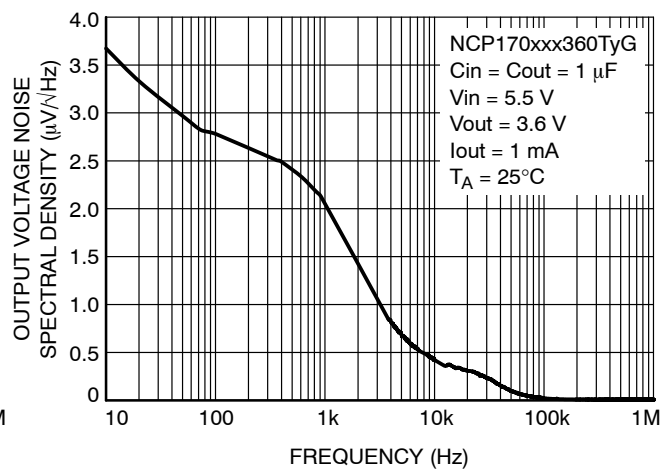
Figure 26. Output Voltage Noise Spectral Density,  $V_{out} = 1.8 V$

# NCP170

## TYPICAL CHARACTERISTICS



**Figure 27. Output Voltage Noise Spectral Density,  $V_{out} = 3.0 \text{ V}$**



**Figure 28. Output Voltage Noise Spectral Density,  $V_{out} = 3.6 \text{ V}$**

# NCP170

## TYPICAL CHARACTERISTICS

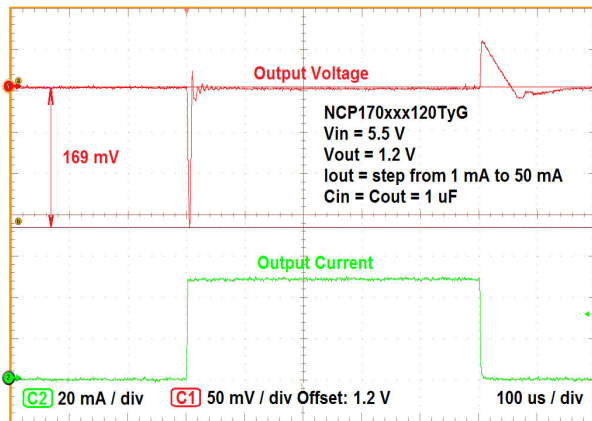


Figure 29. Load Transient Response at Load Step from 1 mA to 50 mA, Vout = 1.2 V

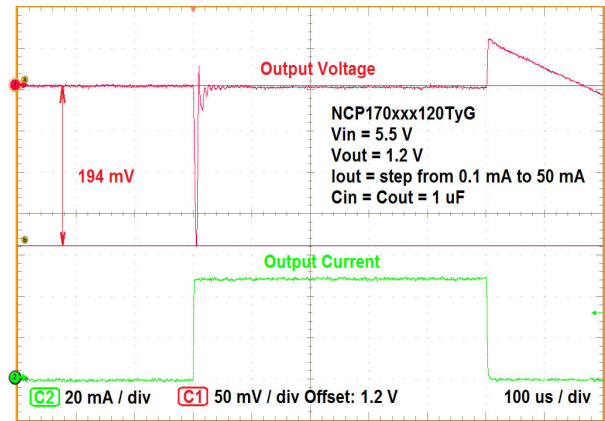


Figure 30. Load Transient Response at Load Step from 0.1 mA to 50 mA, Vout = 1.2 V

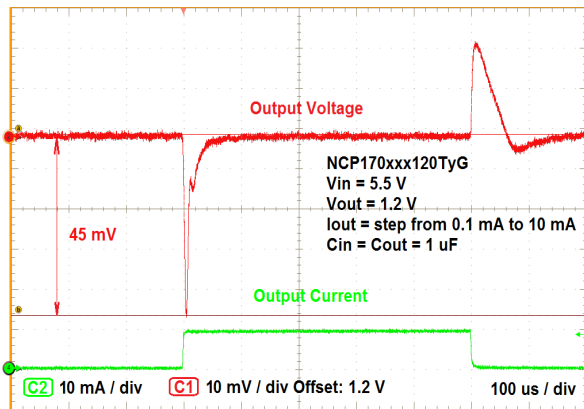


Figure 31. Load Transient Response at Load Step from 0.1 mA to 10 mA, Vout = 1.2 V

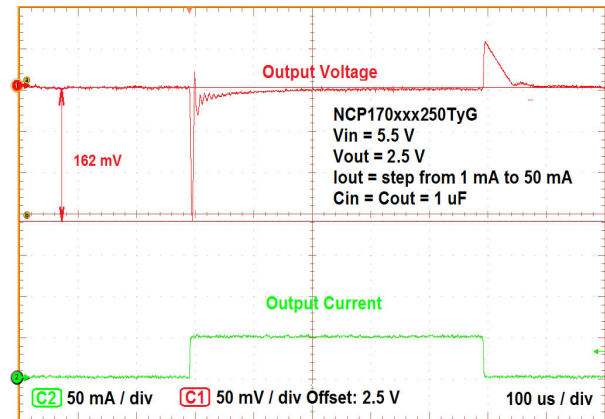


Figure 32. Load Transient Response at Load Step from 1 mA to 50 mA, Vout = 2.5 V

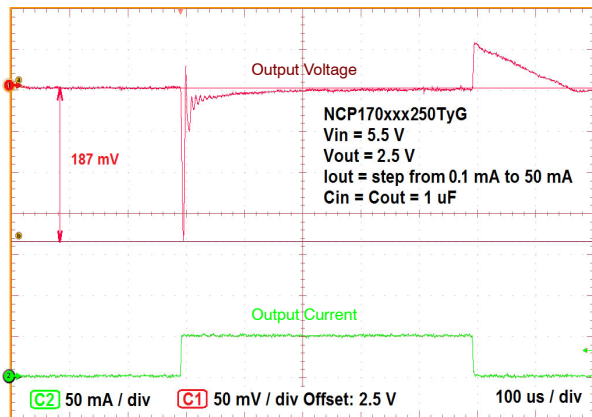


Figure 33. Load Transient Response at Load Step from 0.1 mA to 50 mA, Vout = 2.5 V

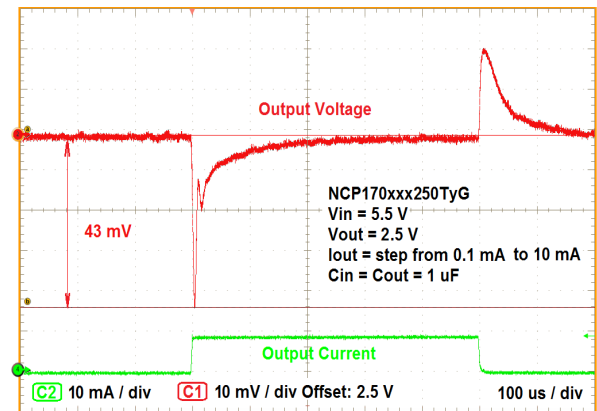


Figure 34. Load Transient Response at Load Step from 0.1 mA to 10 mA, Vout = 2.5 V



# NCP170

## TYPICAL CHARACTERISTICS

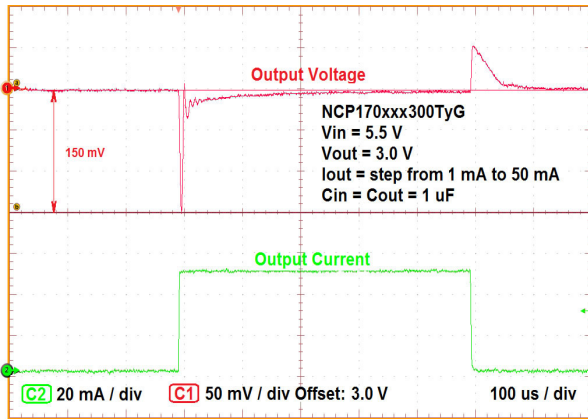


Figure 35. Load Transient Response at Load Step from 1mA to 50 mA, Vout= 3.0 V

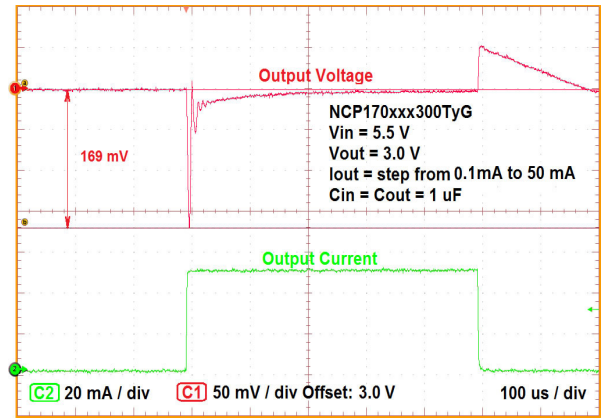


Figure 36. Load Transient Response at Load Step from 0.1 mA to 50 mA, Vout = 3.0 V

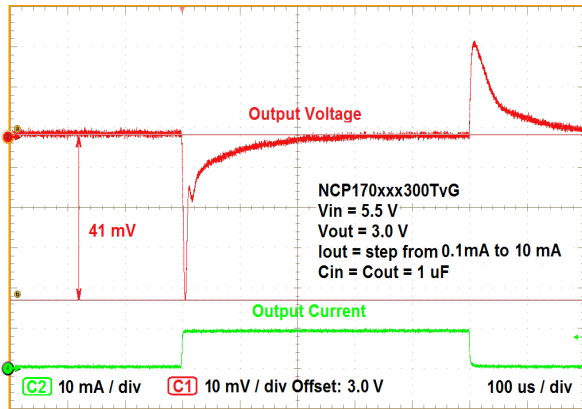


Figure 37. Load Transient Response at Load Step from 0.1 mA to 10 mA, Vout = 3.0 V

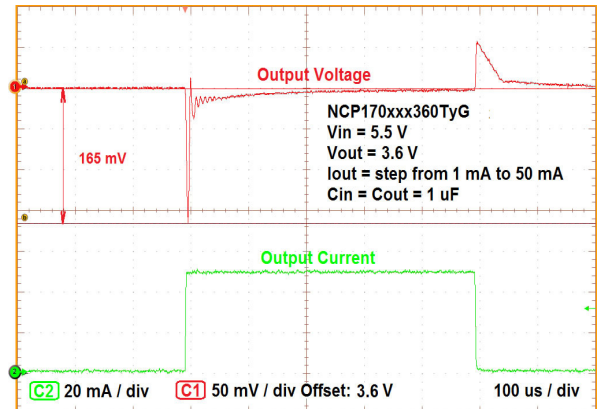


Figure 38. Load Transient Response at Load Step from 1 mA to 50 mA, Vout = 3.6 V

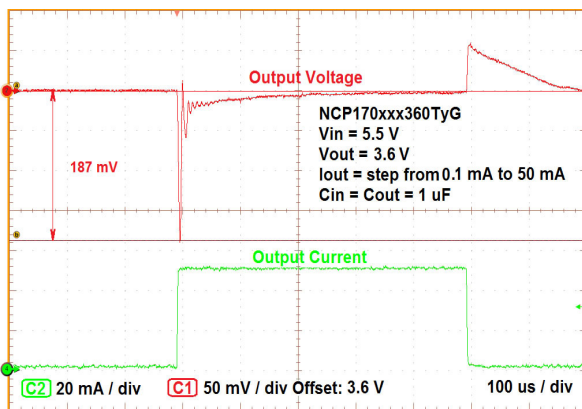


Figure 39. Load Transient Response at Load Step from 0.1 mA to 50 mA, Vout = 3.6 V

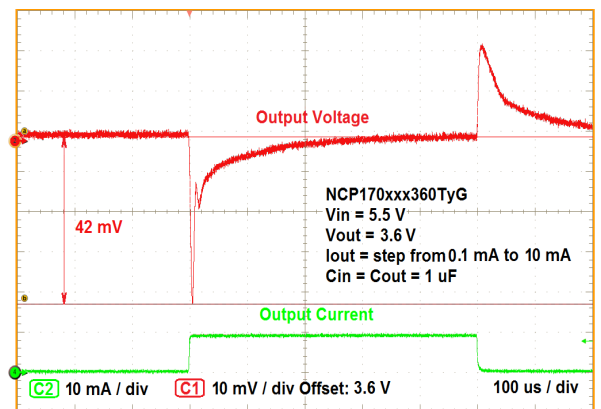


Figure 40. Load Transient Response at Load Step from 0.1 mA to 10 mA, Vout = 3.6 V

# NCP170

## TYPICAL CHARACTERISTICS

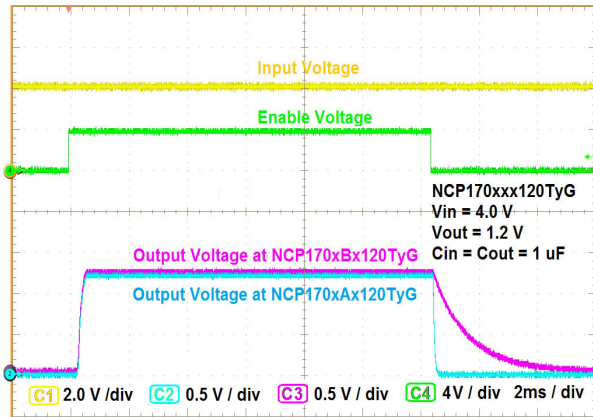


Figure 41. Output Voltage with and without Active Discharge Feature, Vout = 1.2 V

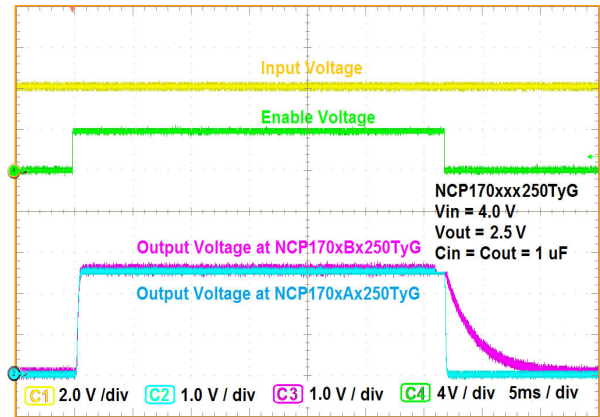


Figure 42. Output Voltage with and without Active Discharge Feature, Vout = 2.5 V

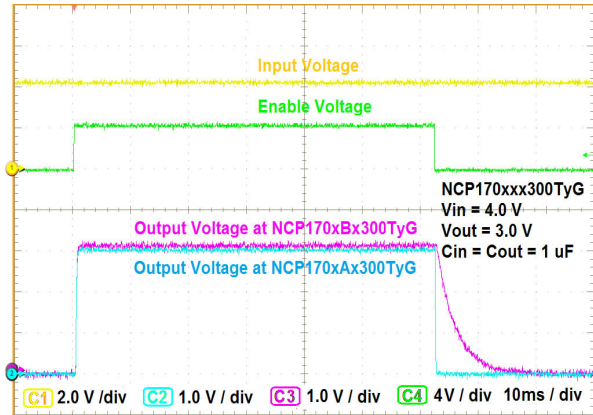


Figure 43. Output Voltage with and without Active Discharge Feature, Vout = 3.0 V

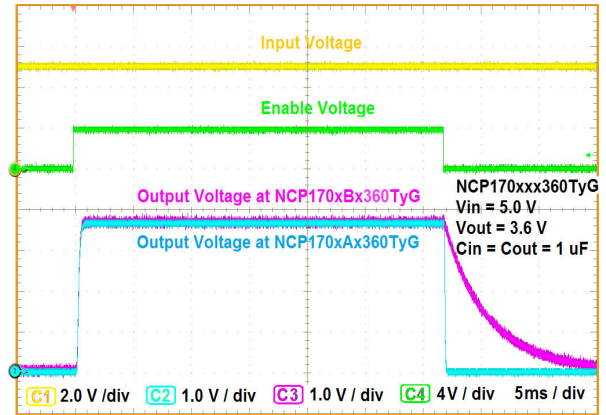


Figure 44. Output Voltage with and without Active Discharge Feature, Vout = 3.6 V

# NCP170

## TYPICAL CHARACTERISTICS

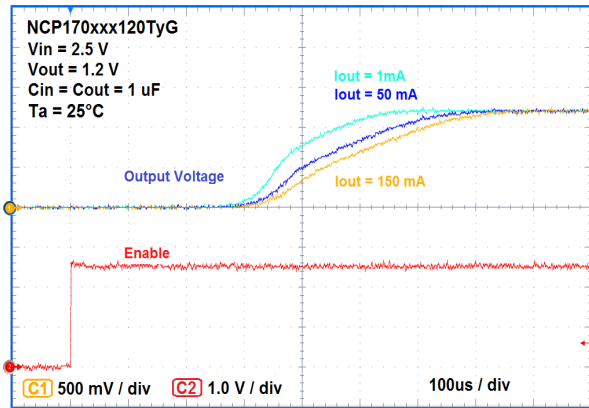


Figure 45. Enable Turn-on Response at  $V_{out} = 1.2\text{ V}$

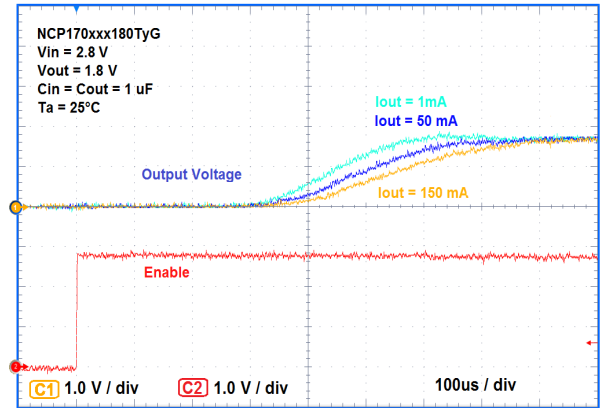


Figure 46. Enable Turn-on Response at  $V_{out} = 1.8\text{ V}$

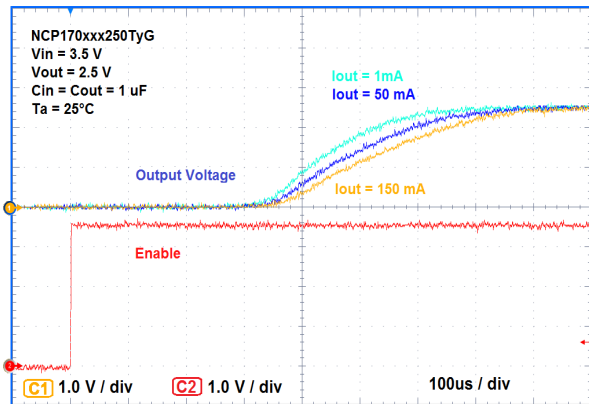


Figure 47. Enable Turn-on Response at  $V_{out} = 2.5\text{ V}$

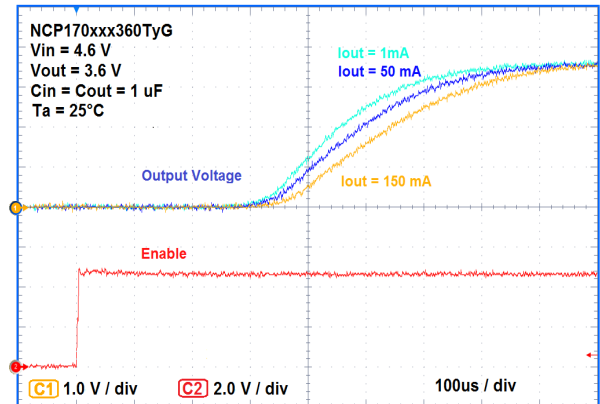


Figure 48. Enable Turn-on Response at  $V_{out} = 3.6\text{ V}$

## APPLICATIONS INFORMATION

### General

The NCP170 is a high performance 150 mA Linear Regulator with Ultra Low IQ. This device delivers low Noise and high Power Supply Rejection Ratio with excellent dynamic performance due to employing the Dynamic Quiescent Current adjustment which assure ultra low  $I_Q$  consumption at no – load state. These parameters make this device very suitable for various battery powered applications.

### Input Decoupling ( $C_{IN}$ )

It is recommended to connect at least a 1  $\mu$ F Ceramic X5R or X7R capacitor between IN and GND pins of the device. This capacitor will provide a low impedance path for any unwanted AC signals or Noise superimposed onto constant Input Voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes.

Higher capacitance and lower ESR Capacitors will improve the overall line transient response.

### Output Decoupling ( $C_{OUT}$ )

The NCP170 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of 1.0  $\mu$ F or greater up to 10  $\mu$ F. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended. There is recommended connect the output capacitor as close as possible to the output pin of the regulator.

### Enable Operation

The NCP170 uses the EN pin to enable /disable its device and to activate /deactivate the active discharge function at devices with this feature. If the EN pin voltage is pulled below 0.4 V the device is guaranteed to be disable. The active discharge transistor at the devices with Active Discharge Feature is activated and the output voltage  $V_{OUT}$  is pulled to GND through an internal circuitry with effective resistance about 100 ohms.

If the EN pin voltage is higher than 1.2 V the device is guaranteed to be enabled. The internal active discharge circuitry is switched off and the desired output voltage is

available at output pin. In case the Enable function is not required the EN pin should be connected directly to input pin.

### Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown point ( $T_{SD} = 175^\circ\text{C}$  typical) the device goes to disabled state and the output voltage is not delivered until the die temperature decreases to  $150^\circ\text{C}$ . The Thermal Shutdown feature provides a protection from a catastrophic device failure at accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

### Power Dissipation and Heat sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation, junction temperature should be limited to  $+125^\circ\text{C}$ . The maximum power dissipation the NCP170 device can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad (\text{eq. 1})$$

The power dissipated by the NCP170 device for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND} + I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}) \quad (\text{eq. 2})$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + (V_{OUT} \times I_{OUT})}{I_{OUT} + I_{GND}} \quad (\text{eq. 3})$$

### Hints

$V_{IN}$  and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCP170, and make traces as short as possible.

# NCP170

## ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Active Discharge	Package	Shipping <sup>†</sup>
NCP170AMX120TCG	1.2	AC	Yes	XDFN4 1.0 × 1.0 (Pb-Free)	3000 / Tape & Reel
NCP170AMX135TCG	1.35	AP			
NCP170AMX150TCG	1.5	AJ			
NCP170AMX170TCG	1.7	AT			
NCP170AMX180TBG	1.8	AD			
NCP170AMX180TCG	1.8	AD			
NCP170AMX190TCG	1.9	AL			
NCP170AMX250TCG	2.5	AE			
NCP170AMX280TBG	2.8	AF			
NCP170AMX280TCG	2.8	AF			
NCP170AMX285TCG	2.85	AK			
NCP170AMX300TBG	3.0	AA			
NCP170AMX300TCG	3.0	AA			
NCP170AMX310TCG	3.1	AN			
NCP170AMX320TCG	3.2	AQ			
NCP170AMX330TBG	3.3	AG			
NCP170AMX330TCG	3.3	AG			
NCP170AMX360TCG	3.6	AM			
NCP170BMX120TCG	1.2	2C	No		
NCP170BMX135TCG	1.35	2P			
NCP170BMX150TCG	1.5	2J			
NCP170BMX170TCG	1.7	2T			
NCP170BMX180TCG	1.8	2D			
NCP170BMX190TCG	1.9	2L			
NCP170BMX250TCG	2.5	2E			
NCP170BMX280TCG	2.8	2F			
NCP170BMX285TCG	2.85	2K			
NCP170BMX300TCG	3.0	2A			
NCP170BMX310TCG	3.1	2N			
NCP170BMX320TCG	3.2	2Q			
NCP170BMX330TCG	3.3	2G			
NCP170BMX360TCG	3.6	2M			

# NCP170

## ORDERING INFORMATION

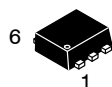
Device	Nominal Output Voltage	Marking	Active Discharge	Package	Shipping <sup>†</sup>
NCP170AXV120T2G	1.2	AC	Yes	SOT-563 (Pb-Free)	4000 / Tape & Reel (Available Soon)
NCP170AXV135T2G	1.35	AL			
NCP170AXV150T2G	1.5	AJ			
NCP170AXV180T2G	1.8	AD			
NCP170AXV190T2G	1.9	AM			
NCP170AXV210T2G	2.1	AK			
NCP170AXV250T2G	2.5	AE			
NCP170AXV280T2G	2.8	AF			
NCP170AXV300T2G	3.0	AA			
NCP170AXV310T2G	3.1	AN			
NCP170AXV330T2G	3.3	AH			
NCP170AXV360T2G	3.6	AG			
NCP170BXV120T2G	1.2	2C	No		
NCP170BXV135T2G	1.35	2L			
NCP170BXV150T2G	1.5	2J			
NCP170BXV180T2G	1.8	2D			
NCP170BXV190T2G	1.9	2M			
NCP170BXV250T2G	2.5	2E			
NCP170BXV280T2G	2.8	2F			
NCP170BXV300T2G	3.0	2A			
NCP170BXV310T2G	3.1	2N			
NCP170BXV330T2G	3.3	2H			
NCP170ASN120T2G	1.2	GCG	Yes	TSOP-5 (Pb-Free)	3000 / Tape & Reel (Available Soon)
NCP170ASN150T2G	1.5	GCH			
NCP170ASN180T2G	1.8	GCF			
NCP170ASN250T2G	2.5	GCE			
NCP170ASN280T2G	2.8	GCA			
NCP170ASN300T2G	3.0	GCC			
NCP170ASN330T2G	3.3	GCD			

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



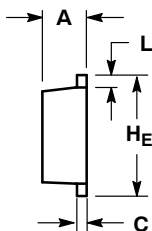
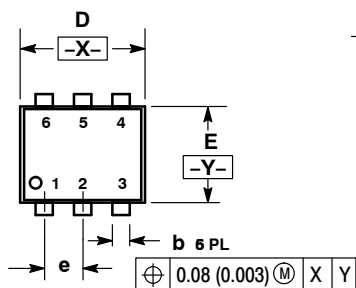
SCALE 4:1

### SOT-563, 6 LEAD

#### CASE 463A

#### ISSUE G

DATE 23 SEP 2015



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H <sub>E</sub>	1.50	1.60	1.70	0.059	0.062	0.066

#### STYLE 1:

- PIN 1. EMITTER 1  
2. BASE 1  
3. COLLECTOR 2  
4. EMITTER 2  
5. BASE 2  
6. COLLECTOR 1

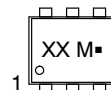
#### STYLE 2:

- PIN 1. EMITTER 1  
2. EMITTER 2  
3. BASE 2  
4. COLLECTOR 2  
5. BASE 1  
6. COLLECTOR 1

#### STYLE 3:

- PIN 1. CATHODE 1  
2. CATHODE 1  
3. ANODE/ANODE 2  
4. CATHODE 2  
5. CATHODE 2  
6. ANODE/ANODE 1

### GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code  
M = Month Code  
■ = Pb-Free Package

#### STYLE 4:

- PIN 1. COLLECTOR  
2. COLLECTOR  
3. BASE  
4. EMITTER  
5. COLLECTOR  
6. COLLECTOR

#### STYLE 5:

- PIN 1. CATHODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. CATHODE  
6. CATHODE

#### STYLE 6:

- PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE

#### STYLE 7:

- PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. ANODE  
6. CATHODE

#### STYLE 8:

- PIN 1. DRAIN  
2. DRAIN  
3. GATE  
4. SOURCE  
5. DRAIN  
6. DRAIN

#### STYLE 9:

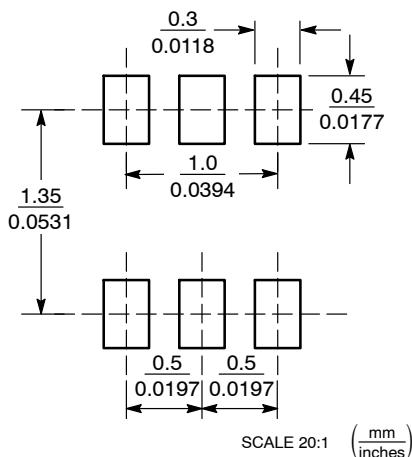
- PIN 1. SOURCE 1  
2. GATE 1  
3. DRAIN 2  
4. SOURCE 2  
5. GATE 2  
6. DRAIN 1

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

#### STYLE 10:

- PIN 1. CATHODE 1  
2. N/C  
3. CATHODE 2  
4. ANODE 2  
5. N/C  
6. ANODE 1

### SOLDERING FOOTPRINT\*

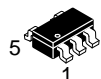


SCALE 20:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON11126D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-563, 6 LEAD	PAGE 1 OF 1

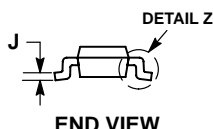
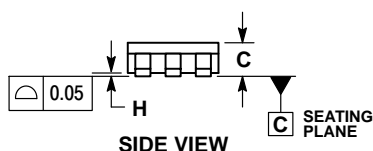
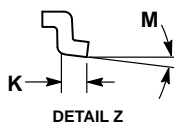
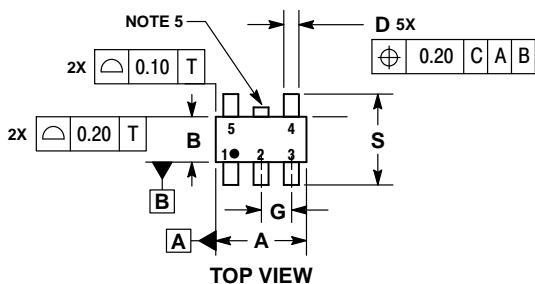
ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.



SCALE 2:1

### TSOP-5 CASE 483 ISSUE M

DATE 17 MAY 2016

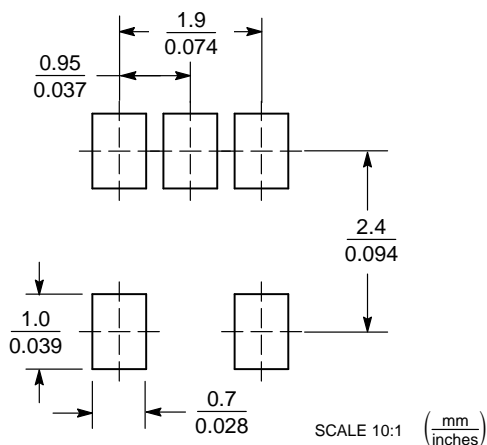


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

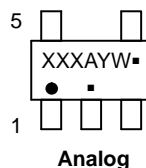
DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

#### SOLDERING FOOTPRINT\*

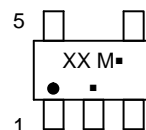


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### GENERIC MARKING DIAGRAM\*



Analog



Discrete/Logic

XXX = Specific Device Code    XX = Specific Device Code  
A = Assembly Location    M = Date Code  
Y = Year    ■ = Pb-Free Package  
W = Work Week  
■ = Pb-Free Package

(Note: Microdot may be in either location)


\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TSOP-5	
		PAGE 1 OF 2





ISSUE	REVISION	DATE
O	INITIATED NEW MECHANICAL OUTLINE #483. REQ BY WL CHIN/L. RENNICK.	28 OCT 1998
A	UPDATE OUTLINE DRAWING TO CORRECT DIN "C" (SHOULD BE FROM TIP OF LID TO TOP OF PKG). DIM IN TABLE INCORRECTLY LISTED TO G, F TO H, H TO J, N TO L & R TO M. REQ BY F. PADILLA	13 NOV 1998
B	CHANGE OF LEGAL OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. REQ BY A. GARLINGTON	20 APR 2001
C	ADDED NOTE "4". REQ BY S. RIGGS	27 JUN 2003
D	ADDED FOOTPRINT INFORMATION. UPDATED MARKING. REQ. BY D. JOERSZ	07 APR 2005
E	CHANGED DEVICE MARKING FROM AWW TO AYW. REQ. BY J. MANES.	14 SEP 2005
F	UPDATED DRAWINGS TO LATEST JEDEC STANDARDS. ADDED NOTE 5. REQ. BY T. GURNETT.	07 JUN 2006
G	ADDED MARKING DIAGRAM FOR IC OPTION. REQ. BY J. MILLER.	21 FEB 2007
H	CORRECTED MARKING DIAGRAM ERROR BY REVERSING ANALOG AND DISCRETE LABELS. REQ. BY GK SUA.	18 MAY 2007
J	CHANGED NOTE 4. REQ. BY A. GARLINGTON.	13 MAR 2013
K	REMOVED DIMENSION L AND ADDED DATUMS A AND B TO TOP VIEW. REQ. BY A. GARLINGTON.	19 APR 2013
L	REMOVED -02 FROM CASE CODE VARIANT. REQ. BY N. CALZADA.	23 SEP 2015
M	CHANGED DIMENSIONS A & B FROM BASIC TO MIN AND MAX VALUES. REQ. BY A. GARLINGTON.	17 MAY 2016

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

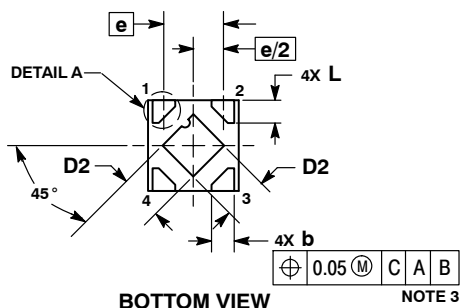
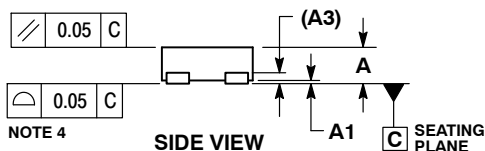
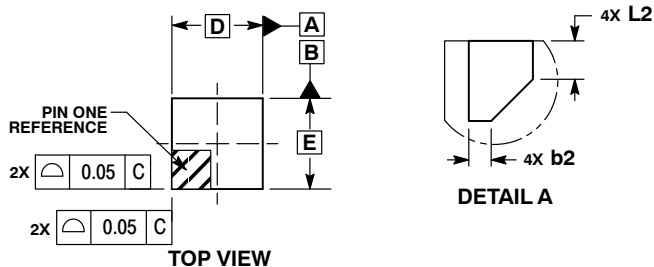
ON Semiconductor®



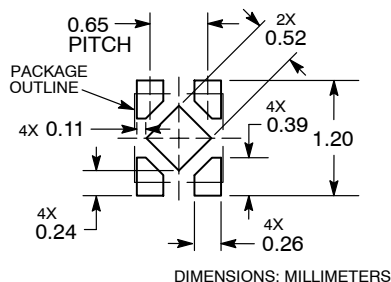
SCALE 4:1

**XDFN4 1.0x1.0, 0.65P**  
CASE 711AJ  
ISSUE A

DATE 13 NOV 2015



### RECOMMENDED MOUNTING FOOTPRINT\*

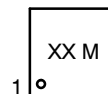


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.33	0.43
A1	0.00	0.05
A3	0.10	REF
b	0.15	0.25
b2	0.02	0.12
D	1.00	BSC
D2	0.43	0.53
E	1.00	BSC
e	0.65	BSC
L	0.20	0.30
L2	0.07	0.17

### GENERIC MARKING DIAGRAM\*



XX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON67179E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	XDFN4, 1.0X1.0, 0.65P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

#### North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

#### Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative