Quasi-Resonant Flyback Controller with HV section for Offline Power Supplies

NCP1344

The NCP1344 is a highly integrated quasi−resonant mode flyback controller capable of controlling rugged and high−performance off−line power supplies as required by adapter applications. This quasi−resonant current mode flyback controller implements the valley switching mode with low loss V_{CC} bias and auto−tune OCP for wide−range Vout applications, such as USB−PD. This system works down to the 32th valley and toggles to frequency variation mode. The controller includes the maximum switching frequency clamp which varies with the feedback pin voltage and synchronizes the turn−on event with the minimum of the drain voltage.

High−Voltage section featuring the High−Voltage startup and Brownout detection greatly simplifies the design of the auxiliary power supply. Adjustable over power protection ensures a flat output power level regardless of the operating input voltage. Slope compensation is ensured via the insertion of a resistor in series with the current sense pin.

Over temperature protection (OTP) is implemented at the current sense pin (SOIC−7) and requires the connection of a simple NTC resistance to the auxiliary winding. Over voltage protection (OVP) is done by sampling the auxiliary plateau but also the VCC pin.

The no−load standby power, low−load efficiency and acoustic noise can be optimized through the numerous configuration options for frozen peak current setpoint, count of pulses in skip mode, skip mode enter level, etc. The frequency variation ramp gradient can be set internally as well.

Features

- Integrated 750 V High−Voltage Startup Circuit with Brownout Detection
- Valley Switching in Discontinuous Conduction Mode for Improved Efficiency
- Valley Lockout Option
- 65 kHz / 100 kHz / 130 kHz / 200 kHz Frequency Clamp Options
- Low−loss V_{CC} Bias
- Auto−tune and Dual Level Over−current Protection
- Adjustable over Power Protection
- 64 ms Overload and 16 ms Peak Power Timers
- Variable Frequency Clamp Characteristic
- Proprietary Quiet Skip Cycle
- Auto−recovery / Latch Short Circuit Protection – Pre−short Compatible
- 5 ms Soft Start on both Peak Current and Frequency for Low Stress on Synchronous Rectifier
- Frequency Jitter for better EMI Signature
- Over Voltage Protection with Precise Auxiliary Voltage Sampling Event
- Over Temperature Protection on CS Pin
- This is a Pb−Free Device

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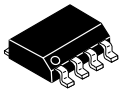
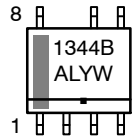


SOIC−7
CASE 751U

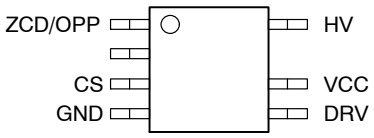
MARKING DIAGRAM



1344B	= Specific Device Code (See Specific Device Setup)
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTION



SOIC−7

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Typical Applications

- USB PD Adapters
- Ac−dc Adapters for Notebooks
- Auxiliary/Housekeeping Power Supplies

TYPICAL APPLICATION EXAMPLE

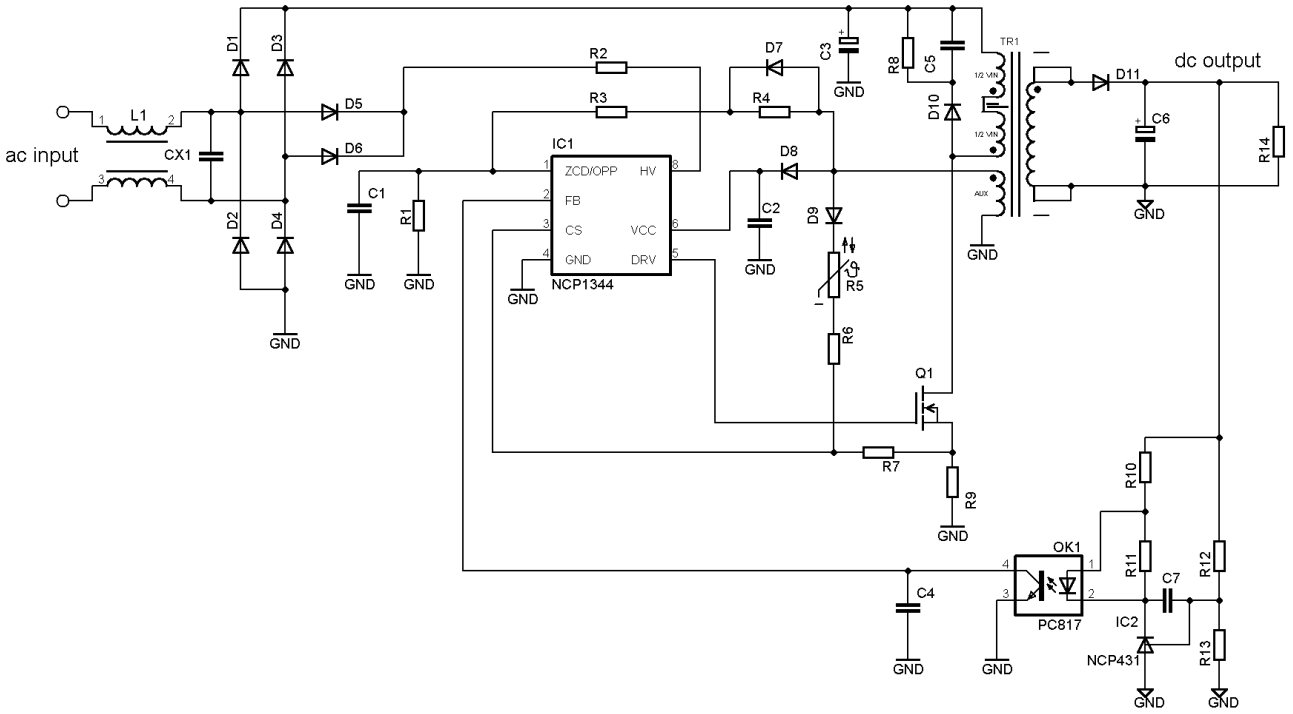


Figure 1. Flyback Converter Application using the NCP1344 in SOIC−7 Package

PIN FUNCTION DESCRIPTION

PIN FUNCTION DESCRIPTION

Pin N°	Pin Name	Function	Pin Description
1	ZCD/OPP/Fault	Detects core reset in QR operation. Latches off the part in OVP. Adjusts OPC level.	A resistive bridge from this pin to the auxiliary winding adjusts the OPC level and lets the controller observe the core magnetic state. A precise OVP level can be set.
2	FB	Feedback	An opto−coupler collector to ground controls the output regulation.
3	CS	Current Sense	This input senses the primary current for current−mode operation, and offers an overpower compensation adjustment. This pin implements over temperature protection as well.
4	GND	−	The controller ground
5	DRV	Drive output	Drives external MOSFET
6	VCC	V_{CC} input	This supply pin accepts up to 37 Vdc, with overvoltage detection. The pin is connected to an external auxiliary voltage.
8	HV	High−voltage pin	Connects to the rectified ac line to perform the functions of start−up current source, Self−Supply, brown−out detection and the HV sensing for the overpower protection purposes.

ORDERING INFORMATION

Ordering Part No.	BO level	Fault	Auto Tune OCP	OCP/OLM	Frequency	Package	Shipping
NCP1344BD1R2G	111−103V	Autorecovery	Enabled	OCP only	65 kHz	SOIC−7 (Pb−Free)	2500 / Tape & Reel

SPECIFIC DEVICE SETUP

SPECIFIC DEVICE SETUP

Firmware name		
NCP1344 Parameters	**Options**	**NCP1344 B**
OSCILLATOR		
Switching frequency clamp	65 kHz; 100 kHz; 130 kHz; 200 kHz	65 kHz
DCM jitter amplitude	10 mV; 20 mV; 30 mV; 40 mV	10 mV
Frequency jittering modulation frequency	1 kHz; 2 kHz; 3 kHz; 4 kHz; 5 kHz; disabled	4 kHz
$V_{CC(ON)}$ level	12 V; 16 V	12 V
SKIP MODE		
Quiet skip enable (timer)/min. pulses # forced	1250 us/enabled; no limit/enabled; no limit/ disabled	no limit/enabled
Minimum current setpoint	disabled; 150 mV; 175 mV; 200 mV; 225 mV; 250 mV; 275 mV; 300 mV	disabled
QR CONTROL ENGINE		
Valley switching during Soft−Start	enabled; disabled	enabled
USB−PD		
Auto tune OCP	enabled; disabled	enabled
Auto tune OCP latch	autorecovery; latched	autorecovery
PROTECTIONS ON/OFF		
OLM protection	enabled; disabled	disabled
Fault timer	enabled; disabled	enabled
AC BO protection	enabled; disabled	enabled
AC OVP protection	enabled; disabled	enabled
PROTECTIONS LEVELS		
Fault timer duration OLM/OCP	32/8 ms; 64/16 ms; 128/32 ms; 256/64 ms	64/16 ms
Fault timer duration multiplier	1; 16	1
VCC OVP level	35.7 V; 26.5 V	35.7 V
BO protection level	111/103 V; 111/0 V; 229/211 V; 95/87 V	111/103 V
BO timer	64 ms; 512 ms	64 ms
AC OVP protection level	430/425 V; 420/415 V	420/415 V
Autorecovery timer	1s; 2s	1s
PROTECTIONS BEHAVIOR		
OCP latched	autorecovery; latched	autorecovery
VCC OVP latched	autorecovery; latched	autorecovery
CS OTP latched	autorecovery; latched	autorecovery

SIMPLIFIED INTERNAL BLOCK SCHEMATIC

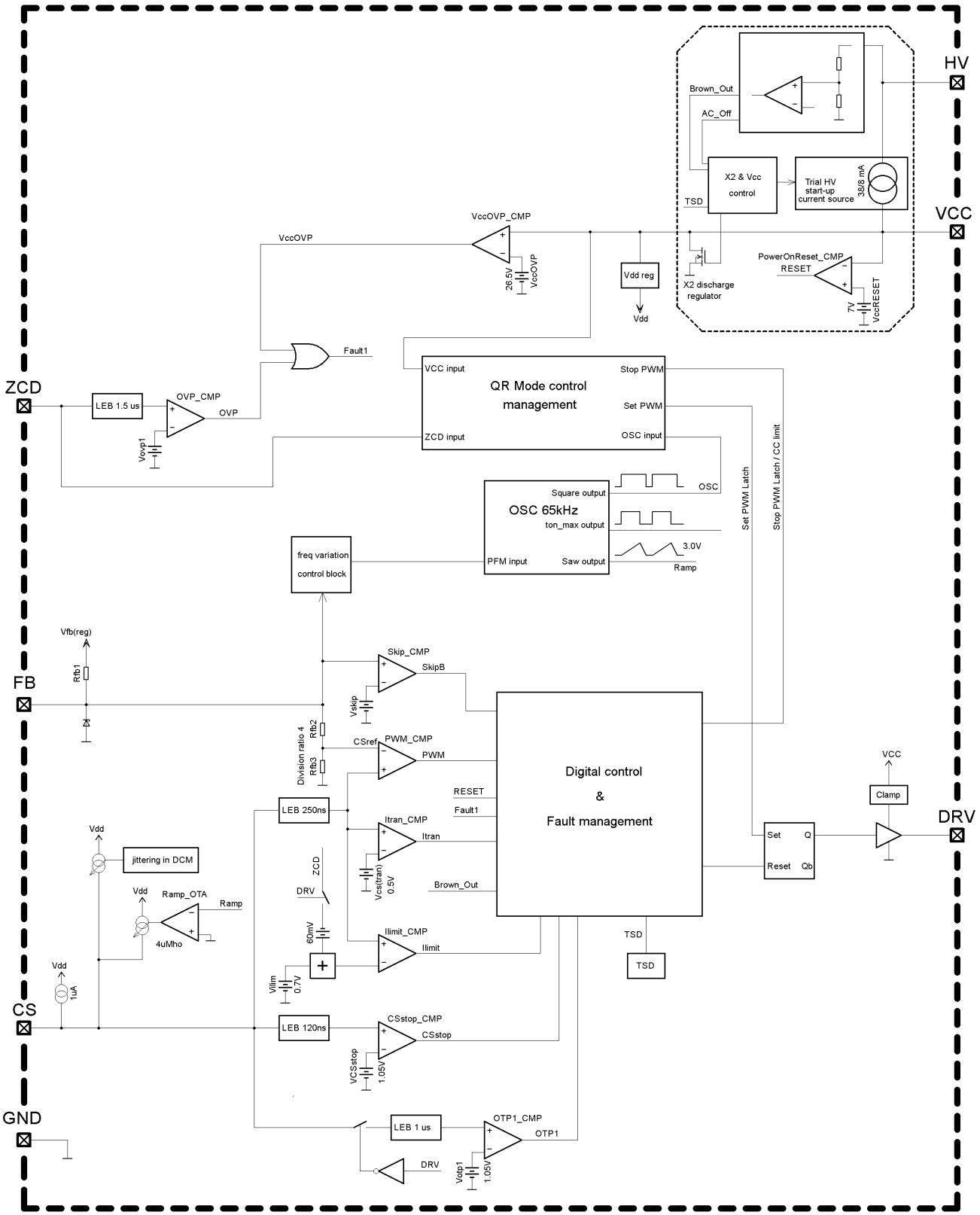


Figure 2. Simplified Internal Block Schematic

MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
DRV	Maximum voltage on DRV pin (Dc−Current self−limited if operated within the allowed range) (Note 2)	− 0.3 to 20 +/−1000 (peak)	V mA
V_{CC}	V_{CC} Power Supply voltage, V_{CC} pin, continuous voltage Power Supply voltage, V_{CC} pin, continuous voltage (Note 2)	− 0.3 to 37 +/− 30 (peak)	V mA
HV	Maximum voltage on HV pin (Dc−Current self−limited if operated within the allowed range)	− 0.3 to 750 +/− 20	V mA
V_{max}	Maximum voltage on low power pins (except pin DRV, pin VCC and pin HV) (Dc−Current self−limited if operated within the allowed range) (Note 2)	− 0.3 to 5.5 +/− 10 (peak)	V mA
$R_{\theta J-A}$	Thermal Resistance SOIC−7 Junction−to−Air, low conductivity PCB (Note 3) Junction−to−Air, medium conductivity PCB (Note 4) Junction−to−Air, high conductivity PCB (Note 5)	 162 147 115	°C/W
$R_{\theta J-C}$	Thermal Resistance Junction−to−Case	73	°C/W
T_{JMAX}	Operating Junction Temperature	−40 to +150	°C
$T_{STRGMAX}$	Storage Temperature Range	−60 to +150	°C
	ESD Capability, HBM model (All pins except HV) (Note 1)	> 4000	V
	ESD Capability, Charge Discharge Model (Note 1)	> 500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 4000 V per JEDEC standard JESD22, Method A114E
   Charge Discharge Model Method 500 V per JEDEC standard JESD22, Method C101E
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78
3. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51−1 conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 100 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51−2 conductivity test PCB. Test conditions were under natural convection or zero air flow.
5. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 650 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51−3 conductivity test PCB. Test conditions were under natural convection or zero air flow.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
HIGH VOLTAGE CURRENT SOURCE						
Minimum voltage for current source operation		$V_{HV(min)}$	–	30	40	V
Current flowing out of V_{CC} pin	V_{CC} = 0 V	I_{start1}	0.2	0.5	0.8	mA
	V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{start2}	5	8	11	
		I_{start3}	28	38	45	
Off−state leakage current	V_{HV} = 500 V, V_{CC} = 15 V	$I_{start(off)}$	–	3	9	μA
SUPPLY						
Turn−on threshold level, V_{CC} going up HV current source stop threshold		$V_{CC(on)}$	11.0	12.0	13.0	V
urn−on threshold level, V_{CC} going up HV current source stop threshold − optional		$V_{CC(on)}$	15.0	16.0	17.0	V
HV current source restart threshold		$V_{CC(min)}$	9.5	10.5	11.5	V
Turn−off threshold		$V_{CC(off)}$	8.3	8.9	9.4	V
Overvoltage threshold		$V_{CC(ovp)}$	34	35.5	37	V
Overvoltage threshold − optional		$V_{CC(ovp)}$	25	26.5	28	V
Blanking duration on $V_{CC(off)}$ and $V_{CC(ovp)}$ detection		$t_{VCC(blank)}$	–	10	–	μs
V_{CC} decreasing level at which the internal logic resets		$V_{CC(reset)}$	4.8	7.0	7.7	V
V_{CC} level for I_{START1} to I_{START2} transition		$V_{CC(inhibit)}$	1.0	2.1	3.0	V
Internal current consumption	DRV open, V_{FB} = 3 V, 65 kHz	I_{cc1}	0.9	1.3	1.5	mA
	Cdrv = 1 nF, V_{FB} = 3 V, 65 kHz	I_{cc2}	1.6	2.1	2.6	mA
	Skip or before start−up	I_{CC3}	250	500	600	μA
	Fault mode (fault or latch)	I_{CC4}	200	475	550	μA
BROWN−OUT						
Brown−Out thresholds − optional	V_{HV} going up	$V_{HV(start)}$	210	229	248	V
	V_{HV} going down	$V_{HV(stop)}$	194	211	228	
Brown−Out thresholds	V_{HV} going up	$V_{HV(start)}$	102	111	120	V
	V_{HV} going down	$V_{HV(stop)}$	94	103	112	
Brown−Out thresholds − optional	V_{HV} going up	$V_{HV(start)}$	87	95	103	V
	V_{HV} going down	$V_{HV(stop)}$	79	87	95	
Brown−In threshold − optional (NO Brown out)	V_{HV} going up	$V_{HV(start)}$	90	100	110	V
Timer duration for line cycle drop−out		t_{HV}	42	64	86	ms
Overvoltage threshold	V_{HV} going up	$V_{HV(OV1)}$	400	430	460	V
	V_{HV} going down	$V_{HV(OV2)}$	395	425	455	
Overvoltage threshold − optional	V_{HV} going up	$V_{HV(OV1)}$	390	420	450	V
	V_{HV} going down	$V_{HV(OV2)}$	385	415	445	
Blanking duration on line overvoltage detection		$t_{OV(blank)}$	–	250	–	μs

ELECTRICAL CHARACTERISTICS (continued) (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
SWITCHING FREQUENCY CLAMP						
Maximum switching frequency clamp		f_{OSC}	61 94	64 100	69 106	kHz
Maximum duty−ratio (corresponding to maximum on time at maximum switching frequency)		D_{MAX}	75	80	85	%
Frequency jittering amplitude for DCM		$V_{jitterDCM}$	–	20	–	mV
Frequency jittering modulation frequency for DCM			0.85	1.00	1.25	kHz
SWITCHING FREQUENCY CLAMP VARIATION CHARACTERISTIC						
Feedback voltage threshold below which frequency variation increases slope		V_{foldS}	2.1	2.2	2.5	V
Feedback voltage threshold below which frequency variation decreases slope		V_{foldE}	1.6	1.7	2.0	V
Typical low switching frequency	$V_{FB} = V_{skip(in)} + 0.1$ V, for 65 kHz version	$f_{osc(low)}$	23	27	33	kHz
Typical low switching frequency	$V_{FB} = V_{skip(in)} + 0.1$ V, for 200 kHz version	$f_{osc(low)}$	18	29	40	kHz
Internal frequency setup reference current		I_{fold}	13	15	17	μA
Frequency variation offset with a 0 Ω resistor from SFF to ground		$V_{fold(off)}$	–	−600	–	mV
Frequency variation offset with a 100 kΩ resistor from SFF to ground		$V_{fold(off)}$	–	0	–	mV
Frequency variation offset with a 200 kΩ resistor from SFF to ground		$V_{fold(off)}$	–	600	–	mV
Frequency variation offset depending on V_{CC}	V_{CC} = 9 V	$V_{fold(sup1)}$	–	−500	–	mV
Frequency variation offset depending on V_{CC}	V_{CC} = 22 V	$V_{fold(sup2)}$	–	0	–	mV
Frequency variation offset depending on V_{CC}	V_{CC} = 35 V	$V_{fold(sup3)}$	–	500	–	mV
OUTPUT DRIVER						
Rise time, 10 to 90 % of VCC	$V_{CC} = V_{CC(off)} + 0.2$ V, C_{DRV} = 1 nF	t_{rise}	–	40	70	ns
Fall time, 90 to 10 % of VCC	$V_{CC} = V_{CC(off)} + 0.2$ V, C_{DRV} = 1 nF	t_{fall}	–	30	60	ns
Current capability	$V_{CC} = V_{CC(off)} + 0.2$ V, C_{DRV} = 1 nF DRV high, V_{DRV} = 0 V DRV low, $V_{DRV} = V_{CC}$	 $I_{DRV(source)}$ $I_{DRV(sink)}$	–	 300 500	 – –	mA
Clamping voltage (maximum gate voltage)	$V_{CC} = V_{CC(ovp)} - 0.1$ V, DRV high, R_{DRV} = 33 kW, C_{load} = 220 pF	$V_{DRV(clamp)}$	10	12	14	V
High−state voltage drop	$V_{CC} = V_{CC(min)} + 0.1$ V, R_{DRV} = 33 kW, DRV high	$V_{DRV(drop)}$	–	–	1	V
CURRENT SENSE						
Input Pull−up Current	V_{CS} = 0.7 V	I_{bias}	–	1	–	μA
Maximum internal current setpoint	V_{FB} > 3.5 V	V_{ILIM}	0.66	0.70	0.74	V
Propagation delay from V_{Ilimit} detection to DRV off	$V_{CS} = V_{ILIM}$	t_{delay}	–	50	100	ns
Leading Edge Blanking Duration for V_{ILIM}		t_{LEB}	180	270	370	ns
Threshold for immediate fault protection activation		$V_{CS(stop)}$	0.95	1.5	1.15	V
Leading Edge Blanking Duration for VCS(stop) (Note 6)		t_{BCS}	50	80	150	ns

ELECTRICAL CHARACTERISTICS (continued) (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Soft−start duration	From 1st pulse to V_{CS} = V_{ILIM}	t_{SSTART}	4.2	5.0	5.8	ms
Over temperature protection threshold when DRV is low	V_{CS} going up	$V_{OTP(CS)}$	0.95	1.00	1.05	V
Blanking duration on OTP detection		$t_{OTP,CS}$	0.7	1.0	1.3	μs
Delay time constant before OTP confirmation		$t_{OTP,del}$	–	600	–	ns
Maximum Setpoint decrease for ZCD pin biased to −290 mV (Note 7)	V_{DMG} = −290 mV	CS_{DROP}	–	32.8	–	%
Voltage setpoint for ZCD pin biased to −250 Mv (Note 7), Tj 25 °C		$V_{CS(OPP)}$	0.46	0.51	0.56	V
Voltage setpoint for ZCD pin biased to −250 mV (Note 7), Tj from −40° to 125 °C		$V_{CS(OPPET)}$	–	0.51	–	V
Blanking delay before considering VDMG for OPP		t_{OPP}	–	600	–	ns
CS pin voltage bias for 0% OPP	V_{DMG} = −60 mV	V_{OPP0}	–	−60	–	mV
INTERNAL SLOPE COMPENSATION						
Slope of the compensation ramp		$S_{comp(65kHz)}$	–	10	–	μA / μs
FEEDBACK						
Equivalent resistance for the optocoupler	T_J = 25°C	$R_{FB(eq)}$	20	30	40	kΩ
V_{FB} to internal current setpoint division ratio (Note 8)		K_{FB}	–	5.4	–	–
Internal pull−up voltage on the FB pin		$V_{FB(open)}$	3.7	4	4.2	V
SKIP CYCLE MODE						
Feedback voltage thresholds for skip mode	V_{FB} going down	$V_{skip(in)}$	0.30	0.40	0.50	V
	V_{FB} going up	$V_{skip(out)}$	0.40	0.50	0.60	
Minimum number of pulses in burst		$n_{P,skip}$	3	–	–	–
Skip out delay (Note 8)		t_{skip}	–	–	38	μs
Quiet−Skip Timer		t_{quiet}	1000	1250	1500	μs
Quiet−Skip escape level (transient enhancer)		$V_{skip(tran)}$	1.7	1.8	1.9	V
DEMAGNETIZATION SENSE						
V_{ZCD} threshold voltage	V_{ZCD} decreasing	$V_{ZCD(TH)}$	25	45	65	mV
V_{ZCD} hysteresis	V_{ZCD} increasing	$V_{ZCD(HYS)}$	–	35	–	mV
Threshold voltage for output short circuit or aux. winding short circuit detection (enter)	After t_{BLANK} if V_{ZCD} < $V_{ZCD(short)}$	$V_{ZCD(short1)}$	–	0.4	–	V
Threshold voltage for output short circuit or aux. winding short circuit detection (exit)	After t_{BLANK} if V_{ZCD} < $V_{ZCD(short)}$	$V_{ZCD(short2)}$	–	0.5	–	V
Propagation Delay from valley detection to DRV high	V_{ZCD} decreasing from 3 V to 0 V	t_{DEM}	–	–	150	ns
Blanking delay after on−time		t_{blank}	1.2	1.5	1.8	μs
Timeout after last demagnetization transition (leakage ringing blanking)	Valley detection timeout	t_{vlyout}	4.5	5.5	6.5	μs
Input leakage current	V_{CC} > $V_{CC(on)}$ V_{ZCD} = 3 V, DRV is low	I_{ZCD}	–	–	0.1	μA
High threshold at ZCD pin V_{OVP1}	V_{ZCD} going up	V_{OVP1}	2.85	3.15	3.35	V
Number of OVP1 event pulses to latch acknowledgment	V_{ZCD} > V_{OVP1}	n_{OVP1}	–	8	–	–
Number of drive pulses before fault acknowledgment when in output short circuit	(V_{ZCD} < $V_{ZCD(short1)}$) & (V_{CS} > V_{ILIM})	n_{OS}	–	8	–	–

ELECTRICAL CHARACTERISTICS (continued) (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
OVERLOAD PROTECTIONS						
Fault timer duration		t_{fault}	14	16	18	ms
Fault timer reset time	V_{CS} < 0.7 V,	$t_{fault,res}$	150	200	250	μs
	D < 90% D_{MAX}					
Autorecovery mode latch−off time duration		$t_{autorec}$	0.85	1.00	1.35	s
CS threshold for overload timer activation − optional		$V_{CS(tran)}$	0.47	0.50	0.53	V
Transient peak power timer duration − optional	$V_{CS(peak)}$ = $V_{CS(tran)}$ + 0.1 V from 1st time V_{CS} > $V_{CS(tran)}$ to DRV stop	t_{tran}	54	64	74	ms
OTP INPUT						
OTP voltage threshold	V_{Latch} going down, T_J = 25°C	V_{OTP}	0.38	0.40	0.42	V
OTP resistance threshold(T_J = 25°C)	External resistance is going down	R_{OTP}	7.6	8.0	8.4	kΩ
OTP resistance threshold (T_J = 80°C)	External NTC resistance is going down	R_{OTP}	−	8.5	−	kΩ
OTP resistance threshold (T_J = 110°C)	External NTC resistance is going down	R_{OTP}	−	9.5	−	kΩ
Current source for direct NTC connection During normal operation During soft−start	V_{Latch} = 0.2 V	I_{NTC} $I_{NTC(SSTART)}$	30 60	50 100	70 140	μA
Current source for direct NTC connection During normal operation	V_{Latch} = 0.2 V, T_J = 25°C	I_{NTC}	47.5	50.0	52.5	μA
Blanking duration on low latch detection		$t_{Latch(OTP)}$	−	350	−	μs
Clamping voltage	I_{Latch} = 0 mA	$V_{clamp0(Latch)}$	1.1	1.3	1.5	V
	I_{Latch} = 1 mA	$V_{clamp1(Latch)}$	1.8	2.4	3.0	
VALLEY LOCKOUT						
Low frequency period for valley lockout refresh		f_{LFC}	−	100	−	μs
The maximum valleys count for lockout		n_{valley}	−	32	−	−
AUTO−TUNE CURRENT LIMIT						
CS pin averaging filter time constant		T_{AVG}	−	100	−	μs
Internal maximum current reference		I_{OCP}	550	700	850	nA
TEMPERATURE SHUTDOWN						
Temperature shutdown	T_J going up	T_{TSD}	−	150	−	ºC
Temperature shutdown hysteresis	T_J going down	$T_{TSD(HYS)}$	−	40	−	ºC

TYPICAL CHARACTERISTICS

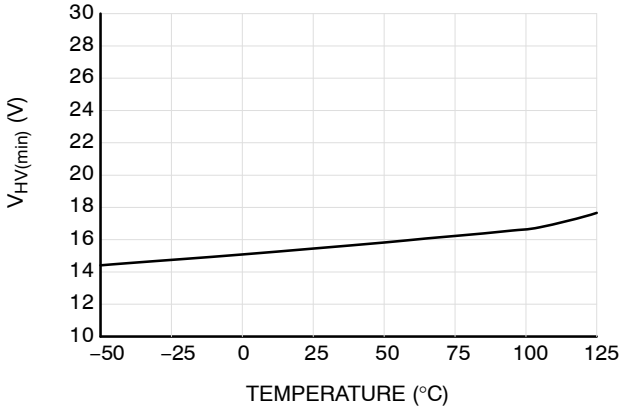


Figure 3. Minimum Voltage for HV Current Source Operation $V_{HV(min)}$

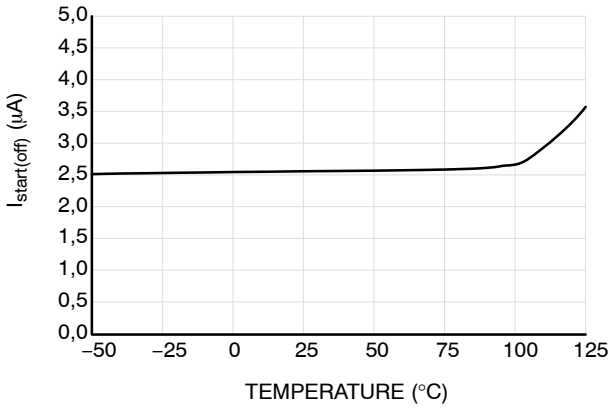


Figure 4. Off−state Leakage Current from HV Pin $I_{start(off)}$

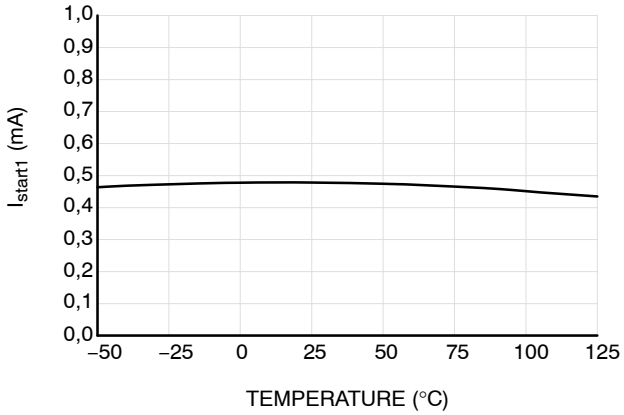


Figure 5. High Voltage Startup Current Flowing out of V_{CC} Pn I_{start1} in Case of V_{CC} Pin Fault/Short

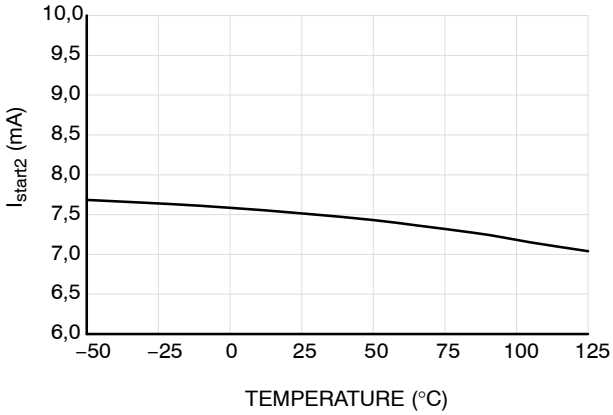


Figure 6. High Voltage Startup Current Flowing Out of V_{CC} Pin I_{start2}

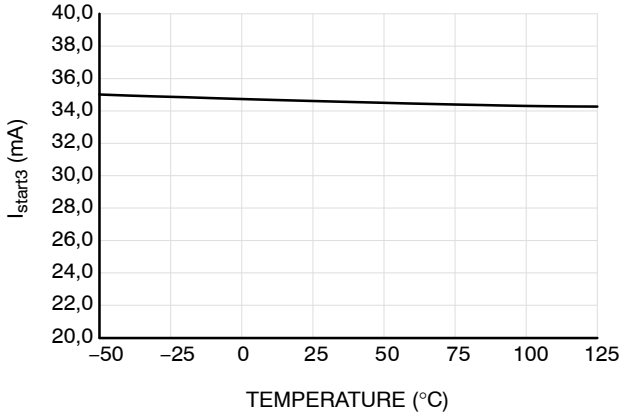


Figure 7. High Voltage Startup Current Flowing Out of V_{CC} Pin I_{start3}

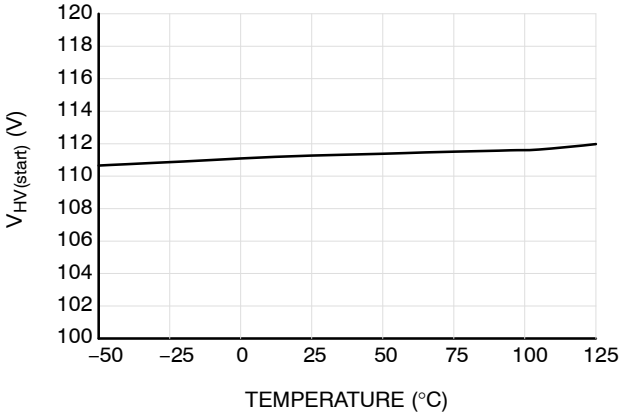


Figure 8. HV Pin Device Startup Threshold $V_{HV(start)}$

TYPICAL CHARACTERISTICS

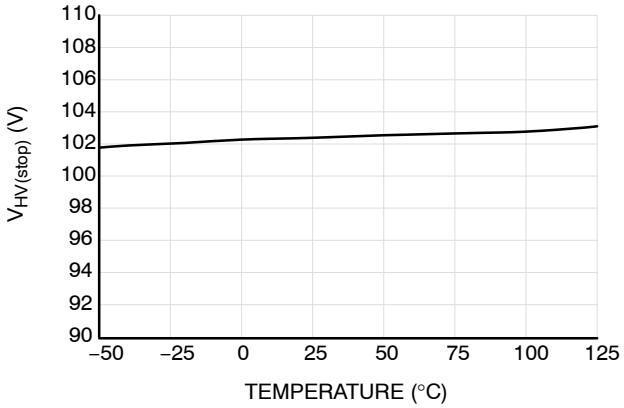


Figure 9. HV Pin Device Stop Threshold $V_{HV(stop)}$

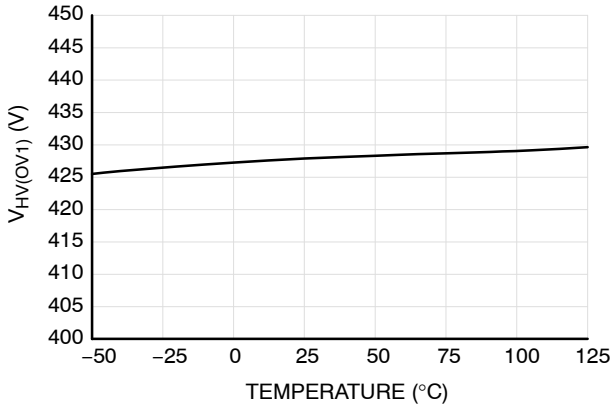


Figure 10. Overvoltage Protection Triggering Threshold on HV Pin $V_{HV(OV1)}$

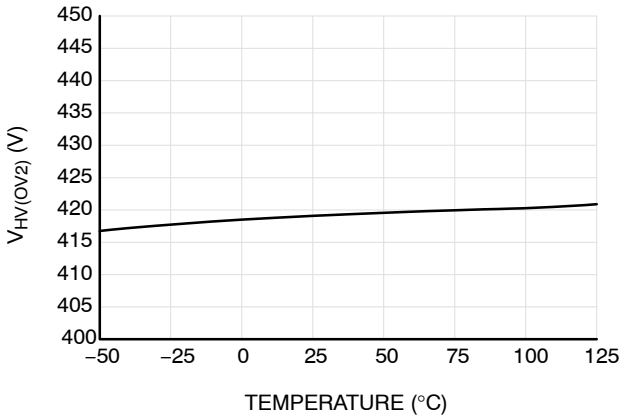


Figure 11. Overvoltage Protection Release Threshold on HV pin $V_{HV(OV2)}$

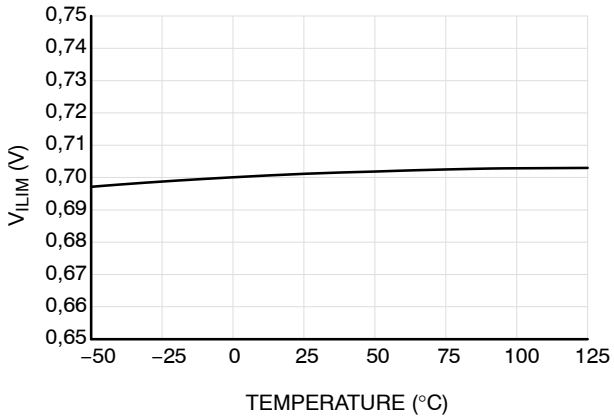


Figure 12. Maximum Internal Current Setpoint V_{ILIM}

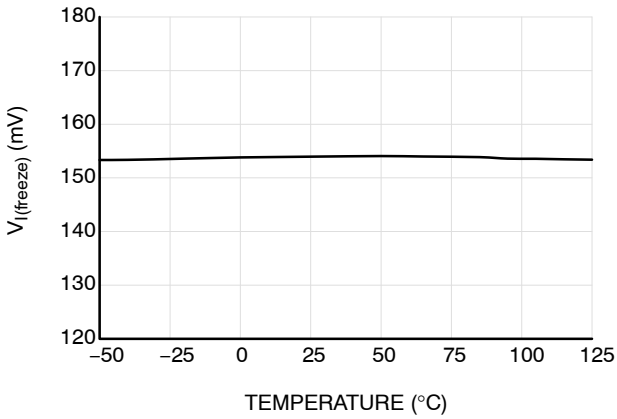


Figure 13. Frozen Current Setpoint $V_{I(freeze)}$ for the Light Load Operation

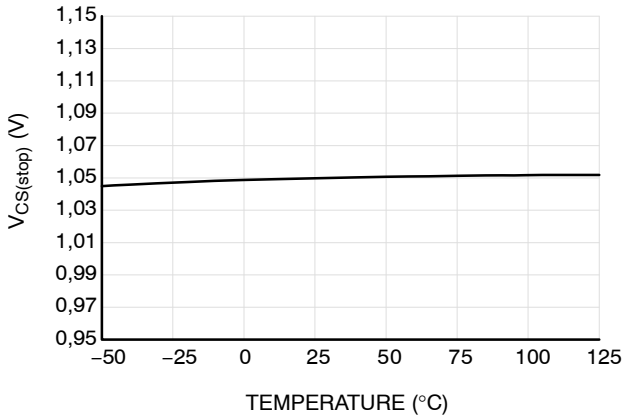


Figure 14. Threshold for the very Fast Fault Protection Activation $V_{CS(stop)}$

TYPICAL CHARACTERISTICS

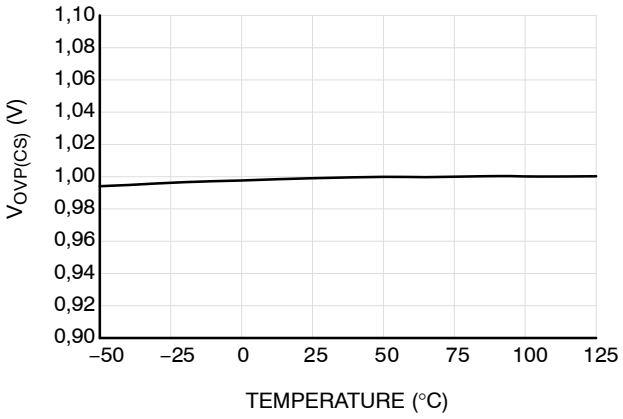


Figure 15. Overvoltage Protection Threshold at CS Pin $V_{OVP(CS)}$

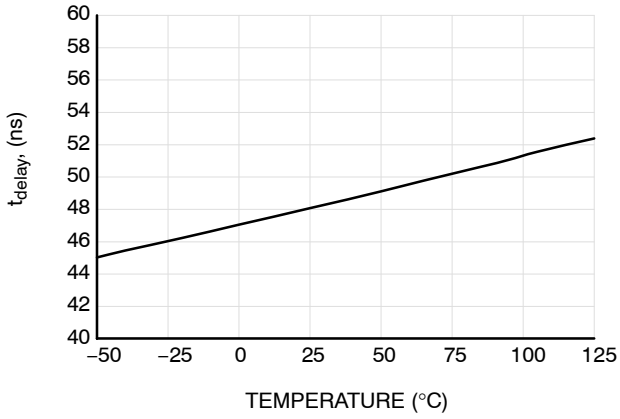


Figure 16. Propagation Delay t_{delay}

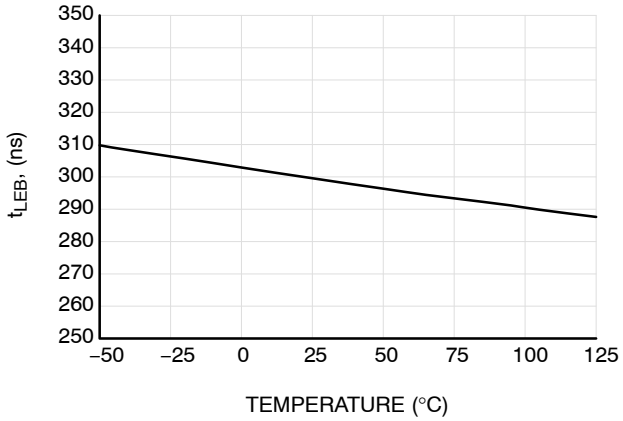


Figure 17. Leading Edge Blanking Duration t_{LEB}

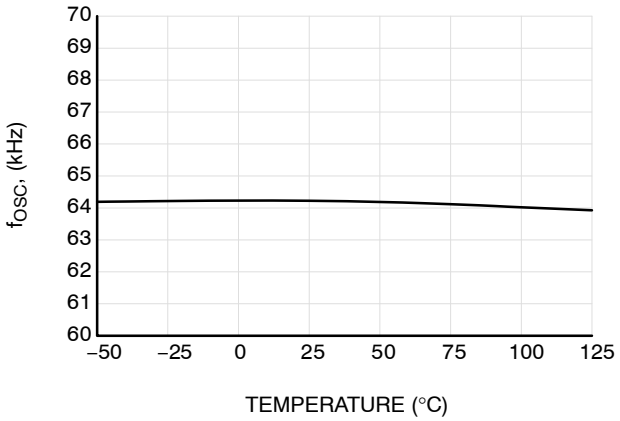


Figure 18. Maximum Switching Frequency Clamp f_{OSC}

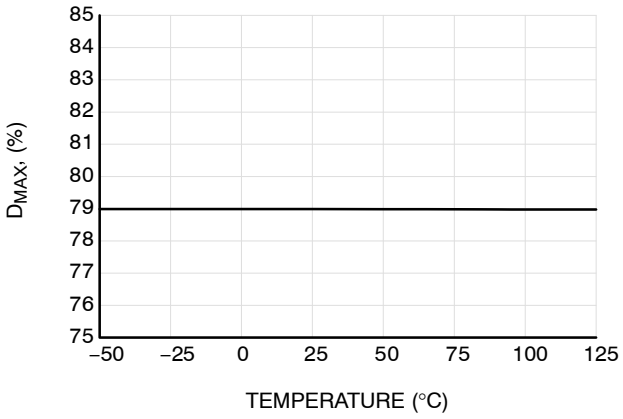


Figure 19. Maximum Duty Cycle D_{MAX}

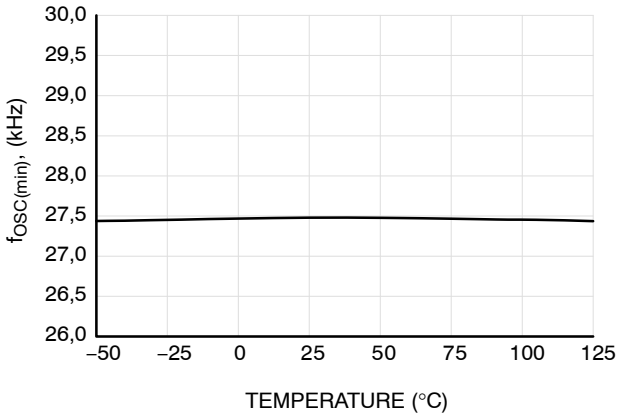


Figure 20. Typical Low Switching Frequency $f_{OSC(low)}$

TYPICAL CHARACTERISTICS

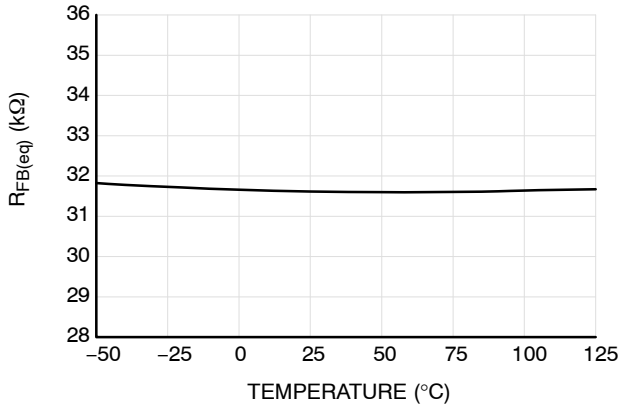


Figure 21. Equivalent Resistance for the Optocoupler $R_{FB(eq)}$

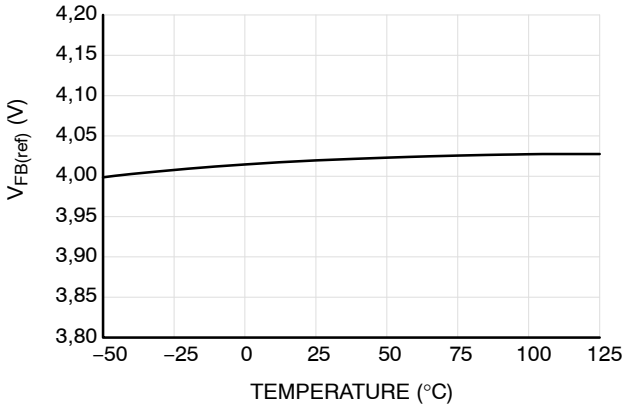


Figure 22. FB Pin Open Voltage $V_{FB(ref)}$

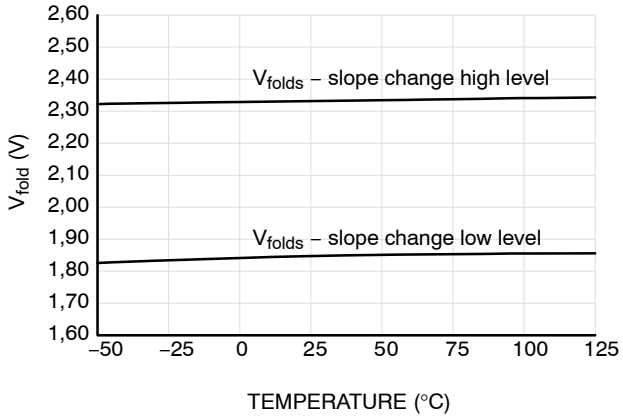


Figure 23. FB Pin Voltage Thresholds for Slope Change of the Frequency Variation V_{foldS}, V_{foldE}

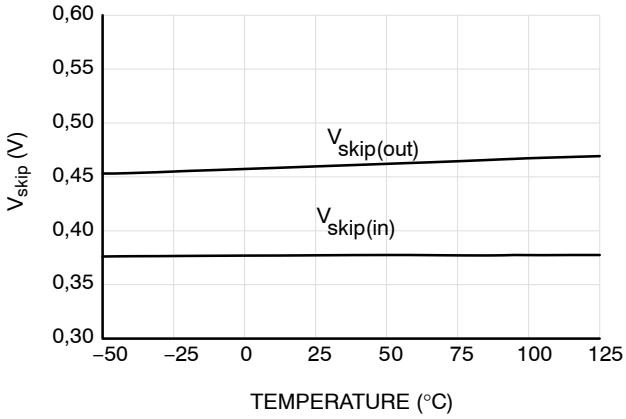


Figure 24. FB pin Skip−In and Skip−Out Levels $V_{skip(in)}$ and $V_{skip(out)}$

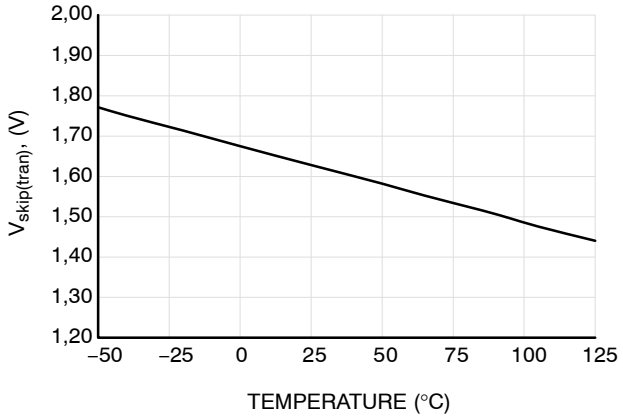


Figure 25. FB Level for Immediate Leaving of the Quiet Skip Mode $V_{skip(tran)}$

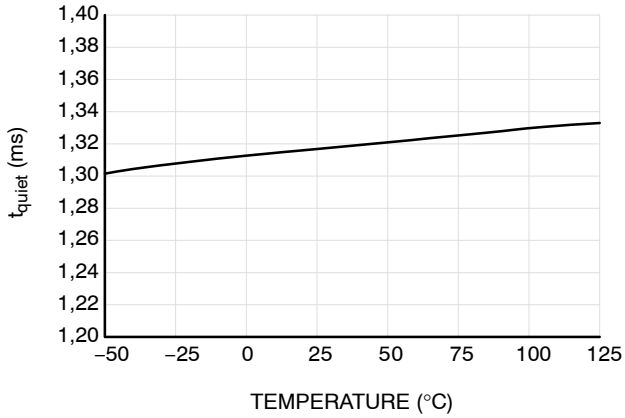


Figure 26. Quiet Skip Timer Duration t_{quiet}

TYPICAL CHARACTERISTICS

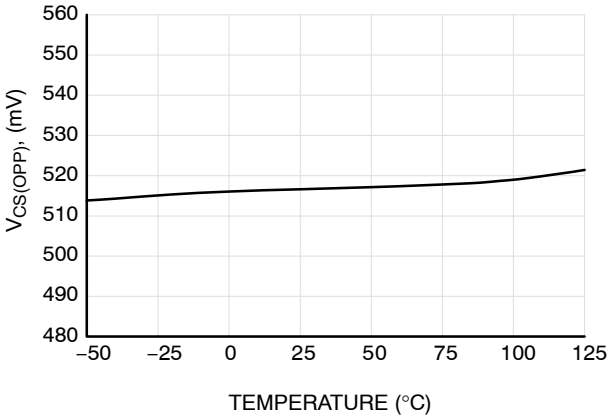


Figure 27. CS Pin Current Setpoint for ZCD Pin Biased to −250 mV $V_{CS(OPP)}$

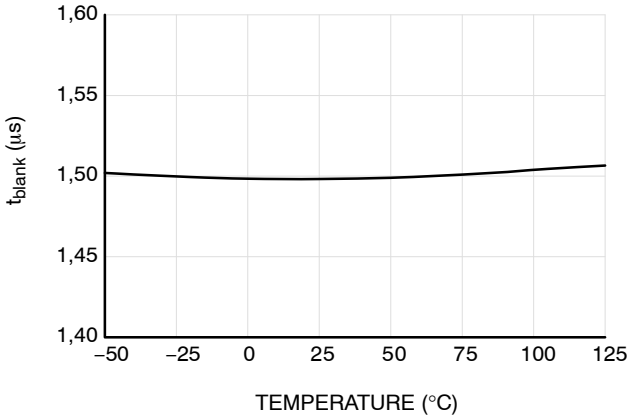


Figure 28. Blanking Time to ZCD OVP Detection after DRV off Event t_{blank}

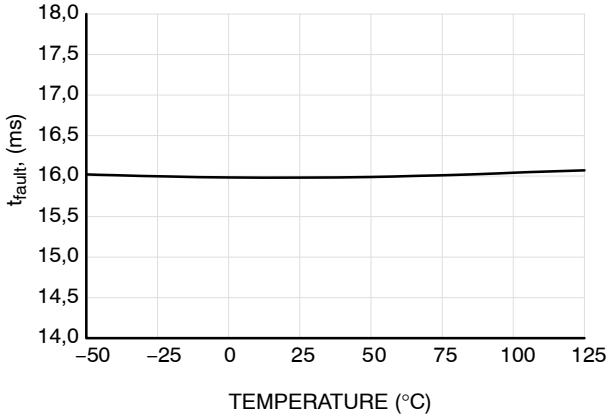


Figure 29. The Fault Timer Duration t_{fault}

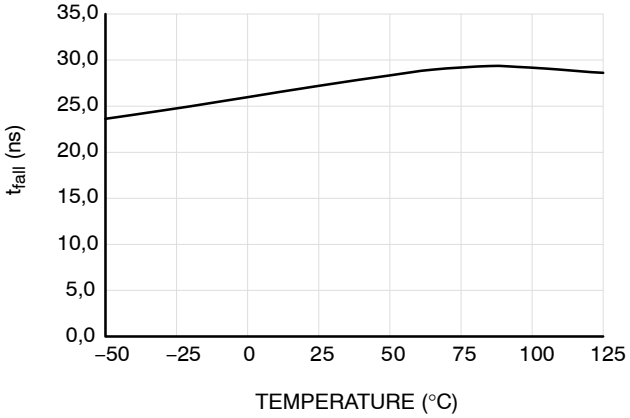


Figure 30. Output Driver Fall Time t_{fall}

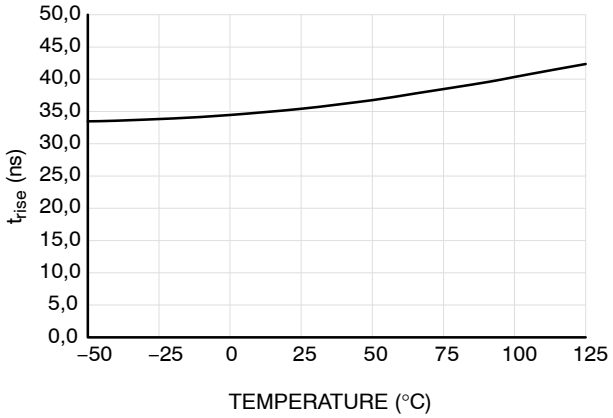


Figure 31. Output Driver Rise Time t_{rise}

TYPICAL CHARACTERISTICS

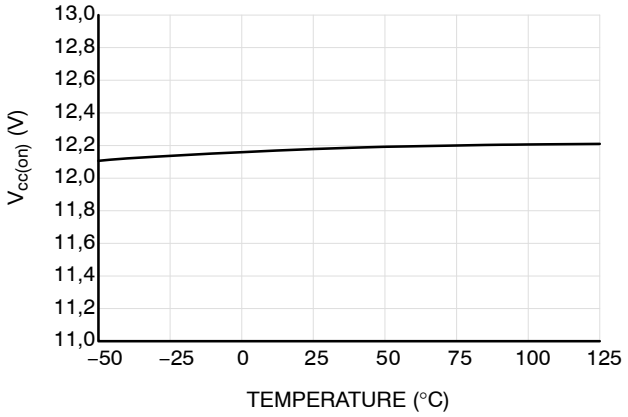


Figure 32. V_{CC} Turn−on Threshold Level, V_{CC} going up HV Current Source Stop Threshold $V_{CC(on)}$

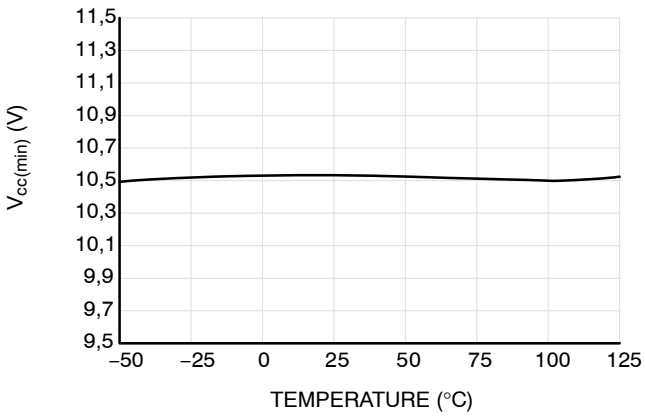


Figure 33. HV Current Cource Restart Threshold $V_{CC(min)}$

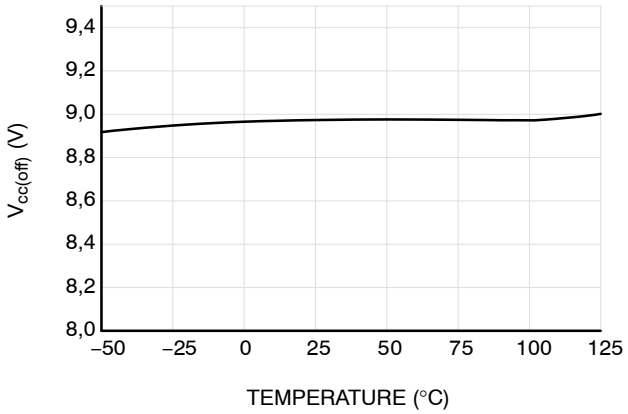


Figure 34. V_{CC} Turn−off Threshold (UVLO) $V_{CC(off)}$

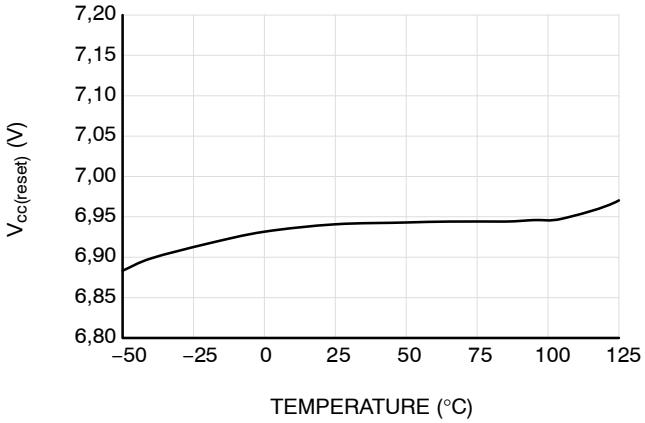


Figure 35. V_{CC} Decreasing Level at which the Internal Logic Resets $V_{CC(reset)}$

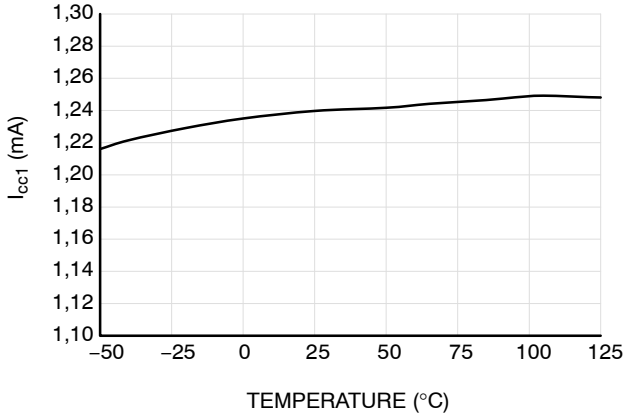


Figure 36. Internal Current Consumption when DRV Pin is Unloaded I_{CC1}

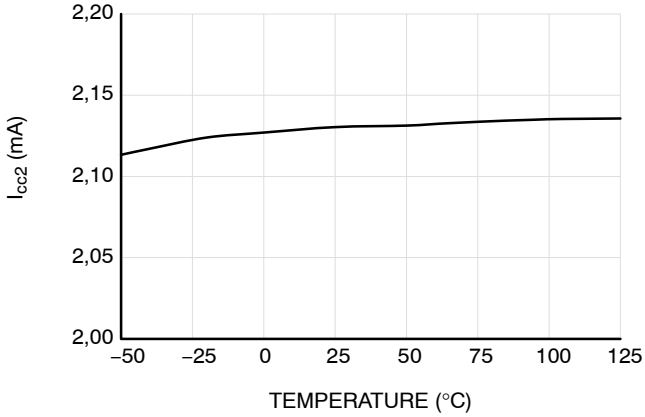


Figure 37. Internal Current Consumption when DRV Pin is Loaded by 1 nF Capacitance I_{CC2}

TYPICAL CHARACTERISTICS

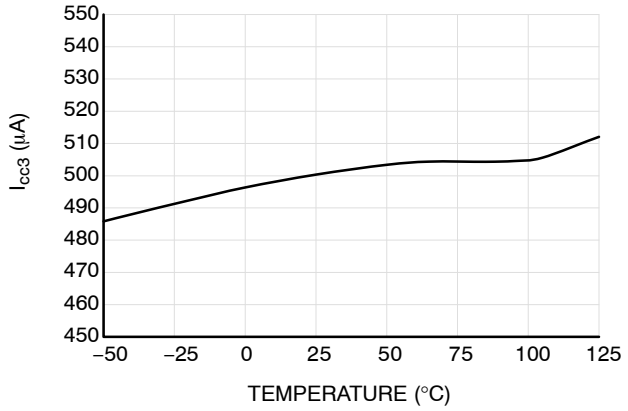


Figure 38. Internal Current Consumption in Skip Mode I_{CC3}

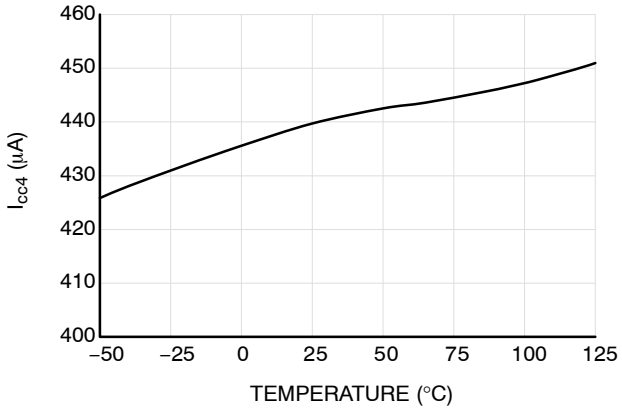


Figure 39. Internal Current Consumption in Fault I_{CC4}

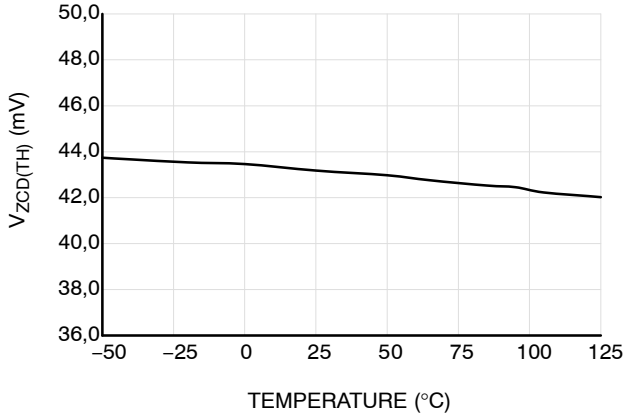


Figure 40. Zero Current Detection Threshold Voltage $V_{ZCD(th)}$

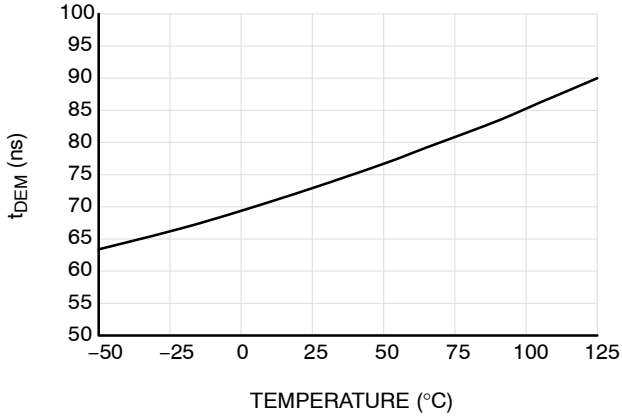


Figure 41. Propagation Delay from Valley Detection to DRV High t_{DEM}

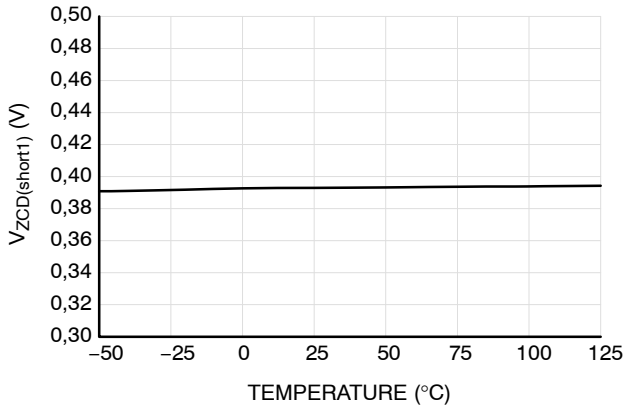


Figure 42. Threshold Voltage on ZCD Pin for Output/Aux Short Circuit Detection $V_{ZCD(short1)}$

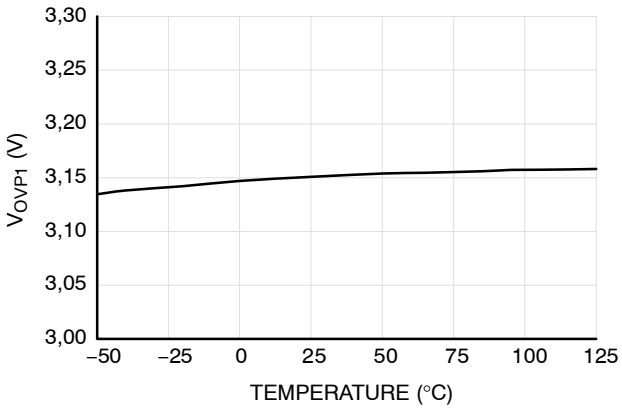


Figure 43. Over Voltage Protection Threshold at ZCD Pin V_{OVP1}

TYPICAL CHARACTERISTICS

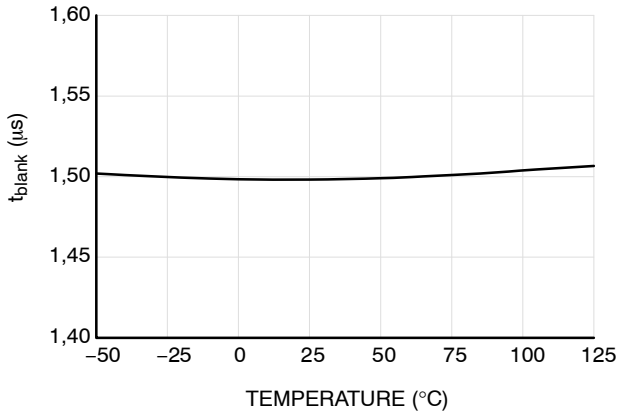


Figure 44. Blanking delay after on−time at ZCD pin t_{blank}

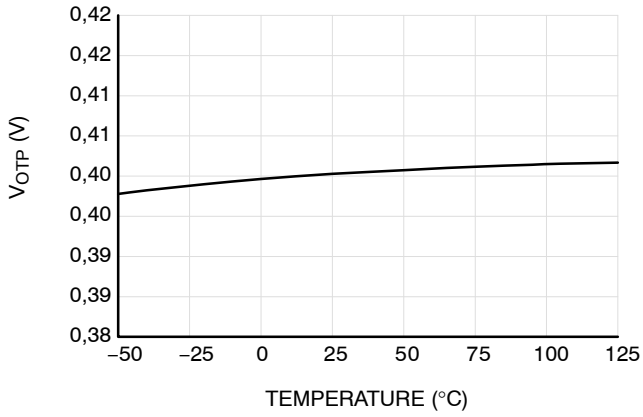


Figure 45. OTP pin low threshold for over−temperature protection V_{OTP}

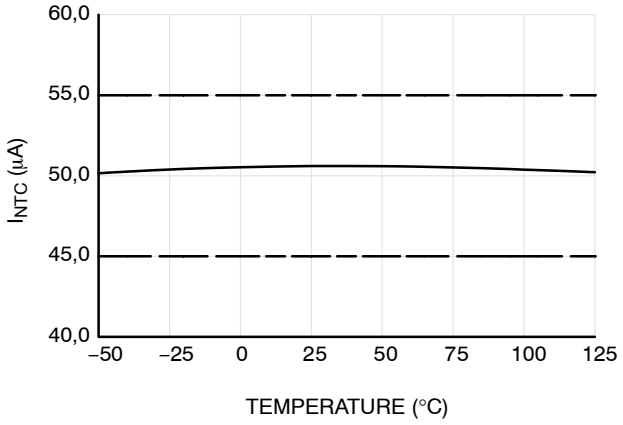


Figure 46. Current INTC Sourced Out of the OTP Pin, allowing the Direct NTC Connection

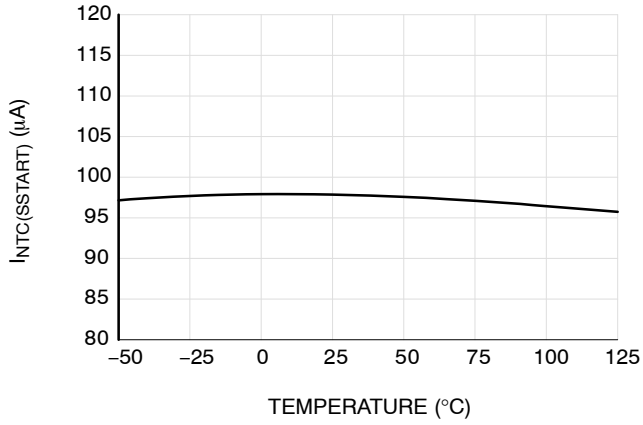


Figure 47. Current $I_{NTC(SSTART)}$ Sourced Out of the OTP Pin during Soft−start Period

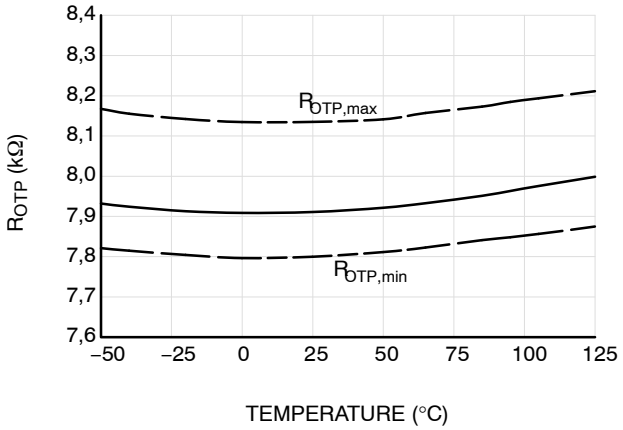


Figure 48. The OTP Resistance Threshold R_{OTP}

NOTE: The OTP resistance maximum and minimum limits are not the guaranteed limits, but the maximum and minimum measured data values from the device characterization.

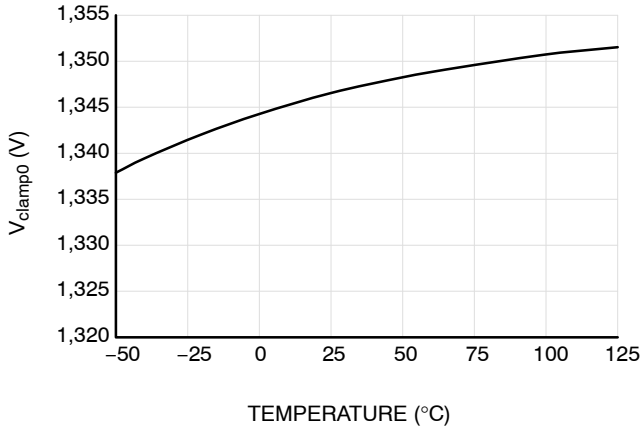


Figure 49. Clamped Voltage at OTP Pin, when this Pin is Left Unloaded V_{clamp0}

APPLICATION INFORMATION

Functional Description

The NCP1344 implements a quasi−resonant current−mode architecture where the switch−off event is dictated by the peak current set−point. This component represents the ideal candidate where low part−count and cost effectiveness are the key parameters, particularly in low−cost ac−dc adapters, open−frame power supplies etc. The NCP1344 brings all the necessary components normally needed in today's modern power supply designs, bringing several enhancements such as a non−dissipative OPP, brownout protection and a sophisticated frequency reduction management for an optimized efficiency over the power range. The frequency is limited at high−power conditions, but reduces as the load is getting lighter. When variable frequency mode is activated, the part jumps in several valleys and remains locked in this state. The peak current is free to move at all times.

Heavy Load Mode

The peak current voltage setpoint is clamped to 0.7 V. The situation with this maximum current voltage setpoint cannot last more than fault timer duration. However, when a short circuit is detected in the output, the controller places the converter in a dangerous situation if it keeps pulsing while V_{out} is almost 0 V (heavy CCM could occur in the primary side with a *RCD* clamp voltage runaway). To avoid this stressful situation, the circuit senses a voltage on the demagnetization pin lower than 0.4 V during the off time duration after the 1.5 μs blanking time. If during t_{off} there is a condition where the demagnetization pin voltage is less than 0.4 V the controller immediately toggles to 65 kHz and lets the fault timer count. If during this mode and before the timer ends, the short circuit disappears and the demagnetization voltage goes above 0.5 V, the 65 kHz lock is reset and f_{sw} is free again to follow V_{FB}.

Quasi−resonant Mode

The NCP1344 controller extends the off−time to exactly match the next available valley in the quasi−resonant mode. The peak current is free to move while locked in the valley. Inside the controller, there is a low−frequency refresh clock (LFC) which initiates valley acquisition. This low−frequency refresh clock is 100 μs with several option to optimize between the acoustic noise level and stability of the system. When the next low−frequency clock occurs, a new valley acquisition is run to determine what valley number matches the upcoming 65 kHz or VCO pulse. It is like a camera shot where you freeze the converter operating point for the next 100 μs. Assume 1st valley was selected, then if the new acquisition confirms valley 3 is the right one, then the part locks in valley 3 and remains there until the next LFC acquisition occurs. That way, jumping between valleys can only occur 10 kHz frequency.

Start−up of the Controller

At start−up, the current source turns on when the voltage on the HV pin is higher than $V_{HV(min)}$, and turns off when V_{CC} reaches $V_{CC(on)}$, then turns on again when V_{CC} reaches $V_{CC(min)}$, until the input voltage is high enough to ensure a proper start−up, i.e. when V_{HV} reaches $V_{HV(start)}$. The controller actually starts the next time V_{CC} reaches $V_{CC(on)}$. The controller then delivers pulses, starting with a soft−start period t_{SSTART} during which the peak current linearly increases before the current−mode control takes over.

Even though the Dynamic Self−Supply is able to maintain the V_{CC} voltage between $V_{CC(on)}$ and $V_{CC(min)}$ by turning the HV start−up current source on and off, it can only be used in light load condition, otherwise the power dissipation on the die would be too much. As a result, an auxiliary voltage source is needed to supply V_{CC} during normal operation.

The Dynamic Self−Supply is useful to keep the controller alive when no switching pulses are delivered, e.g. in brown−out condition, or to prevent the controller from stopping during load transients when the V_{CC} might drop. The NCP1344 accepts a supply voltage as high as 37 V, with an overvoltage threshold $V_{CC(ovp)}$ that latches the controller off.

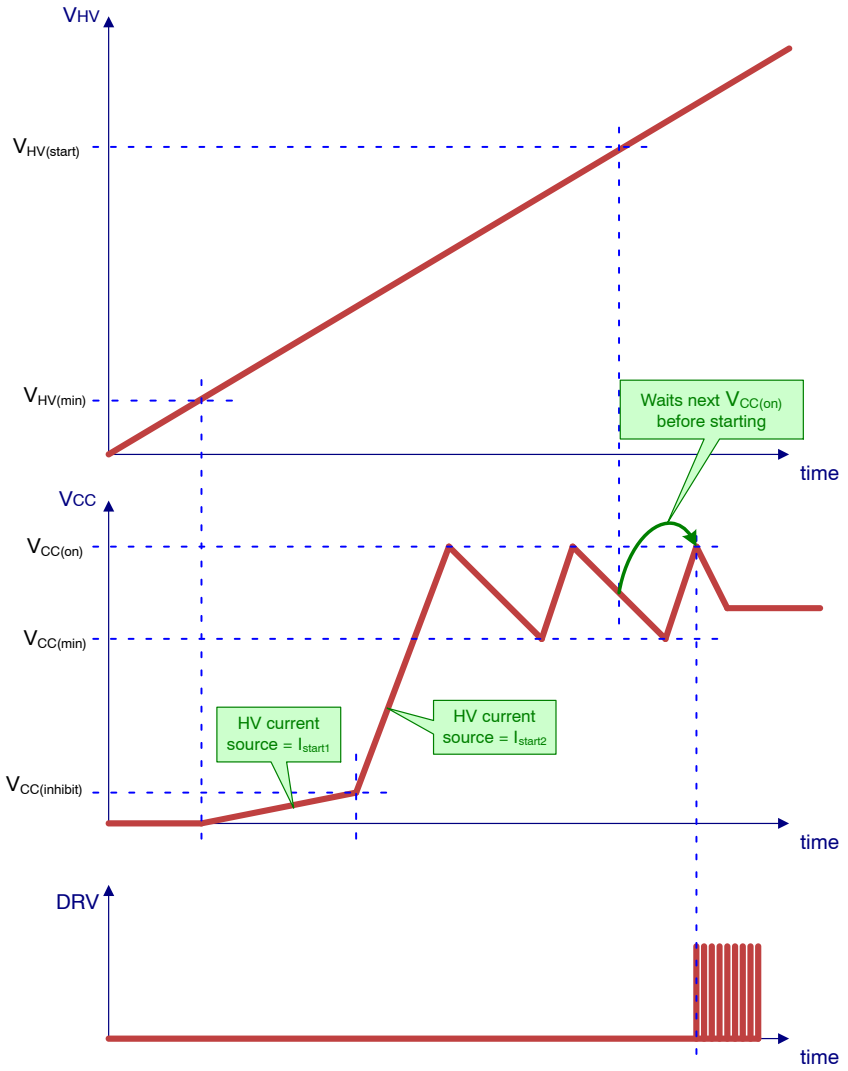


Figure 50. Vcc Start−up Timing Diagram

For safety reasons, the start−up current is lowered when V_{CC} is below $V_{CC(inhibit)}$, to reduce the power dissipation in case the VCC pin is shorted to GND (in case of V_{CC} capacitor failure, or external pull−down on V_{CC} to disable the controller). There is only one condition for which the current source doesn't turn on when V_{CC} reaches $V_{CC(inhibit)}$: the voltage on HV pin is too low (below $V_{HV(min)}$).

Low loss V_{CC} bias

The power adapters designed with variable output may have output voltage range 1:4. Such wide range requires wide range of the V_{CC}. In some cases, e.g. light load conditions, the V_{CC} could drop below the $V_{CC(off)}$ and application may unlikely latch. The low loss V_{CC} bias is designed to prevent such event. The low loss V_{CC} bias helps to keep the V_{CC} above $V_{CC(off)}$ level during the light load conditions in run mode, frequency fold−back mode or skip mode. The dynamic self−supply is quite lossy system to supply the primary controller. Usage of it overheats the controller package in run mode and significantly increases the no load consumption by high voltage drop across the HV startup device. To prevent high drop across the HV startup device inside the IC the HV pin is sensed voltage and the HV startup device could be activated only if the HV voltage is below the $V_{HV(Cstart)}$. This feature enable to keep the stand−by consumption below the desired level 50 mW even at low output voltage level. The time period when the HV startup device could be quite short in comparison with the time when is the V_{CC} pin capacitor discharged so it is needed to increase the HV start−up current level. The 3rd level of the start−up current source is added and named I_{start3}. The typical value of this current is 38 mA. If the effect of the X and Y capacitor is considered to the HV (normally "high Z") pin the valley of the voltage waveform across that pin usually does not drop to zero level. But the voltage across HV pin could drop to 100 V only. That's why he HV startup device is activated after the valley detection event and turned−off after up−crossing the $V_{HV(Cstop)}$ level. If the $V_{CC(on)}$ threshold at VCC pin is reached sooner the V_{CC} is kept at $V_{CC(on)}$ level.

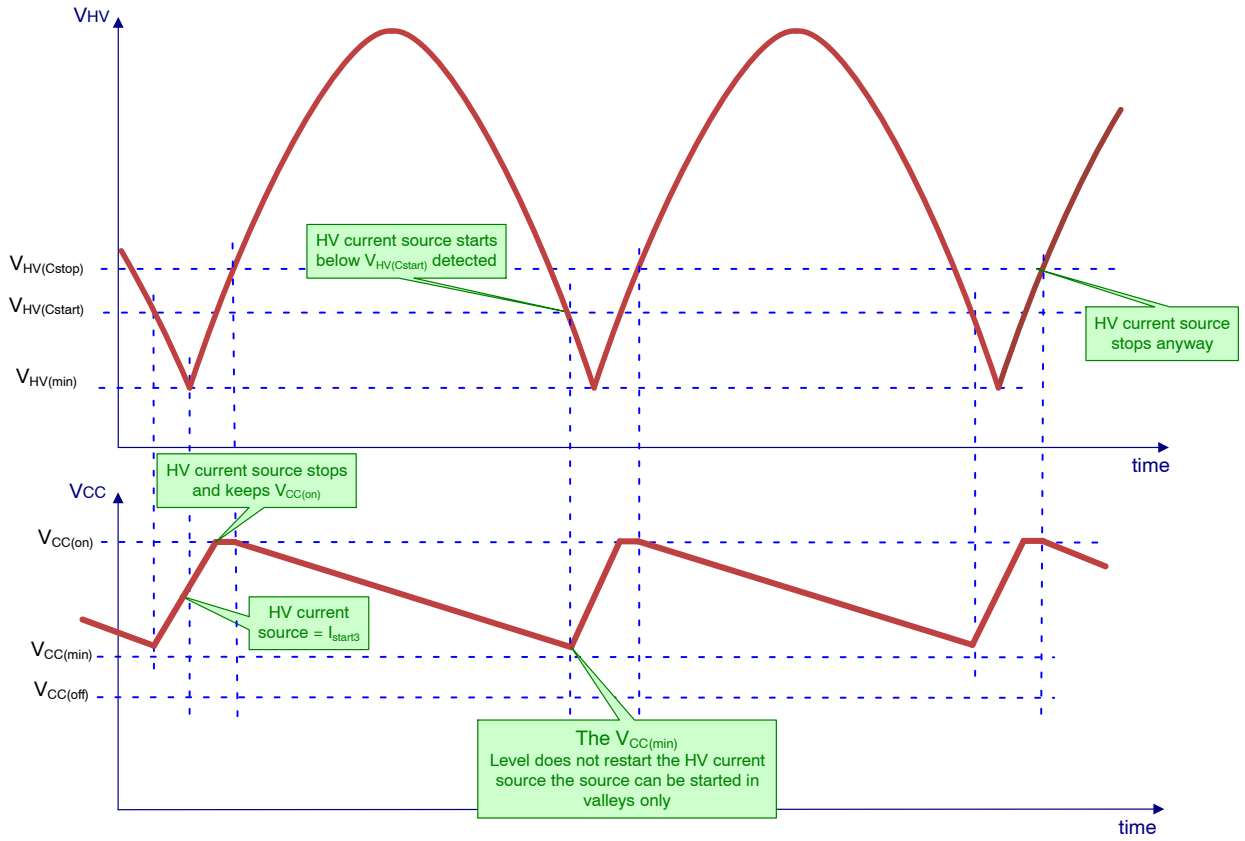


Figure 51. Low Loss V_{CC} Bias under the Low Output Voltage Conditions

HV Sensing of Rectified AC Voltage

The NCP1344 features on its HV pin a true ac line monitoring circuitry. It includes a minimum start−up threshold and an autorecovery brown−out protection and AC line over−voltage protection, both of them independent of the ripple on the input voltage. The brown−out protection thresholds are fixed, but they are designed to fit most of the standard ac−dc conversion applications.

When the input voltage goes below $V_{HV(stop)}$, a brown−out condition is detected, and the controller stops. The HV current source maintains V_{CC} between $V_{CC(on)}$ and $V_{CC(min)}$ levels until the input voltage is back above $V_{HV(start)}$.

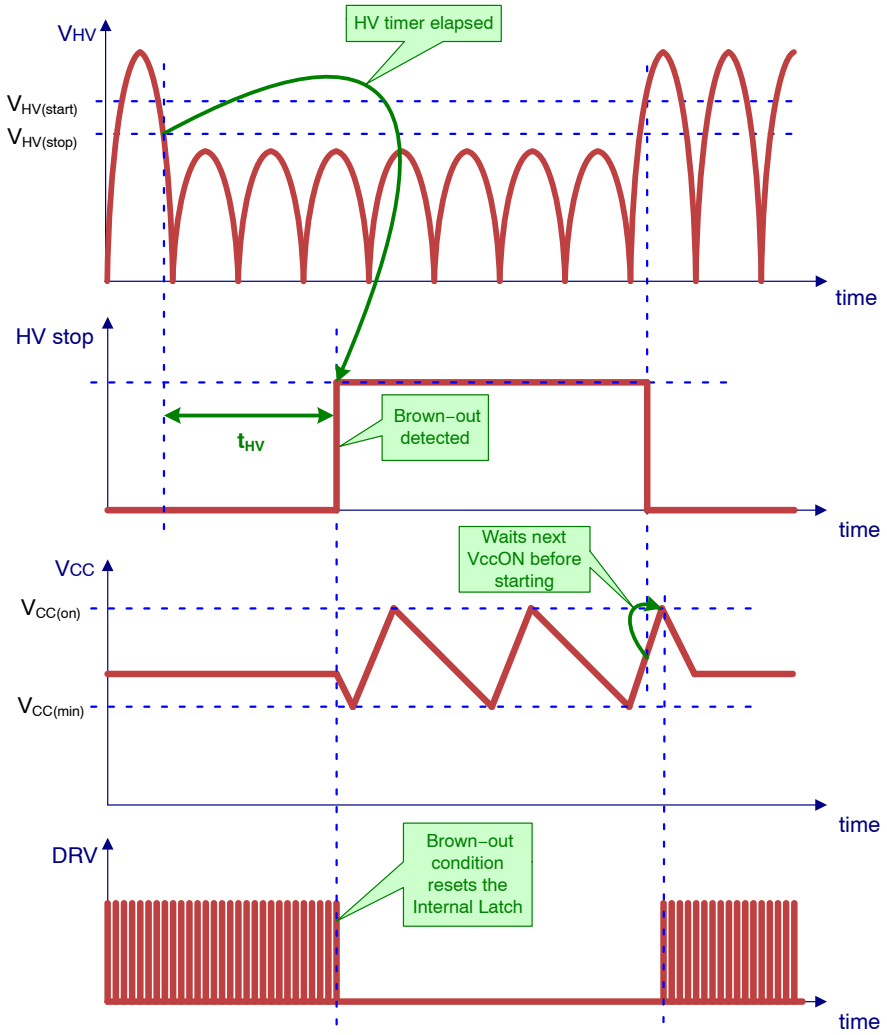


Figure 52. A_C Line Drop−out Timing Diagram

When V_{HV} crosses the $V_{HV(start)}$ threshold, the controller can start immediately. When it crosses $V_{HV(stop)}$, it triggers a timer of duration t_{HV}, this ensures that the controller doesn't stop in case of line cycle drop−out. When V_{HV} crosses the $V_{HV(start)}$ threshold, the controller starts when the V_{CC} crosses the next $V_{CC(on)}$ event. When it crosses $V_{HV(stop)}$, it triggers a timer of duration t_{HV}, this ensures that the controller doesn't stop in case of line cycle drop−out.

The same system is used for the Line OVP, except that this time the controller must not stop instantaneously when the input voltage goes above $V_{HV(OV1)}$, in order to be insensitive to spikes and voltage surges shorter than $t_{OV(blank)}$. Therefore a blanking circuit is inserted after the output of the comparator. When the overvoltage event occurs, HV OVP signal is set and controller stops. When the HV OVP event finishes and the input voltage is below brown out the controller is stopped (without DRV pulses), than the controller is waiting for another brown out condition.

Frequency Jittering

In order to improve the EMI signature a +/− 20 mV triangular signal is added to the peak current setpoint and modulates the t_{on} in the current sense system. The modulation frequency is 1 kHz by default, but can be selected to different values: 2 kHz, 3 kHz, 4 kHz and 5 kHz.

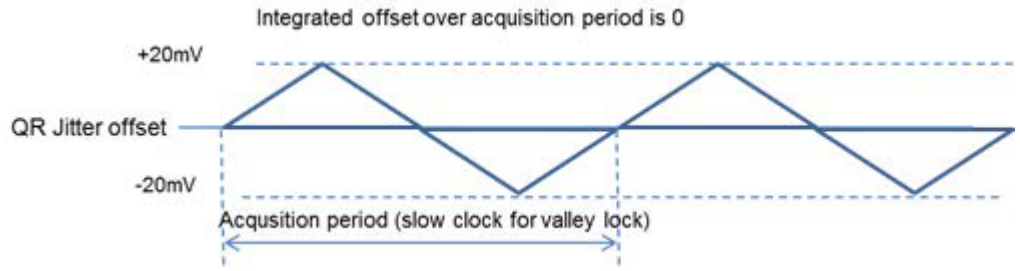


Figure 53. Frequency Modulation of the Current Setpoint in the DCM Mode

Low Load Operation Modes: Frequency Variation Mode (FVM) and Skip Mode

When the load gets lighter, the feedback voltage starts decreasing and drives the control frequency for QR mode. When it reaches V_{foldS} level, the frequency reduces down with increases slope. The slope is reduced when the FB voltage reaches level V_{foldE}. The control frequency for is typically set to 25 kHz at this point and still reduces depending on volage present at FB pin. when V_{FB} reaches 1.8 V. Below this value, f_{sw} is fixed to 25 kHz and down to the skip cycle point, the part operates in peak current mode control. The current setpoint could be optionally fixed to $V_{I(freeze)}$ level in the frequency variation mode if the feedback voltage decreases below the $V_{FB(freeze)}$ level. This feature increases efficiency under the light loads conditions as well.

The controller selects the valley next to the VCO clock, when the frequency reduces and locks in until the next refresh signal comes from the LFC. By using a 5−bit counter, the controller goes down to the 32nd valley. Beyond this point, switching occurs asynchronously. If the demagnetization signal is damped after valley 10 for instance, a time out circuit delivers a pulse to keep triggering the part. When a transient is detected on the feedback voltage (load re− or disconnection), the LFC disappears and refresh is synced to the main 65 kHz clock.

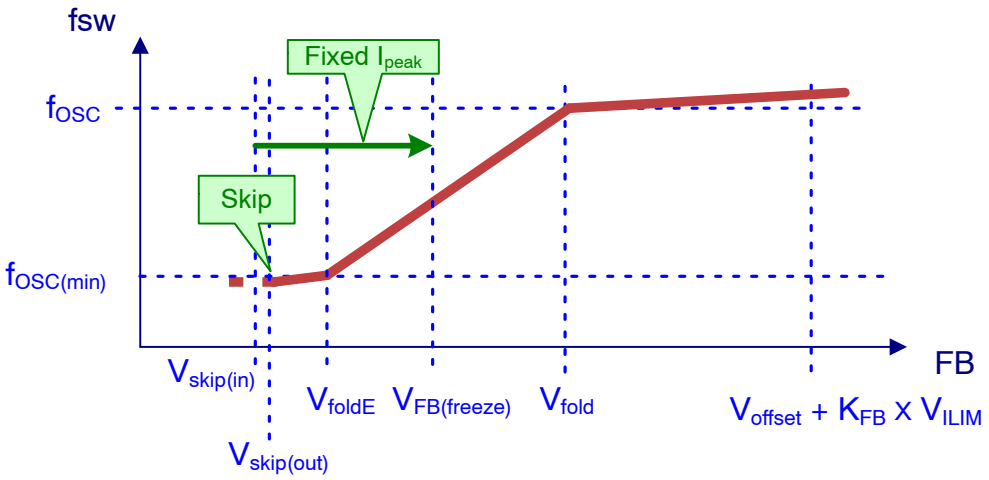


Figure 54. Frequency Variation Mode Characteristic

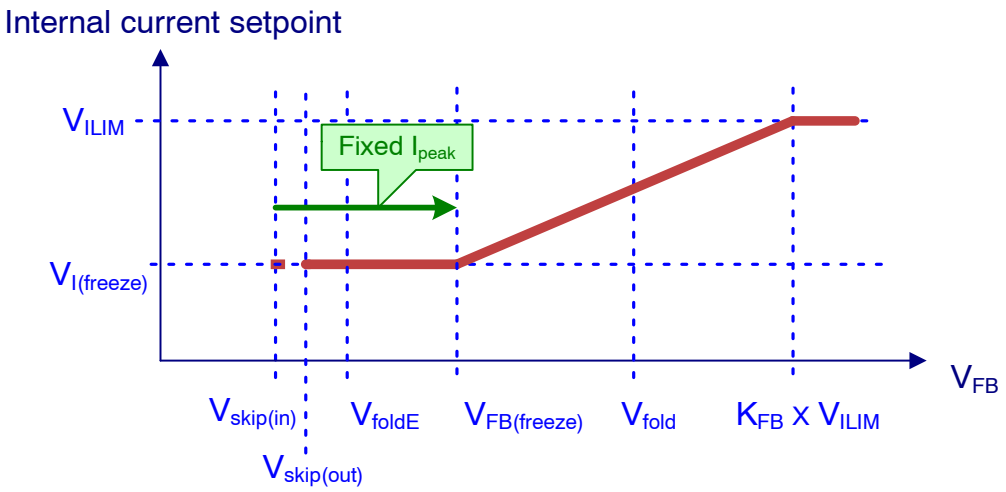


Figure 55. Current Setpoint Dependency on the Feedback Pin Voltage

The frequency variation characteristic is adjustable via the SFF pin by the external resistor to optimize average efficiency in variety of the applications. The setting is done by the external pull down resistor. The resistor value at SFF pin can shift the V_{foldE} and V_{foldS} thersholds by +/− 600 mV. The frequency variation characteristic could eventually depend on the VCC pin voltage. The V_{CC} value at VCC pin can shift the V_{foldE} and V_{foldS} thersholds by +/− 500 mV. Both features ensure the fitting of the system parameters to the setting of the output voltage. This feature allows to effectively build the variable output voltage power supplies. The option when the frequency variation is adjusted via the dedicated pin or by the voltage at VCC pin is selectable by the IPT options.

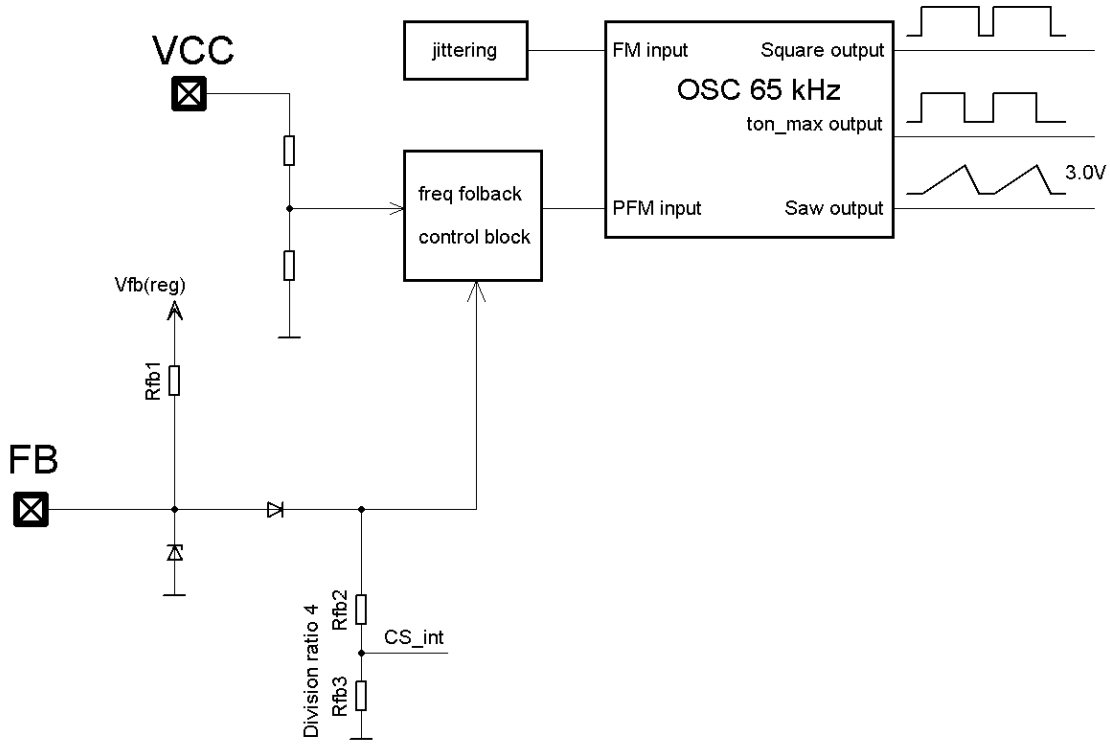


Figure 56. System for Variable Frequency Characteristic

When the FB voltage reaches $V_{skip(in)}$ while decreasing, skip mode is activated: the driver stops, and the internal consumption of the controller is decreased. While V_{FB} is below $V_{skip(out)}$, the controller remains in this state; but as soon as V_{FB} crosses the skip out threshold, the DRV pin starts to pulse again.

The NCP1344 device includes logic which allows going into skip mode after the DRV cycle is finished by reaching of the peak current value. This technique eliminates the last short pulses in skip mode, which increases the system efficiency at light loads and makes easier the application of active secondary rectification circuitry.

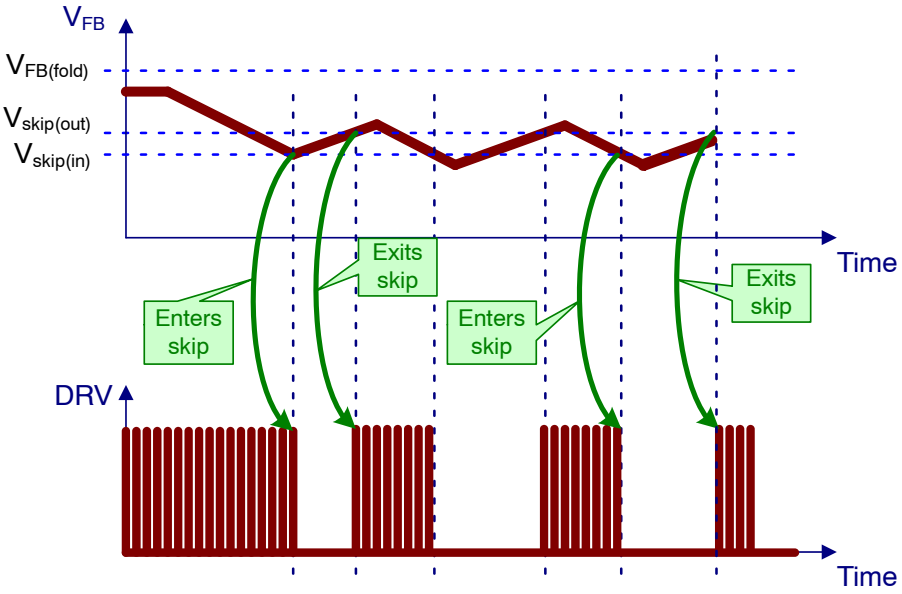


Figure 57. Skip Mode Timing Diagram

Quiet−Skip − Option

To further avoid acoustic noise, the circuit prevents the burst frequency during skip mode from entering the audible range by limiting it to a maximum of 800 Hz. This is achieved via a timer t_{quiet} that is activated during Quiet−Skip. The start of the next burst cycle is prevented until this timer has expired. As the output power decreases, the switching frequency decreases. Once it hits minimum switching frequency $f_{OSC(min)}$, the skip−in threshold is reached and burst mode is entered − switching stops as soon as the current drive pulses ends – it does not stop immediately.

Once switching stops, FB will rise. As soon as FB crosses the skip−exit threshold, drive pulses will resume, but the controller remains in burst mode. At this point, a 1250 µs (typ) timer t_{quiet} is started together with a count to $n_{P,skip}$ pulses counter. This $n_{P,skip}$ pulses counter ensures the minimum number of DRV signal pulses in burst. The next time the FB voltage drops below the skip−in threshold, DRV pulses stop at the end of the current pulse as long as $n_{P,skip}$ drive pulses have been counted (if not, they do not stop until the end of the $n_{P,skip}$ −th pulse). They are not allowed to start again until the timer expires, even if the skip−exit threshold is reached first. It is important to note that the timer will not force the next cycle to begin – i.e. if the natural skip frequency is such that skip−exit is reached after the timer expires, the drive pulses will wait for the skip−exit threshold.

This means that during no−load, there will be a minimum of $n_{P,skip}$ drive pulses, and the burst−cycle period will likely be much longer than 1250 µs. This operation helps to improve efficiency at no−load conditions.

In order to exit burst mode, the FB voltage must rise higher than $V_{skip(tran)}$ level. If this occurs before t_{quiet} expires, the drive pulses will resume immediately – i.e. the controller won't wait for the timer to expire. Figure 59 provides an example of how Quiet−Skip works, while Figure 58 shows the immediate leaving the quiet skip mode by crossing the transient enhancement level $V_{skip(tran)}$.

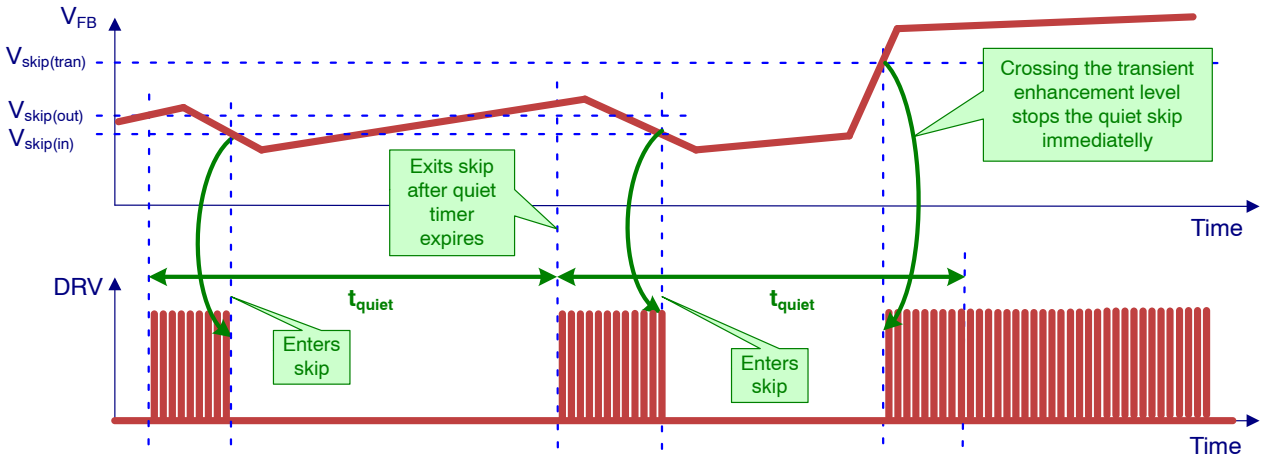


Figure 58. Leaving the Quiet−Skip Mode during Load Transient

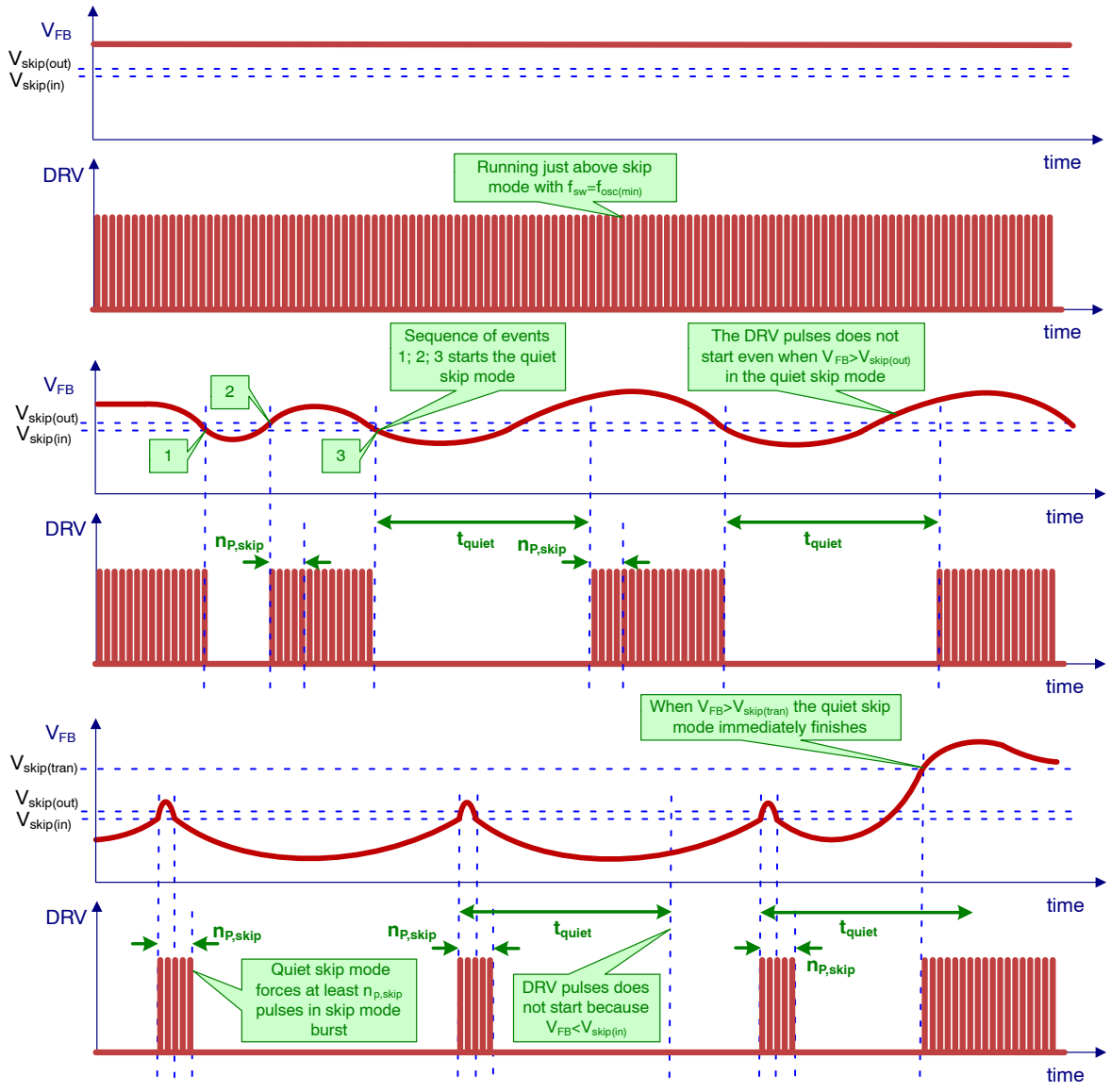


Figure 59. Quiet−Skip Timing Diagram − Option

Clamped Driver

The supply voltage for the NCP1344 can be as high as 37 V, but most of the MOSFETs that will be connected to the DRV pin cannot accept more than 20 V on their gate. The driver pin is therefore safely clamped below 16 V. This driver has a typical capability of 300 mA for source current and 500 mA for sink current.

Current−mode Control with Slope Compensation and Soft−start

NCP1344 is a current−mode controller, which means that the FB voltage sets the peak current flowing in the transformer primary inductance and the MOSFET. This is done through a PWM comparator: the current is sensed across a resistor and the resulting voltage is applied to the CS pin. It is applied to one input of the PWM comparator through a 250 ns LEB block. On the other input the FB voltage divided by 5.4 (optionally 4) sets the threshold: when the voltage ramp reaches this threshold, the output driver is turned off. The maximum value for the current sense is 0.7 V, and it is set by a dedicated comparator.

Each time the controller is starting, i.e. the controller was off and starts – or restarts – when V_{CC} reaches $V_{CC(on)}$, a soft−start is applied: the current sense set−point is increased by 32 discrete steps from 0 (the minimum level can be higher than 0 because of the LEB and propagation delay) until it reaches V_{ILIM} (after a duration of t_{SSTART}), or until the FB loop imposes a setpoint lower than the one imposed by the soft−start (the 2 comparators outputs are OR'ed).

During the soft−start the oscillator frequency increase from the minimum switching frequency to the maximum switching frequency following the ramp applied to current sense set−point.

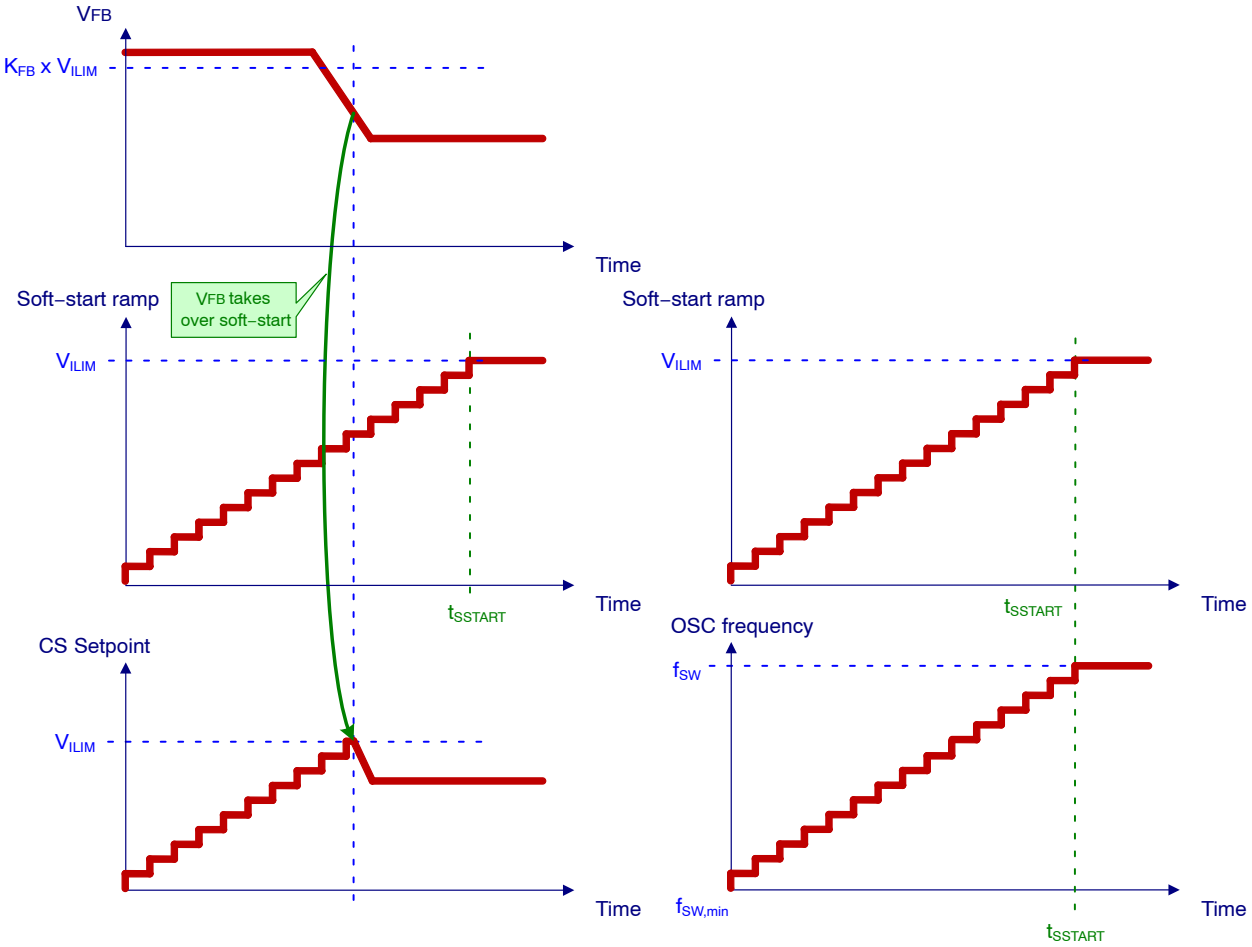


Figure 60. Soft−start Feature

Under some conditions, like a winding short−circuit for instance, not all the energy stored during the on−time is transferred to the output during the off−time, even if the on−time duration is at its minimum (imposed by the propagation delay of the detector added to the LEB duration). As a result, the current sense voltage keeps on increasing above V_{ILIM}, because the controller is blind during the LEB blanking time. Dangerously high current can grow in the system if nothing is done to stop the controller. That's what the additional comparator, that senses when the current sense voltage on CS pin reaches $V_{CS(stop)}$ (= 1.5 x V_{ILIM}), does: as soon as this comparator toggles, the controller immediately enters the protection mode.

Internal Overpower Protection

The power delivered by a flyback power supply is proportional to the square of the peak current in discontinuous conduction mode:

$$P_{OUT} = \frac{1}{2} \times \eta \times L_P \times F_{SW} \times I^2_P \qquad \text{(eq. 1)}$$

Unfortunately, due to the inherent propagation delay of the logic, the actual peak current is higher at high input voltage than at low input voltage, leading to a significant difference in the maximum output power delivered by the power supply.

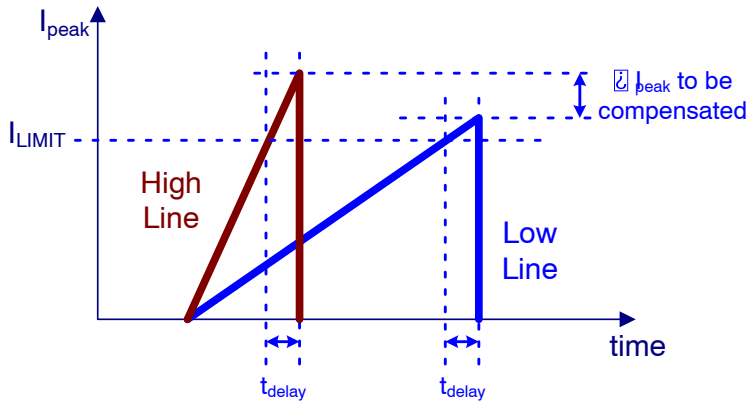


Figure 61. Needs for Line Compensation for True Overpower Protection

To compensate this and have an accurate overpower protection, when the part switches, a small negative voltage is applied at the demagnetization pin during the on−time. After a 600 ns blanking time, this negative voltage is directly added to the maximum current sense voltage reference of 700 mV. A positive 60 mV offset is internally created in series with the demagnetization voltage prior to adding it to the reference voltage. If we assume −60 mV observed on the demagnetization pin during t_{on} for a 120 V input voltage, the net OPP contribution at this low line is 0% and the controller offers the full peak current dynamics. As the input voltage increases, the resulting negative OPP voltage (after the 60 mV offset) grows and starts reducing the maximum sense voltage. By adjusting how negative the demagnetization pin swings during the on−time, the user has a means to reduce the maximum output power in fault condition.

Precaution should be taken regarding this pin as it permanently switches below ground. A maximum of 300 mV should be possible without adverse operation form this IC. Also, clamping precaution must ensure that if this pin is accidentally biased to a positive level, the maximum peak current setpoint of 0.7 V must remain unaffected.

Overcurrent Protection with Fault Timer

The overload protection depends only on the current sensing signal, making it able to work with any transformer, even with very poor coupling or high leakage inductance.

When an overcurrent occurs on the output of the power supply, the FB loop asks for more power than the controller can deliver, and the CS set−point reaches V_{ILIM}. When this event occurs, an internal t_{fault} timer is started: once the timer times out, DRV pulses are stopped and the controller is latched off. Other possibilities of the latch release are the brown−out condition or the V_{CC} power on reset. The timer is reset when the CS set−point goes back below V_{ILIM} before the timer elapses. The controller also enters the same protection mode if the voltage on the CS pin reaches 1.5 times the maximum internal set−point $V_{CS(stop)}$ (allows to detect winding short−circuits) or there appears low V_{CC} supply. See Figure 62 for the timing diagrams.

PROTECTION MODES AND THE LATCH MODE RELEASES

Event	Timer protection	Next device status	Release to normal operation mode
Overcurrent $V_{CS} \geq V_{ILIM}$	Fault timer	Latch	Autorecovery – depends on version Brown−out $V_{CC} < V_{CC(reset)}$
Peak power $V_{CS} > V_{CS(tran)}$	Transient timer	Latch	Autorecovery – depends on version Brown−out $V_{CC} < V_{CC(reset)}$
Maximum duty cycle	Fault timer	Latch	Autorecovery – depends on version Brown−out $V_{CC} < V_{CC(reset)}$
Auto tuning over−current (I_{OUT} limit)	Fault timer	Latch	Autorecovery – depends on version Brown−out $V_{CC} < V_{CC(reset)}$
Winding short $V_{CS} > V_{CS(stop)}$	4 consecutive pulses	Latch	Autorecovery – depends on version Brown−out $V_{CC} < V_{CC(reset)}$
Low supply $V_{CC} < V_{CC(off)}$	10 μs timer	Latch	Autorecovery – depends on version Brown−out $V_{CC} < V_{CC(reset)}$
External OTP	350 μs	Latch	Autorecovery – depends on version Brown−out $V_{CC} < V_{CC(reset)}$
External OTP at CS	8 consecutive pulses	Latch	Autorecovery – depends on version Brown−out $V_{CC} < V_{CC(reset)}$
External OVP at ZCD	8 consecutive pulses	Latch	Autorecovery – depends on version Brown−out $V_{CC} < V_{CC(reset)}$
Low V_{OUT}	8 consecutive pulses	Latch	Autorecovery – depends on version Brown−out $V_{CC} < V_{CC(reset)}$
High supply $V_{CC} > V_{CC(ovp)}$	10 μs timer	Latch	Brown−out $V_{CC} < V_{CC(reset)}$
Brown−out $V_{HV} < V_{HV(stop)}$	HV timer	Device stops	$(V_{HV} > V_{HV(start)})\&(V_{CC} > V_{CC(on)})$
Internal TSD	10 μs timer	Device stops, HV start−up current source stops	$(V_{HV} > V_{HV(start)})\&(V_{CC} > V_{CC(on)})\&$TSDb

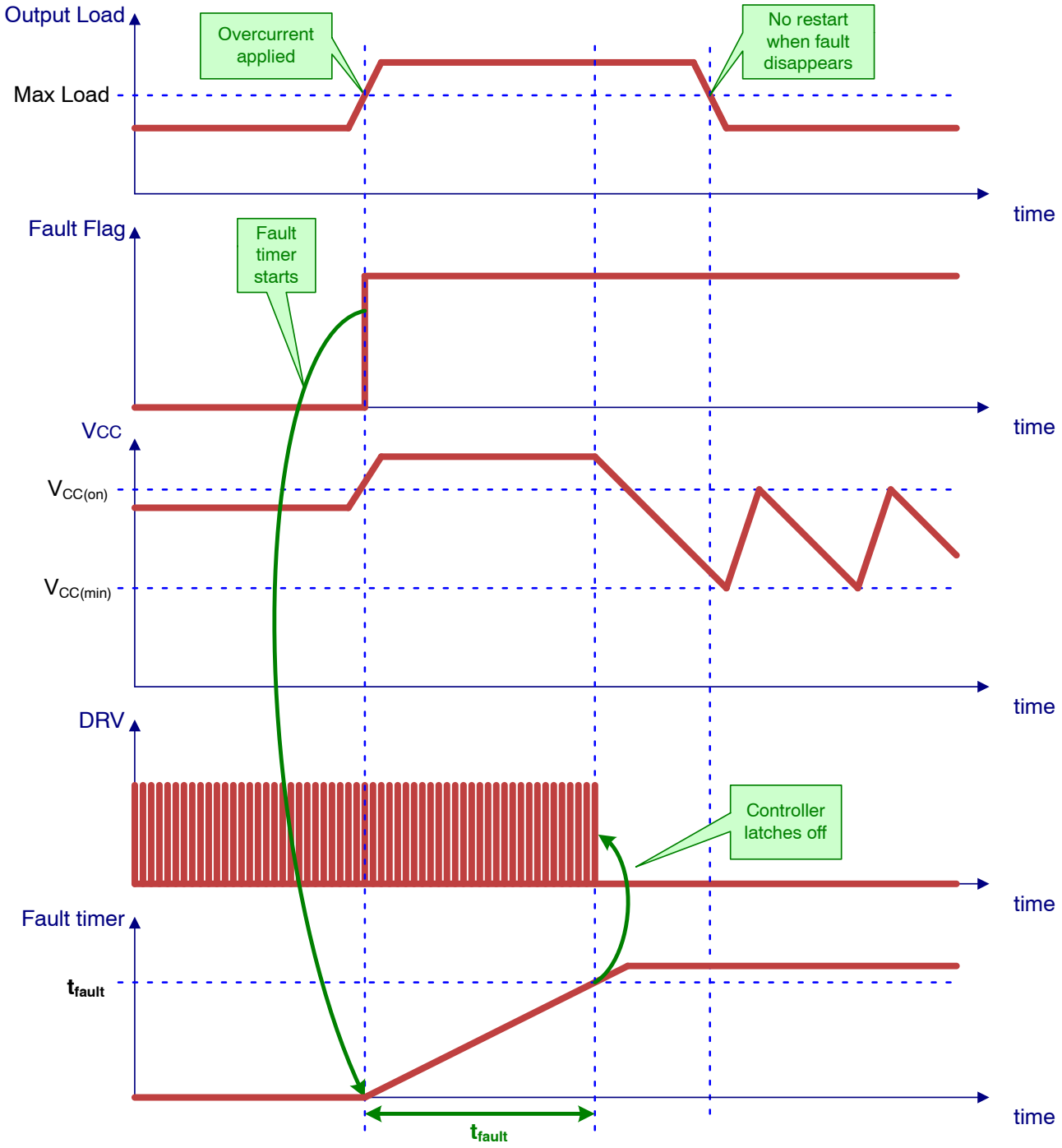


Figure 62. Latched Timer−based Overcurrent Protection

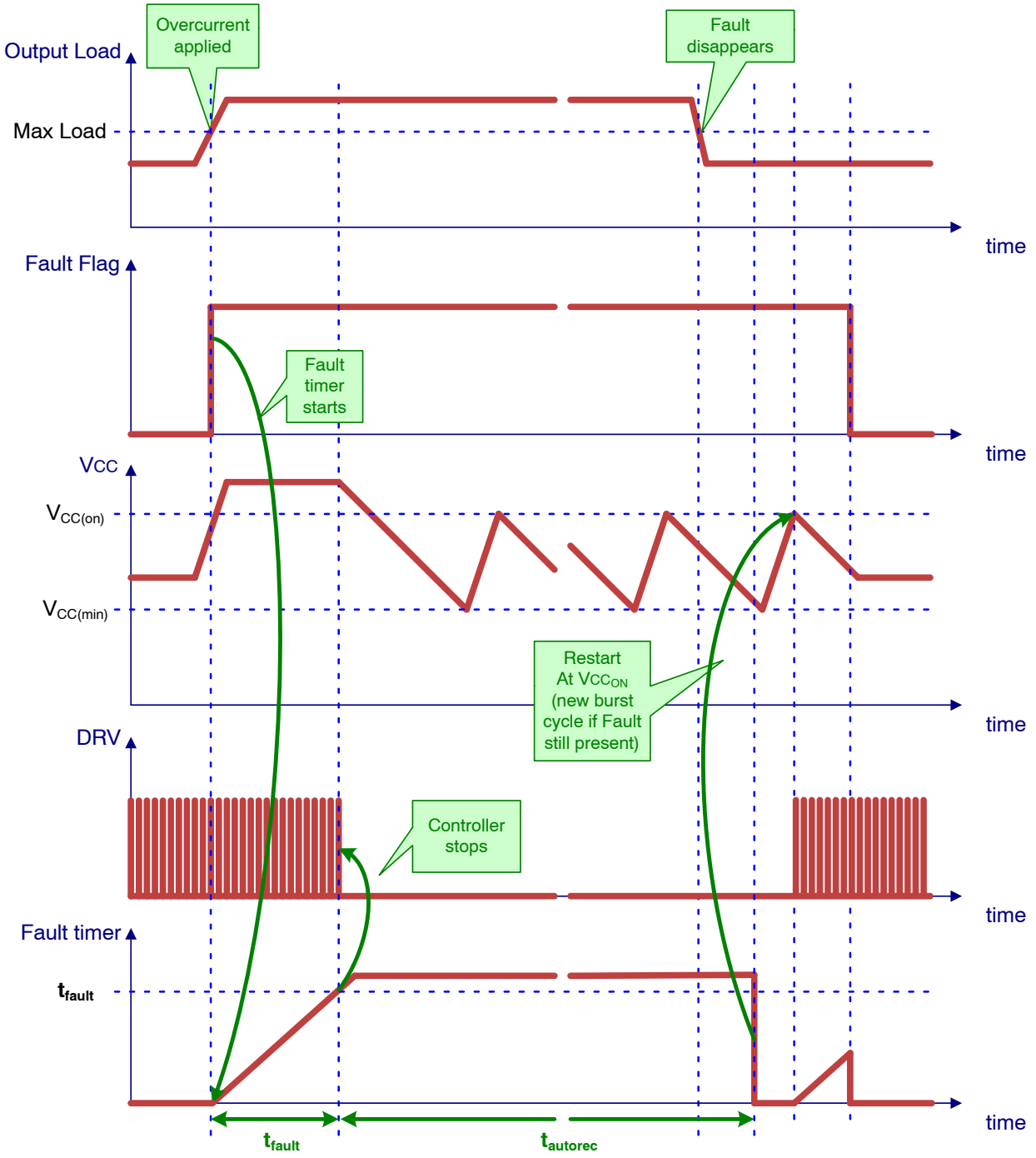


Figure 63. Timer−based Protection Mode with Autorecovery Release from Latch−off

Auto−tuning Over−current Protection

The variable output is required for applications like power delivery via the USB cable depending on the load setup. The new USB−PD adapter design needs include the ability to limit maximum output current at any level of the output voltage to pass the safety requirements. The problem is that the flyback converter controlled by peak current mode is naturally the source of the constant power, when the regulation loop saturates and delivers full power. If the output voltage level is decreased by the control circuit, the converter can deliver higher output current under overload conditions. This can exceed the safe limit. The device limiting the output current could be placed at the secondary side of the SMPS. In case of single fail of this protection the maximum output current of the SMPS is limited by the primary side protection to increase the safety level of the design.

Low Output Voltage Protection

When the converter undergoes a short circuit, V_{out} collapses to a few volts and the feedback pin goes to the max value. Switching frequency is usually clamped at its

maximum value in this mode. This mode is dangerous for the power supply as a deep continuous conduction mode (CCM) operation can be entered with peak current runaway. If no precautions are taken, the drain clamping voltage can easily exceed the MOSFET breakdown voltage and destruction occurs. A secondary−side synchronous rectifier could also be damaged in this mode if it is present. To ensure an efficient protection, a comparator permanently checks the demagnetization voltage 1.5 μs on ZCD pin after the MOSFET has open. If this voltage is above 0.4 V during t_{off}, it means the output voltage is high enough to ensure demagnetization. When V_{FB} goes up, this is ok and can last at least 16 ms before latch or auto−recovery is entered (latched version or auto−recovery version). However, if the feedback voltage asks for the maximum frequency and the demagnetization voltage during t_{off} is less than 0.4 V, then V_{out} is too low or even in short circuit. When both events are detected, the controller toggles its switching frequency to 65 kHz and accepts the situation for 8 clock cycles. After that, it activates a latch or an auto−recovery event depending on the selected option. If while in SCP the demagnetization voltage returns above 0.5 V for 8 clock cycles, then the maximum frequency clamp lock is reset and f_{sw} is free again to follow V_{FB} and activates (or keeps counting) the fault timer if necessary (V_{FB} is high again but not in a shorted V_{out} situation).

Please note that while the soft start flag is high, as f_{sw} is stuck to clamp in this start−up mode, the controller ignores the low V_{ZCD} flag until the soft−start is over. After the 5 ms soft−start, if the V_{ZCD} flag is asserted (the voltage is still less than 0.4 V after soft start), then the part immediately latches off or auto−recovers depending on the selected option.).

OVP Protection at ZCD Pin

The controller monitors cycle by cycle the voltage on the demagnetization pin after a blanking time. This blanking time is 1.5 μs and is there to make sure the leakage ringing is fully damped. After 8 successive OVP events, the part latches off. In case, the OVP disappears before the 8 cycles are counted, the counter resets and waits for another event.

Temperature Shutdown

The NCP1344 includes a temperature shutdown protection with a trip point typically at 150°C and with typical hysteresis of 40°C. When the temperature rises above the high threshold, the controller stops switching instantaneously, and goes to the off mode with extremely low power consumption. There is kept the V_{CC} supply to keep the TSD information. When the temperature falls below the low threshold, the start−up of the device is enabled again, and a regular start−up sequence takes place.

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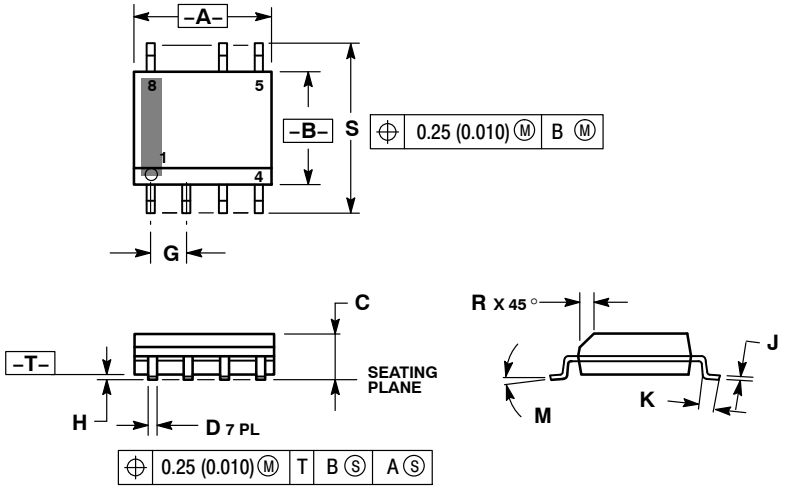
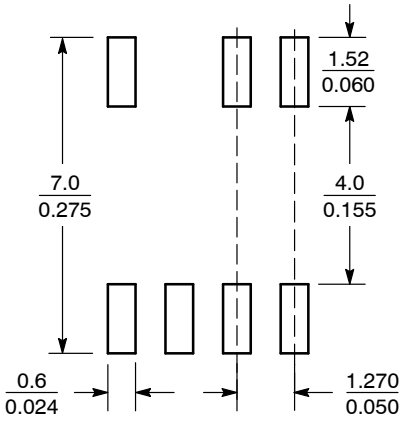
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

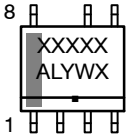
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

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STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY M. JONES	14 NOV 2002
A	REPLACED ALL PIN 7 IN STYLES WITH “NOT USED”. REQ BY M. JONES	06 DEC 2002
B	ADMINISTRATIVE CHANGE	07 JAN 2003
C	CORRECTED DIMENSIONS K AND H. REQ. BY M. JONES	03 JAN 2005
D	CORRECTED DEVICE MARKING INFORMATION FROM “AYWW” TO ALYW”. ADDED PIN 1 BARS TO DIAGRAMS. REQ. BY S. BROW.	25 MAY 2007
E	ADDED SOLDER FOOTPRINT. REQ. BY D. BRIGGS.	20 OCT 2009

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