# STLJFS014N04M8L

# MOSFET, Single N-Channel, POWERTRENCH®

## 40 V, 10 A, 14 mΩ

### General Description

This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $r_{DS(on)}$ and gate charge provide excellent switching performance.

### Features

- Max $r_{DS(on)}$ = 14 mΩ at $V_{GS}$ = 10 V, $I_D$ = 10 A
- Max $r_{DS(on)}$ = 18 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 8.5 A
- Low Profile – 0.8 mm maximum in the new package MicroFET 2 x 2 mm
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

### Application

- DC–DC Buck Converters

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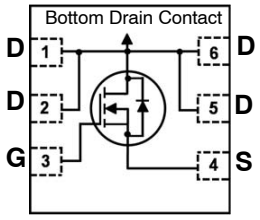
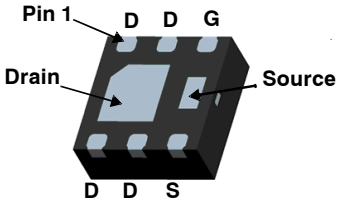
### ELECTRICAL CONNECTION

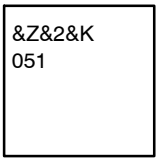



**Single N-Channel MOSFET**




**MicroFET 2x2**
**(WDFN6 2x2, 0.65P)**
**CASE 511DB**

### MARKING DIAGRAM




&Z = Assembly Plant Code
&2 = Numeric Date Code
&K = Lot Code
051 = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

### MOSFET MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 40 | V |
| $V_{GS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Drain Current – Continuous $T_A$ = 25°C (Note 2a) | 10 | A |
| | – Pulsed (Note 4) | 80 | |
| $P_D$ | Power dissipation $T_A$ = 25°C (Note 2a) | 2.4 | W |
| | Power dissipation $T_A$ = 25°C (Note 2b) | 0.9 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | –55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 2a) | 52 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 2b) | 145 | |

### PACKAGE MARKING AND ORDERING INFORMATION

| Device Marking | Device | Package | Shipping† |
|---|---|---|---|
| 051 | STLJFS014N04M8L | MicroFET 2x2 | 3000 Units/ Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

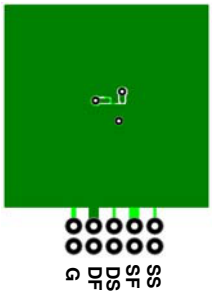
**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 40 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | | 22 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 32 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate−to−Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1.0 | 1.6 | 3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | | −5 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 10 A | | 11 | 14 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 8.5 A | | 14 | 18 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 10 A, $T_J$ = 125°C | | 15 | 19 | |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = 5 V, $I_D$ = 10 A | | 35 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, f = 1MHz | | 901 | 1260 | pF |
| $C_{oss}$ | Output Capacitance | | | 251 | 350 | |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 16 | 25 | |
| $R_g$ | Gate Resistance | | 0.1 | 0.6 | 1.8 | Ω |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $td_{(on)}$ | Turn – On Delay Time | $V_{DD}$ = 20 V, $I_D$ = 10 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 6.4 | 13 | ns |
| $t_r$ | Rise Time | | | 1.8 | 10 | |
| $t_{D(off)}$ | Turn – Off Delay Time | | | 17 | 31 | |
| $t_f$ | Fall Time | | | 1.8 | 10 | |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0V to 10 V | | 14 | 20 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0V to 4.5 V | | 6.4 | 9.0 | |
| $Q_{gs}$ | Total Gate Charge | $V_{DD}$ = 20 V, $i_D$ = 10 A | | 2.4 | 3.7 | |
| $Q_{gd}$ | Gate to Source Charge | | | 1.8 | 2.5 | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2 A (Note 3) | | 0.7 | 1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 10 A (Note 3) | | 0.8 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 10 A, di/dt = 100 A/μs | | 23 | 37 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 6.7 | 14 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

2. $R_{\theta JA}$ is determined with the device mounted on a 1 in$^2$ pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.




a) 52°C/W when mounted on a 1 in$^2$ pad of 2 oz copper.


b) 145°C/W when mounted on a minimum pad of 2 oz copper.

3. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
4. Pulsed $I_D$ limited by junction temperature, td<= 100 μS, please refer to SOA curve for more details.

## TYPICAL CHARACTERISTICS $T_J$ = 25°C unless otherwise noted

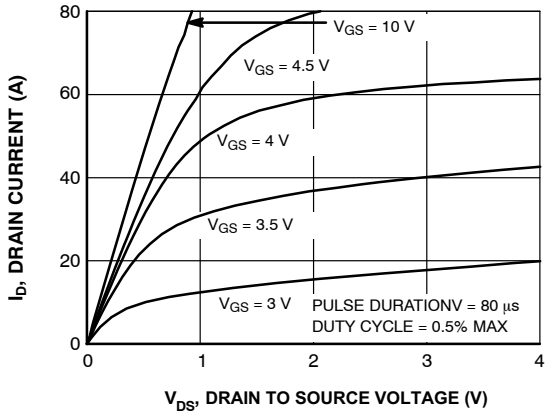



**Figure 14. On Region Characteristics**

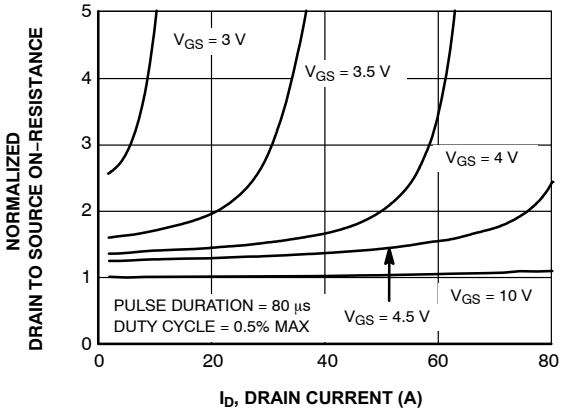



**Figure 15. Normalized On−Resistance vs. Drain Current and Gate Voltage**

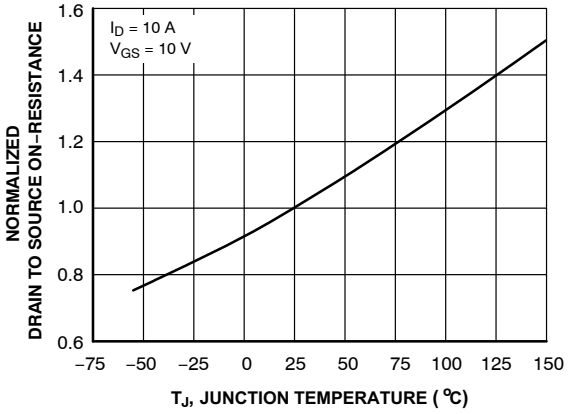



**Figure 16. Normalized On Resistance vs. Junction Temperature**

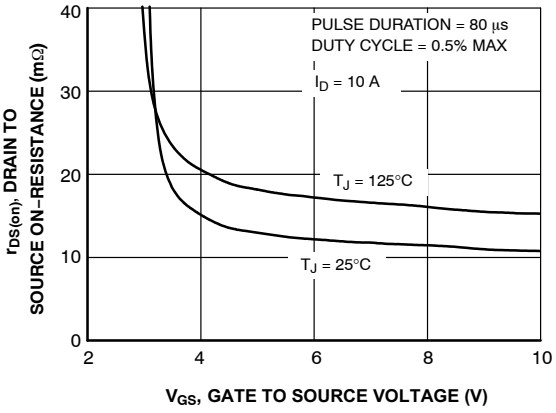



**Figure 17. On−Resistance vs. Gate to Source Voltage**

## TYPICAL CHARACTERISTICS $T_J$ = 25°C unless otherwise noted (continued)

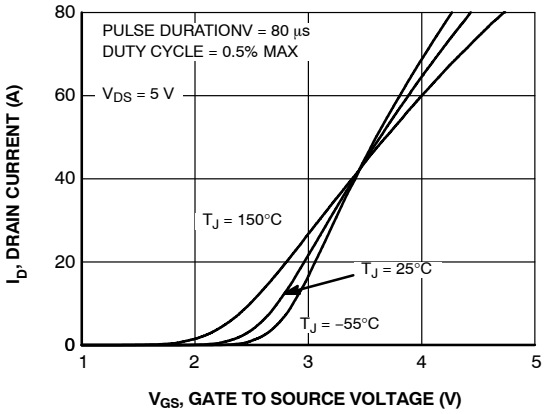



**Figure 18. Transfer Characteristics**

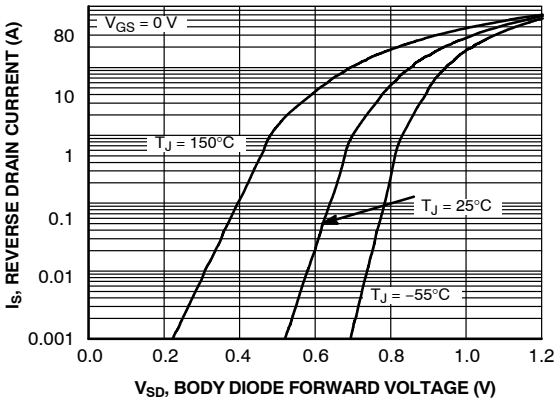



**Figure 19. Source to Drain Diode Forward Voltage vs. Source Current**

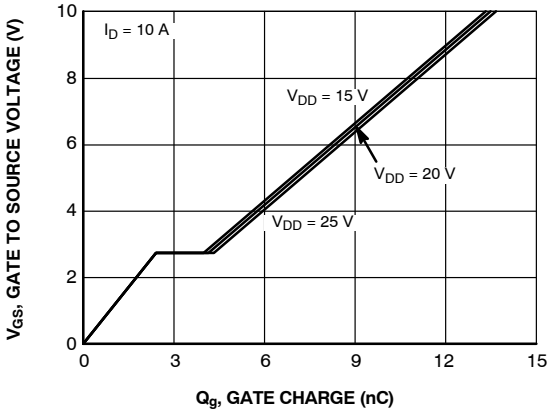



**Figure 20. Gate Charge Characteristics**

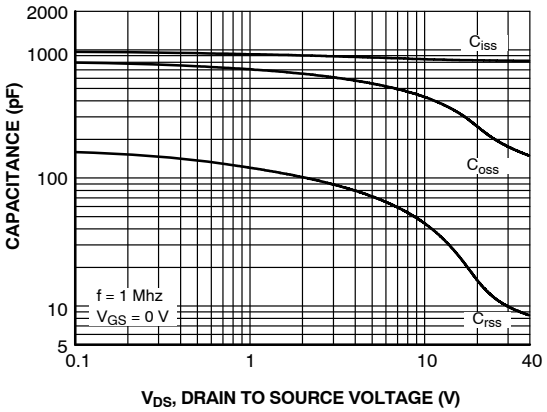



**Figure 21. Capacitance vs. Drain to Source Voltage**

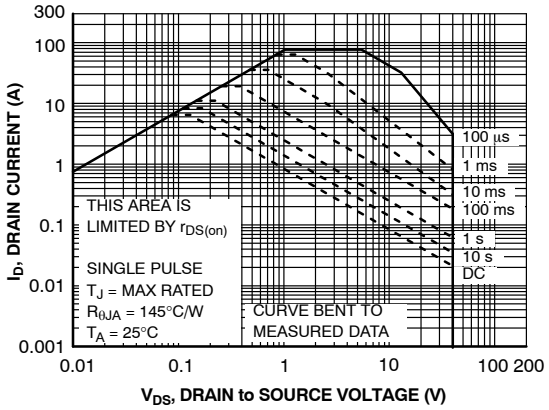



**Figure 22. Forward Bias Safe Operating Area**

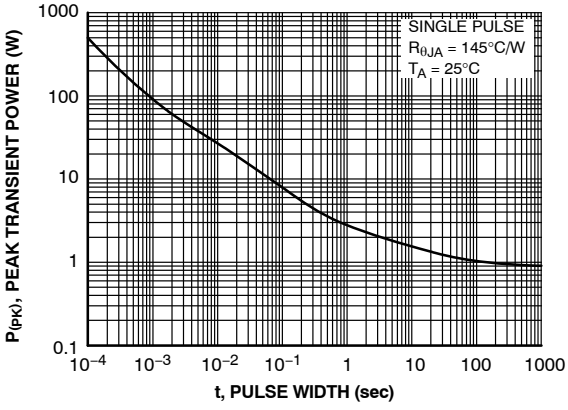



**Figure 23. Single Pulse Maximum Power Dissipation**

**TYPICAL CHARACTERISTICS** $T_J$ = 25°C unless otherwise noted (continued)

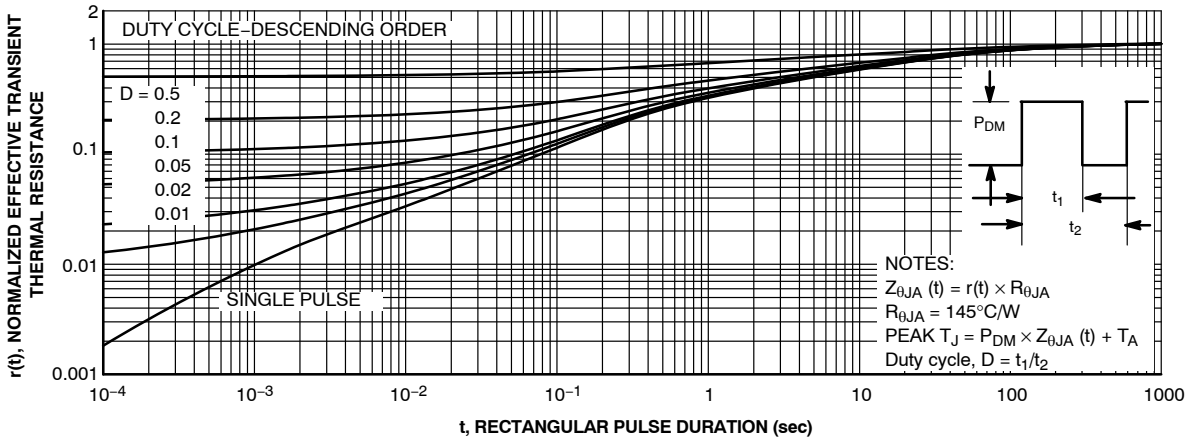



**Figure 24. Single Pulse Junction−to−Ambient Transient Thermal Response Curve**

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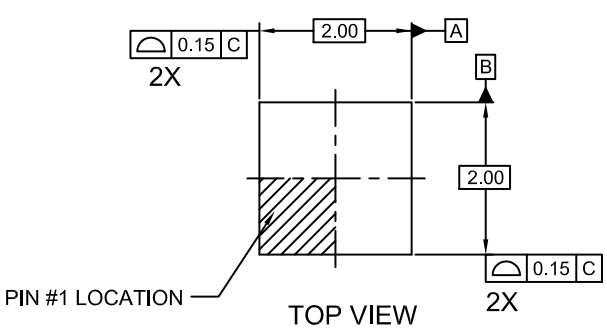
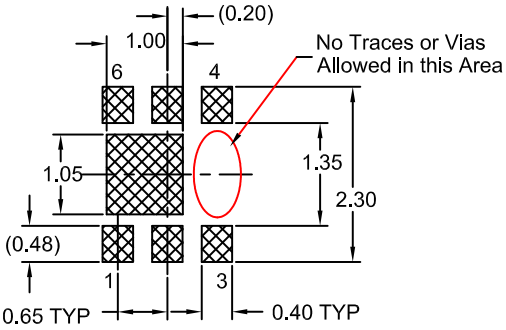
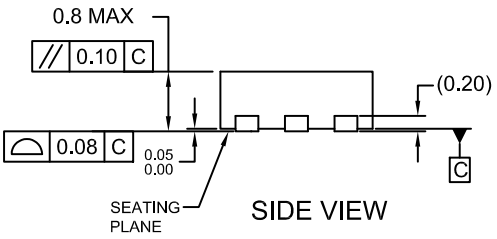
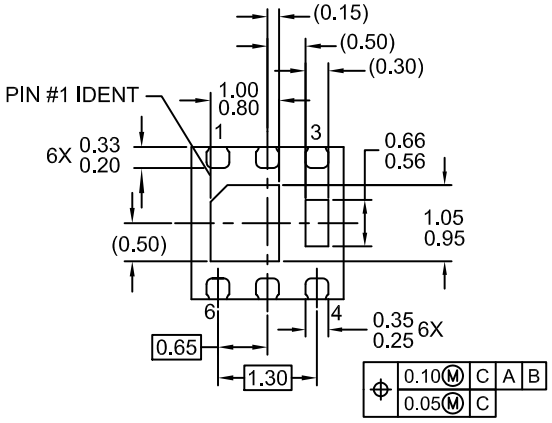


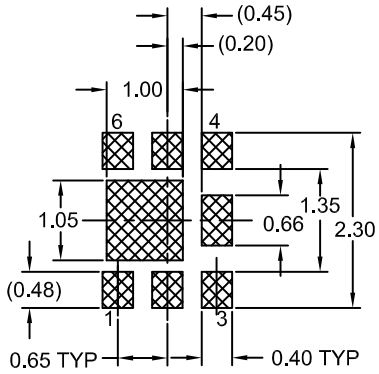




RECOMMENDED LAND PATTERN OPT 1




BOTTOM VIEW




RECOMMENDED LAND PATTERN OPT 2

NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION
MO-229 DATED AUG/2003
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

| ISSUE | REVISION | DATE |
|---|---|---|
| O | RELEASED FOR PRODUCTION FROM FAIRCHILD MLP06P TO ON SEMICONDUCTOR. REQ. BY B. MARQUIS. | 31 AUG 2016 |
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