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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild guestions@onsemi.com.

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April 2015

FDD8445

N-Channel PowerTrench® MOSFET 40V, 50A, 8.7m Ω

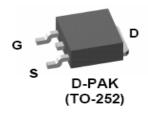
Features

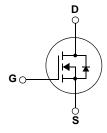
- $R_{DS(ON)} = 6.7 \text{ m}\Omega$ (Typ), $V_{GS} = 10V$, $I_D=50A$
- $Q_{g(10)} = 45nC \text{ (Typ)}, V_{GS}=10V$
- Low Miller Charge
- Low Qrr Body Diode
- UIS Capability (Single Pulse/ Repetitive Pulse)
- RoHS Compliant



Applications

- Powertrain Management
- Electronic Transmission
- Distributed Power Architecture and VRMs
- Primary Switch for 12V Systems





Absolute Maximum Ratings T_c = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
	Drain Current Continuous (V _{GS} =10v) (Note 1)	70	Α
I _D	Continuous ($V_{GS}=10v$, with $R_{\theta JA}=52^{\circ}C/W$)	15.2	Α
	Pulsed	Figure 4	
E _{AS}	SinglePulseAvalancheEnergy (Note2)	144	mJ
В	Power Dissipation	79	W
P_{D}	Derate above 25°C	0.53	W/ºC
T _J , T _{STG}	Operating and Storage Temperature	-55 to +175	°C

Thermal Characteristics

F	$R_{ heta JC}$	Thermal Resistance, Junction to Case	1.9	°C/W
F	$R_{ heta JA}$	Thermal Resistance, Junction to Ambient TO-252, lin ² copper pad area	52	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8445	FDD8445	TO-252AA	13"	16mm	2500 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Тур	Max	Units
Off Chara	acteristics						
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_C$	40	-	-	V	
	Zara Cata Valtaga Drain Current	V _{DS} = 32V		-	-	1	μΑ
IDSS	Zero Gate Voltage Drain Current	$V_{GS} = 0V$	T _J =150°C	-	-	250	
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V$		-	-	±100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	2.8	4	V
		$I_D = 50A, V_{GS} = 10V$	-	6.7	8.7	
R _{DS(ON)}	Drain to Source On Resistance	$I_D = 50A$, $V_{GS} = 10V$, $T_J = 175$ °C	-	12.5	16.3	mΩ

Dynamic Characteristics

-							
C _{ISS}	Input Capacitance	\/ OF\/ \/	V _{DS} = 25V, V _{GS} = 0V, -f = 1MHz		3040	4050	pF
Coss	Output Capacitance				295	390	pF
C _{RSS}	Reverse Transfer Capacitance	1 - 1101112			178	270	pF
R_G	Gate Resistance	f = 1MHz		-	1.7	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V _{GS} = 0 to 10V		-	45	59	nC
Q _{g(5)}	Total Gate Charge at 5V	$V_{GS} = 0$ to 5V		-	17	22	nC
Q _{g(TH)}	Threshold Gate Charge	$V_{GS} = 0$ to $2V$	V _{DD} =20V,	-	5.8	7.6	nC
Q _{gs}	Gate to Source Gate Charge		$I_D = 50A$	-	12.5	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau			-	9.5	-	nC
Q_{qd}	Gate to Drain "Miller" Charge			-	10.5	-	nC

Electrical Characteristics	$T_1 = 25$ °C unless otherwise noted
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Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Switching	g Characteristics					
t _(on)	Turn-On Time		-	-	138	ns
t _{d(on)}	Turn-On Delay Time		-	10	-	ns
t _r	Turn-On Rise Time	$V_{DD} = 20V, I_{D} = 50A$ $V_{GS} = 10V, R_{GS} = 2\Omega$	-	82	-	ns
t _{d(off)}	Turn-Off Delay Time		-	26	-	ns
t _f	Turn-Off Fall Time		-	9.6	-	ns
t _{off}	Turn-Off Time		-	-	53	ns

Drain-Source Diode Characteristics

V _{SD}	Source to Drain Diode Voltage	I _{SD} =50A	-	-	1.25	V
		I _{SD} =25A	-	•	1.0	V
t _{rr}	Reverse Recovery Time	I _F = 50A, dI _F /dt=100A/μs	-	-	39	ns
Q _{rr}	Reverse Recovery Charge	I _F = 50A, dI _F /dt=100A/μs	-	-	38	nC

 $\begin{tabular}{ll} \textbf{Notes:} \\ \textbf{1:} & \text{Maximum package current capability is 50A.} \\ \textbf{2:} & \text{Starting T}_J = 25^{\circ}\text{C}, L=0.18\text{mH, I}_{AS}=40\text{A}. \\ \end{tabular}$

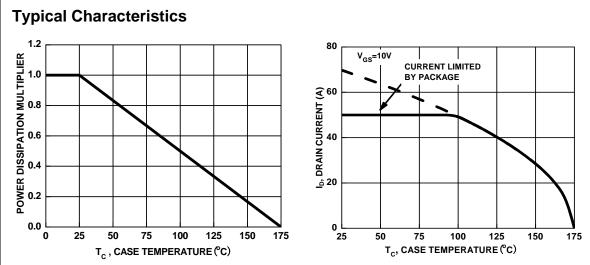


Figure 1. Normalized Power Dissipation vs Case Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

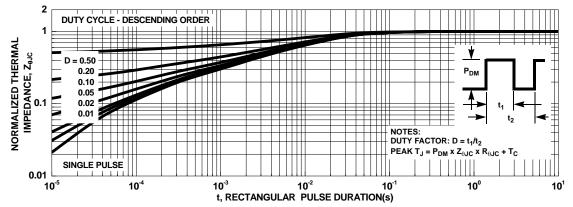


Figure 3. Normalized Maximum Transient Thermal Impedance

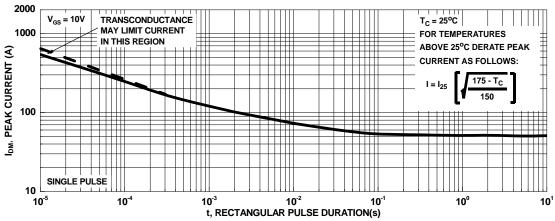
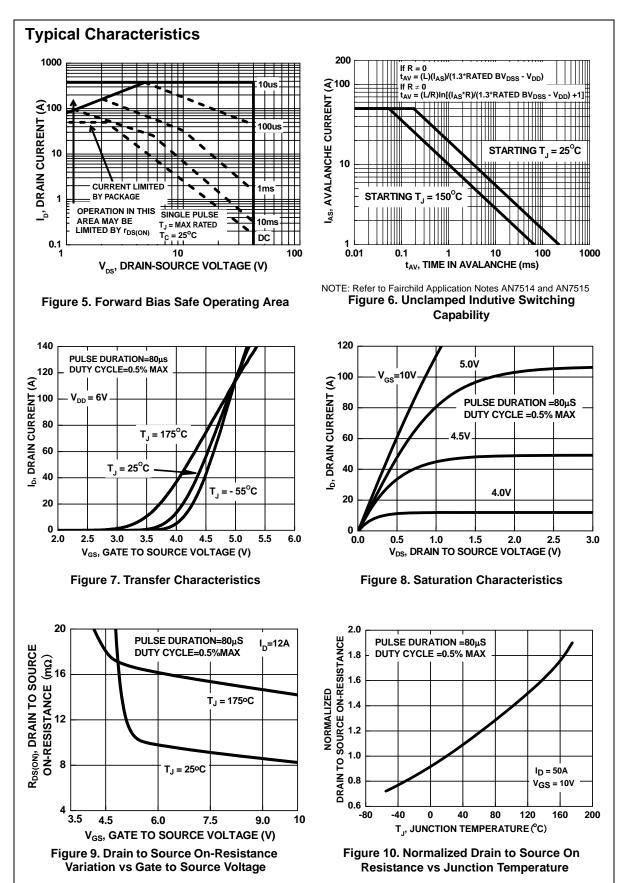


Figure 4. Peak Current Capability



Typical Characteristics

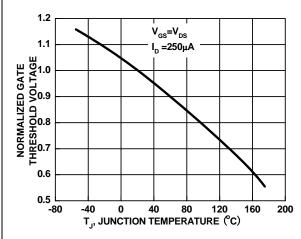


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

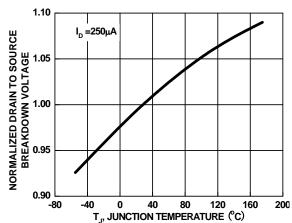


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

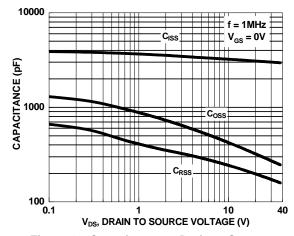


Figure 13. Capacitance vs Drain to Source Voltage

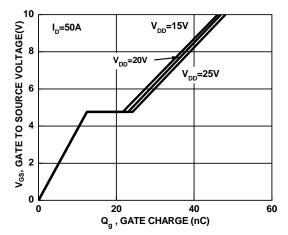
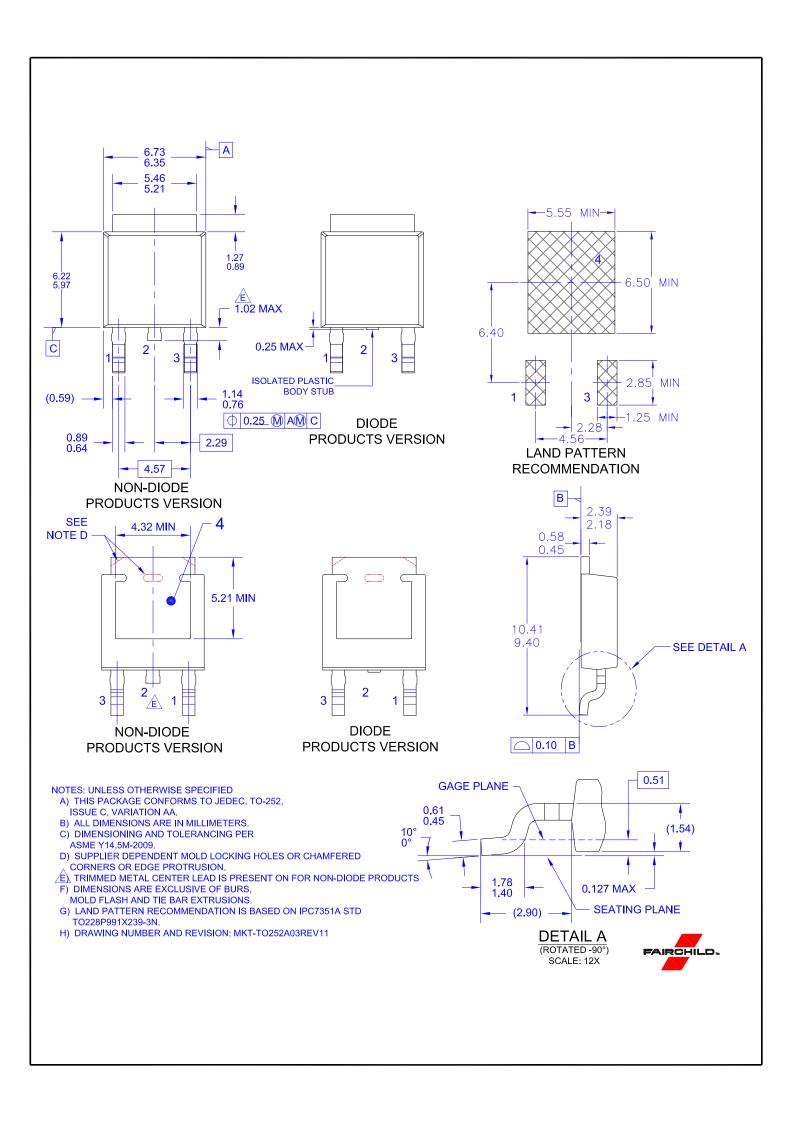


Figure 14. Gate Charge vs Gate to Source Voltage



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