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FAIRCHILD SEMICONDUCTOR™

September 2001

FDC6420C

20V N & P-Channel PowerTrench® MOSFETs

General Description

These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

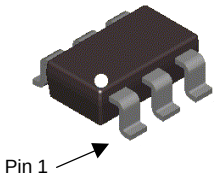
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

Applications

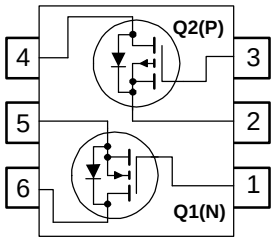
- DC/DC converter
- Load switch
- LCD display inverter

Features

- **Q1** 3.0 A, 20V. $R_{DS(ON)}$ = 70 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 95 mΩ @ V_{GS} = 2.5 V
- **Q2** –2.2 A, 20V. $R_{DS(ON)}$ = 125 mΩ @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 190 mΩ @ V_{GS} = –2.5 V
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$.
- SuperSOT –6 package: small footprint (72% smaller than SO-8); low profile (1mm thick).



SuperSOT™-6



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DSS}	Drain-Source Voltage		20	–20	V
V_{GSS}	Gate-Source Voltage		±12	±12	V
I_D	Drain Current – Continuous	(Note 1a)	3.0	–2.2	A
	– Pulsed		12	–6	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.96		W
		(Note 1b)	0.9		
		(Note 1c)	0.7		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.420	FDC6420C	7"	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter		Test Conditions		Min	Typ	Max	Units
Off Characteristics								
BV_{DSS}	Drain–Source Breakdown Voltage		V_{GS} = 0 V, I_D = 250 µA V_{GS} = 0 V, I_D = –250 µA	**Q1** **Q2**	20 –20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient		I_D = 250 µA, Ref. to 25°C I_D = –250 µA, Ref. to 25°C	**Q1** **Q2**		13 –11		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current		V_{DS} = 16 V, V_{GS} = 0 V V_{DS} = –16 V, V_{GS} = 0 V	**Q1** **Q2**			1 –1	µA
I_{GSSF}	Gate–Body Leakage, Forward		V_{GS} = 12 V, V_{DS} = 0 V V_{GS} = 12 V, V_{DS} = 0 V	**Q1** **Q2**			100 100	nA
I_{GSSR}	Gate–Body Leakage, Reverse		V_{GS} = –12 V, V_{DS} = 0 V V_{GS} = –12 V, V_{DS} = 0 V	**Q1** **Q2**			–100 –100	nA
On Characteristics (Note 2)								
$V_{GS(th)}$	Gate Threshold Voltage	**Q1**	V_{DS} = V_{GS}, I_D = 250 µA		0.5	0.9	1.5	V
		Q2	V_{DS} = V_{GS}, I_D = –250 µA		–0.6	–1.0	–1.5	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	**Q1**	I_D = 250 µA, Ref. To 25°C			–3		mV/°C
		Q2	I_D = –250 µA, Ref. to 25°C			–3		
$R_{DS(on)}$	Static Drain–Source On–Resistance	**Q1**	V_{GS} = 4.5 V, I_D = 3.0 A V_{GS} = 2.5 V, I_D = 2.5 A V_{GS} = 4.5 V, I_D = 3.0 A,T_J=125°C			50 66 71	70 95 106	mΩ
		Q2	V_{GS} = –4.5 V, I_D = –2.2 A V_{GS} =– 2.5 V, I_D = –1.8 A V_{GS}= – 4.5 V,I_D=–2.2 A,T_J=125°C			100 145 137	125 190 184	
$I_{D(on)}$	On–State Drain Current	**Q1**	V_{GS} = 4.5 V, V_{DS} = 5 V		12			A
		Q2	V_{GS} = –4.5 V, V_{DS} = –5 V		–6			
g_{FS}	Forward Transconductance	**Q1**	V_{DS} = 5 V I_D = 2.5 A			10		S
		Q2	V_{DS} = –5 V I_D = –2.0A			6		
Dynamic Characteristics								
C_{iss}	Input Capacitance	**Q1**	V_{DS}=10 V, V_{GS}= 0 V, f=1.0MHz			324		pF
		Q2	V_{DS}=–10 V, V_{GS}= 0 V, f=1.0MHz			337		
C_{oss}	Output Capacitance	**Q1**	V_{DS}=10 V, V_{GS}= 0 V, f=1.0MHz			82		pF
		Q2	V_{DS}=–10 V, V_{GS}= 0 V, f=1.0MHz			88		
C_{rss}	Reverse Transfer Capacitance	**Q1**	V_{DS}=10 V, V_{GS}= 0 V, f=1.0MHz			42		pF
		Q2	V_{DS}=–10 V, V_{GS}= 0 V, f=1.0MHz			51		
Switching Characteristics (Note 2)								
$t_{d(on)}$	Turn–On Delay Time	**Q1**	For **Q1**: V_{DS} =10 V, I_{DS}= 1 A V_{GS}= 4.5 V, R_{GEN} = 6 Ω For **Q2**: V_{DS} =–10 V, I_{DS}= –1 A V_{GS}= –4.5 V, R_{GEN} = 6 Ω			5	10	ns
		Q2				9	18	
t_r	Turn–On Rise Time	**Q1**				7	14	ns
		Q2				12	22	
$t_{d(off)}$	Turn–Off Delay Time	**Q1**				13	23	ns
		Q2				10	20	
t_f	Turn–Off Fall Time	**Q1**				1.6	3	ns
		Q2				5	10	
Q_g	Total Gate Charge	**Q1**	For **Q1**: V_{DS} =10 V, I_{DS}= 3.0 A V_{GS}= 4.5 V, For **Q2**: V_{DS} =–10 V, I_{DS}= –2.2 A V_{GS}= –4.5 V,			3.3	4.6	nC
		Q2				3.7		
Q_{gs}	Gate–Source Charge	**Q1**				0.95		nC
		Q2				0.68		
Q_{gd}	Gate–Drain Charge	**Q1**				0.7		nC
		Q2				1.3		

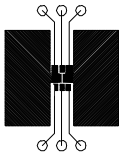
Electrical Characteristics

T_A = 25°C unless otherwise noted

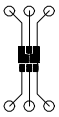
Symbol	Parameter		Test Conditions		Min	Typ	Max	Units
Drain–Source Diode Characteristics and Maximum Ratings								
I_S	Maximum Continuous Drain–Source Diode Forward Current			**Q1**			0.8	A
				Q2			–0.8	
V_{SD}	Drain–Source Diode Forward Voltage	**Q1**	V_{GS} = 0 V, I_S = 0.8 A (Note 2)			0.7	1.2	V
		Q2	V_{GS} = 0 V, I_S = 0.8 A (Note 2)			–0.8	–1.2	

Notes:

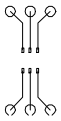
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 130 °C/W when mounted on a 0.125 in^2 pad of 2 oz. copper.



b) 140 °C/W when mounted on a .004 in^2 pad of 2 oz copper



c) 180 C°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Typical Characteristics: N-Channel

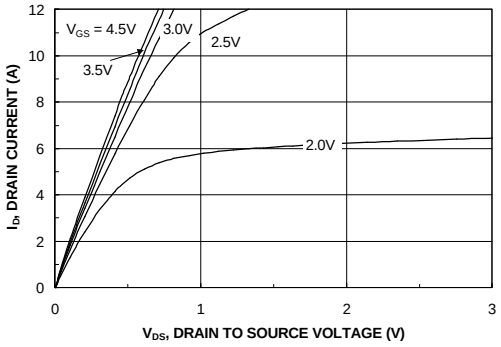


Figure 1. On-Region Characteristics.

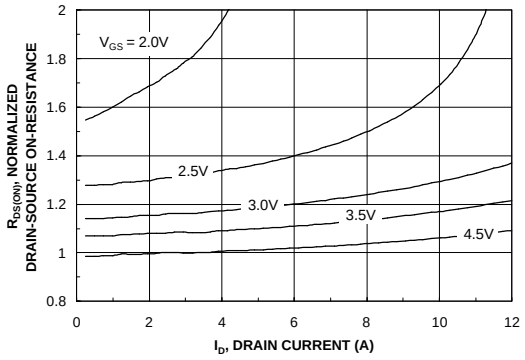


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

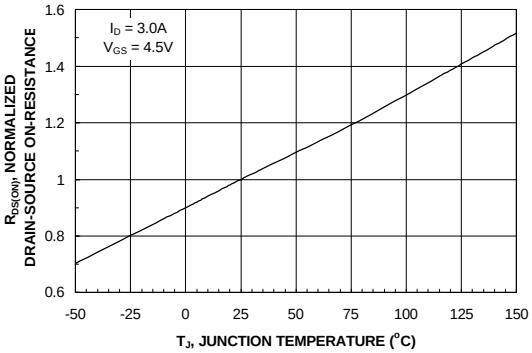


Figure 3. On-Resistance Variation with Temperature.

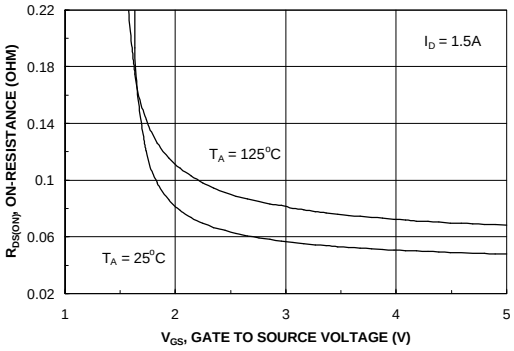


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

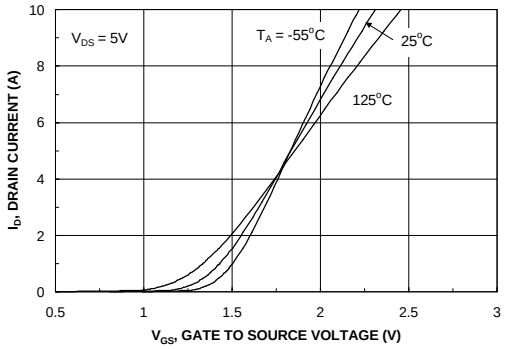


Figure 5. Transfer Characteristics.

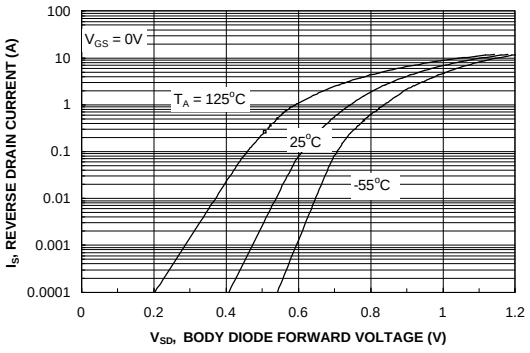


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

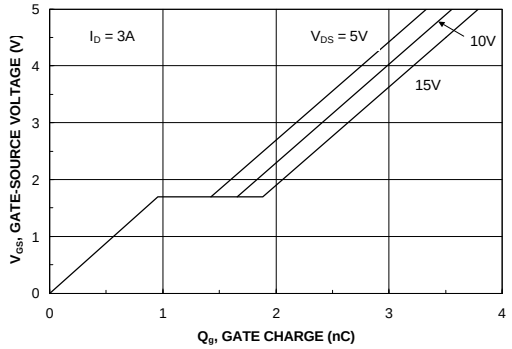


Figure 7. Gate Charge Characteristics.

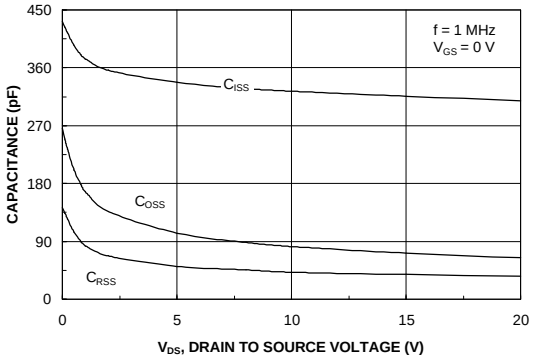


Figure 8. Capacitance Characteristics.

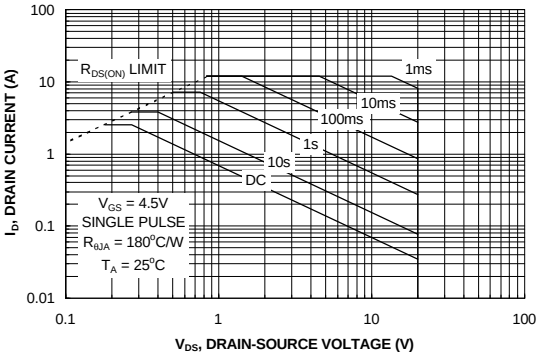


Figure 9. Maximum Safe Operating Area.

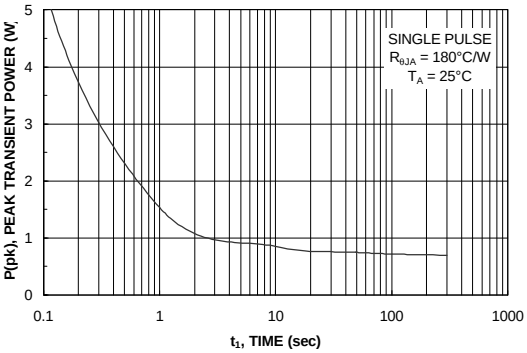


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: P-Channel

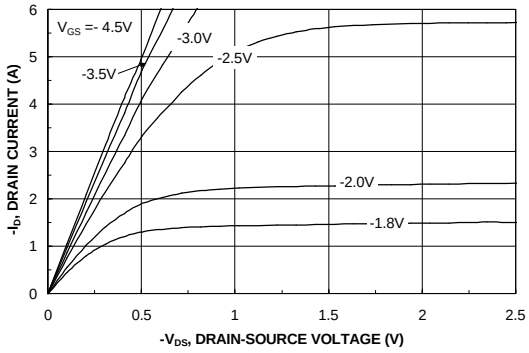


Figure 11. On-Region Characteristics.

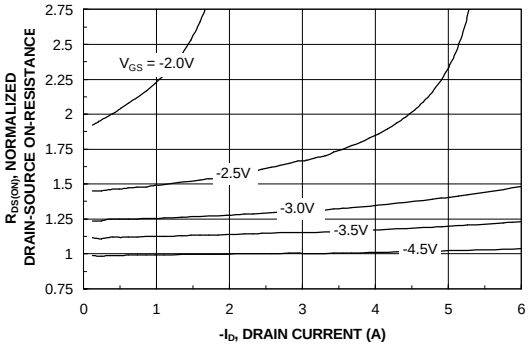


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

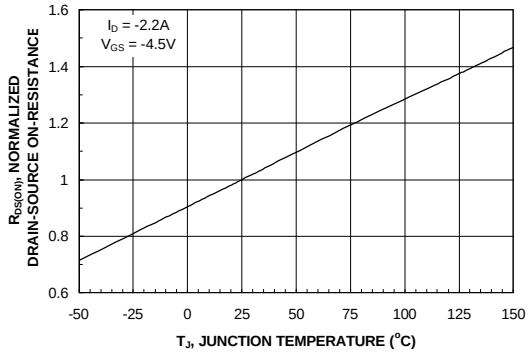


Figure 13. On-Resistance Variation with Temperature.

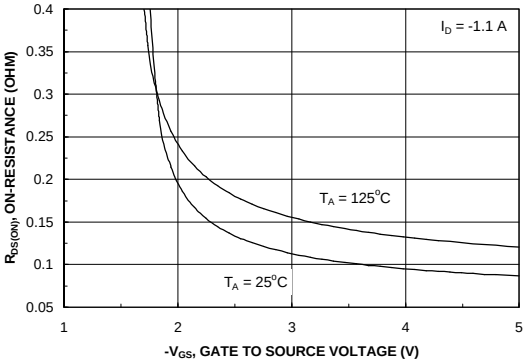


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

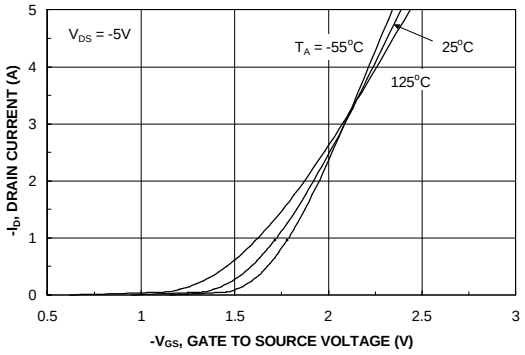


Figure 15. Transfer Characteristics.

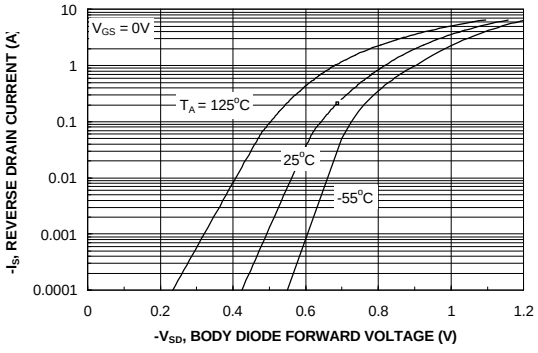


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

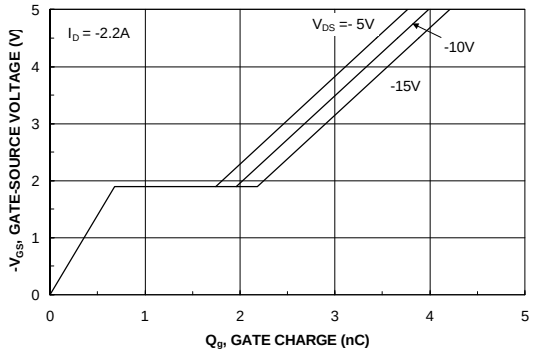


Figure 17. Gate Charge Characteristics.

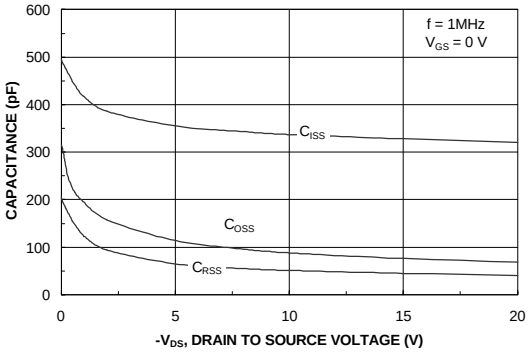


Figure 18. Capacitance Characteristics.

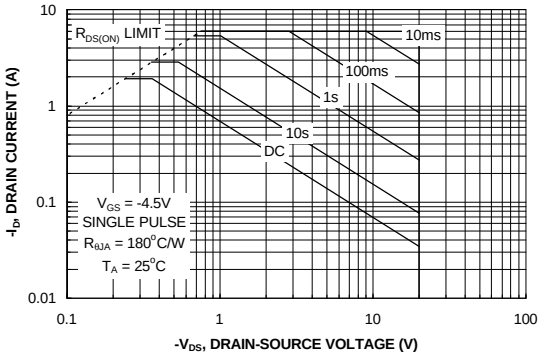


Figure 19. Maximum Safe Operating Area.

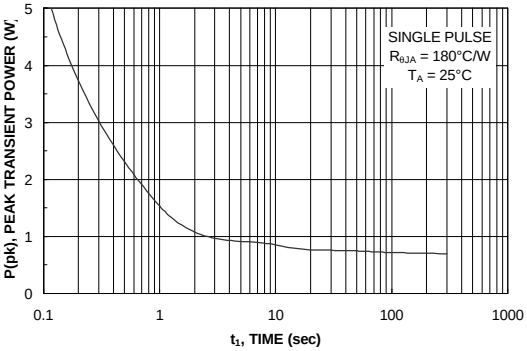


Figure 20. Single Pulse Maximum Power Dissipation.

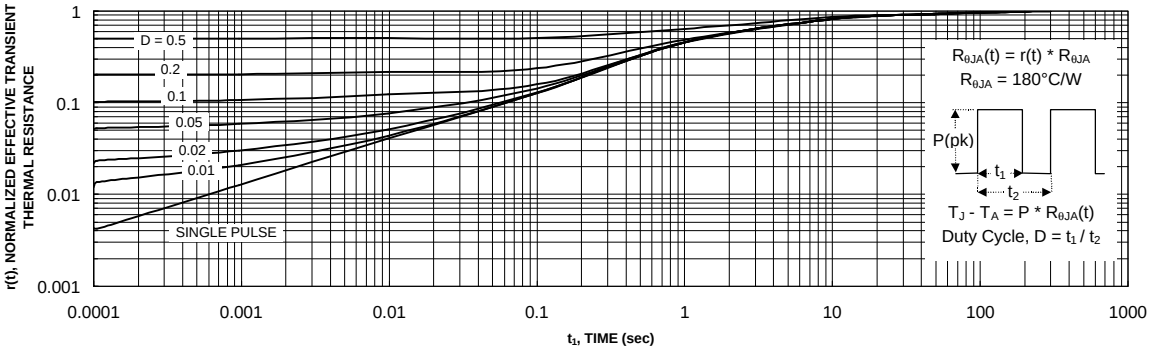


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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