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FAN2564

300mA Low V_{IN} LDO for Digital Applications

Features

- Input Voltage 1.65V to 3.6V
- Guaranteed 300mA Output
- High Initial Output Voltage Accuracy: $\pm 1\%$
- Fixed Output Voltage options from 1.2V to 2.8V
- Very Low Dropout: 100mV at 300mA
- 45 μ A Quiescent Current at No Load
- Low Output Noise of 100 μ V_{RMS}
- Inrush Current Controlled to Less Than 500mA
- PSRR of 60dB at 1kHz
- 100 μ s Startup Time
- Stable with Ceramic Capacitors
- Thermal and Short-Circuit Protection
- 4-bump WLCSP, 0.5mm Pitch
- 6-pin 2 x 2mm UMLP

Description

The FAN2564 operates from a minimum input of 1.65V and provides outputs as low as 1.2V. Output current is guaranteed to 300mA, making this regulator ideal for digital loads.

The unique low input voltage capability and very low dropout make this device an ideal post regulator to a synchronous buck regulator. In this configuration, accurate low voltage regulation is provided without the inefficiencies typically related to linear regulators.

The enable pin can be used to initiate shutdown mode, where the operating current falls to an extremely low 10nA, typically.

The FAN2564 is designed to be stable with space-saving ceramic capacitors as small as 0402 case size.

The FAN2564 is available in 4-bump 0.5mm pitch wafer-level chip-scale package (WLCSP) and a 6-lead 2 x 2mm ultra-thin molded leadless package (UMLP).

Applications

- Post Regulator
- Cell Phones and Smart Phones
- WLAN, 3G, and 4G Data Cards
- PMP and MP3 Players

Typical Application Circuit

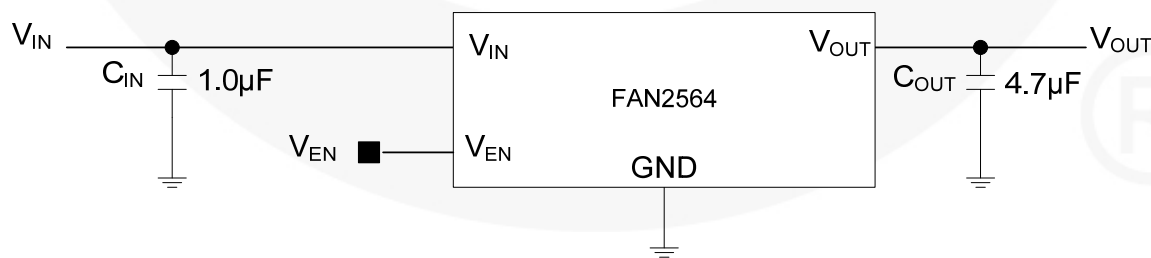


Figure 1. Typical Application Circuit

Ordering Information

Part Number	Output Voltage ⁽¹⁾	Temperature Range	Package	Packing Method
FAN2564UC12X	1.2	-40 to 85°C	WLCSP-4 0.5mm Pitch	Tape and Reel
FAN2564UC13X	1.3			
FAN2564UC15X	1.5			
FAN2564UC18X	1.8			
FAN2564UC25X	2.5			
FAN2564UMP12X	1.2	-40 to 85°C	6 Lead UMLP 2 x 2mm	Tape and Reel
FAN2564UMP13X	1.3			
FAN2564UMP15X	1.5			
FAN2564UMP18X	1.8			

Notes:

- Other voltage options available upon request. Contact a Fairchild representative.

Block Diagram

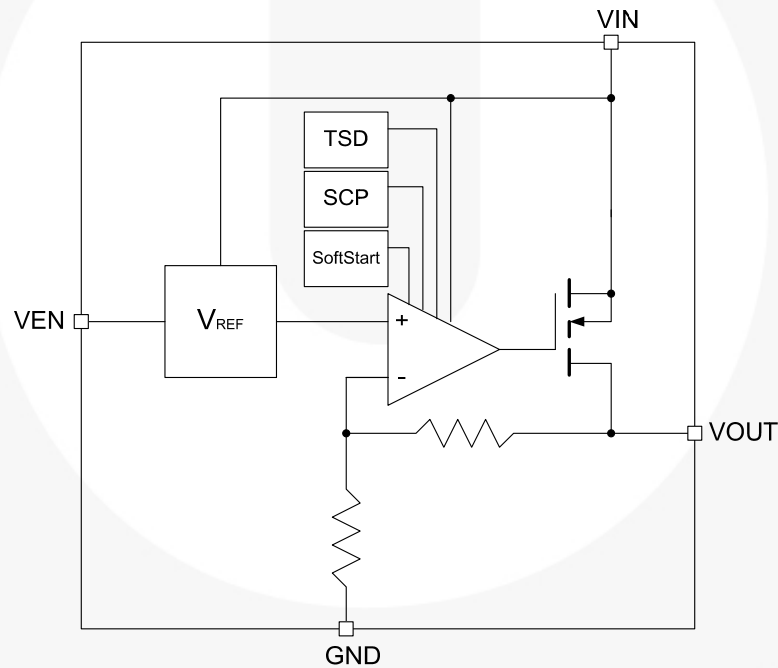


Figure 2. Block Diagram

Pin Configuration

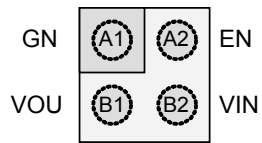


Figure 3. WLCSP Bumps Facing Down

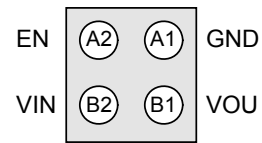


Figure 4. WLCSP, Bumps Facing Up

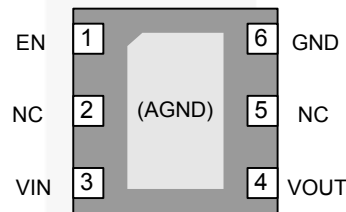


Figure 5. UMLP, Leads Facing Down

Pin Definitions

Pin #		Name	Description
WLCSP	UMLP		
A1	6	GND	Ground. Power and IC ground. All signals are referenced to this pin.
B1	4	VOUT	V_{OUT}. Connect to output voltage.
B2	3	VIN	Input Voltage. Connect to input power source.
A2	1	EN	Enable. The device is in shutdown mode when voltage to this pin is <0.4V and enabled when >0.95V.
	5	NC	No connect.
	2	NC	No connect.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Input Voltage with Respect to GND	-0.3	4.5	V
	Voltage on Any Other Pin with Respect to GND	-0.3	V_{IN}	V
T_J	Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-65	+150	°C
T_L	Lead Temperature (Soldering 10 Seconds)		+260	°C
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	4	kV
		Charged Device Model per JESD22-C101	2	
		Machine Model per JESD22-A115	200	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range	1.8		3.6	V
I_{OUT}	Output Current	0		300	mA
C_{IN}	Input Capacitor		1.0		μ F
C_{OUT}	Output Capacitor	1.0	4.7	10.0	μ F
T_A	Operating Ambient Temperature	-40		+85	°C
T_J	Operating Junction Temperature	-40		+125	°C

Thermal Properties

Symbol	Parameter	Min.	Typ.	Max.	Units
Θ_{JA}	Junction-to-Ambient Thermal Resistance ⁽²⁾	WLSCP	200		°C/W
		UMLP	49		°C/W

Note:

- Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JESD51- JEDEC standard. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A .

Electrical Characteristics

$V_{IN}^{(3)} = V_{OUT} + 0.5V$ or $1.8V$ (whichever is higher). $T_A = -40^{\circ}C$ to $+85^{\circ}C$, test circuit is Figure 1, typical values are at $T_A = 25^{\circ}C$, $I_{LOAD} = 1mA$, $V_{EN} = V_{IN}$, unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Power Supplies							
V _{IN}	Input Voltage Range			1.65		3.60	V
I _{GND}	Ground Current	I _{LOAD} =0mA			45	75	μA
		I _{LOAD} =300mA			140	200	μA
I _{SD}	Shutdown Supply Current	V _{IN} =3.6V, EN=GND			0.01	1.00	μA
V _(EN)	Enable High-level Input Voltage			0.95			V
	Enable Low-level Input Voltage					0.4	
I _(EN)	Enable Input Leakage Current	EN=GND			0		
		EN=V _{IN} =3.6V			2.5	4.0	μA
Regulation							
I _{OUT}	Minimum Output Current			0			mA
I _{OUT}	Maximum Output Current			300			mA
V _{DO}	Dropout Voltage ⁽⁴⁾	I _{LOAD} =300mA			100	160	mV
ΔV _{OUT}	Output Voltage Accuracy	1.8V, 2.5V	Over Full V _{IN} , I _{OUT} , at Room Temperature	-1.0		1.0	%
		1.2V, 1.3V, 1.5V		-1.5		1.5	
		1.2V, 1.3V, 1.5V, 1.8V, 2.5V	Over Full V _{IN} , I _{OUT} , Tempera- ture Range	-2.5		2.5	
ΔV _{OUTline}	Line Regulation	V _{IN} =V _{OUT(NOM)} + 0.5V to 3.6V, I _{OUT} =1mA			0.03	0.50	%/V
ΔV _{OUTload}	Load Regulation	I _{OUT} =1mA to 300mA			10	60	μV/mA
I _{SCP}	Short-circuit Current Limit				500	900	mA
I _{SU}	Start-up Peak Current	EN Transition, LOW to HIGH			500	900	mA
t _{ON}	Turn-on Time ⁽⁵⁾	EN Transition, LOW to HIGH			100		μs
	Startup Overshoot ⁽⁵⁾	I _{OUT} =1mA			0		%
TSD	Thermal Shutdown	Rising Temperature			+160		°C
		Hysteresis			+30		°C
PSRR	Power Supply Rejection Ratio ⁽⁵⁾	f=1kHz			60		dB
e _n	Output Noise Voltage ⁽⁵⁾	10Hz to 100kHz			100		μV _{RMS}
Timing Characteristics							
Peak ΔV _{OUTline}	Line Transient Response ⁽⁵⁾	600mV, t _{RISE} =t _{FALL} =30μs			±6		mV
Peak ΔV _{OUTload}	Load Transient Response ⁽⁵⁾	1mA-300mA-1mA, t _{RISE} =t _{FALL} =1μs			±50		mV

Note:

- V_{IN} voltage tolerance $\pm 5\%$.
- Dropout voltage is the minimum input to output differential voltage needed to maintain V_{OUT} to within 5% of nominal value. This parameter is only specified for output voltages greater than or equal to 1.8V.
- This electrical specification is guaranteed by design.

Typical Performance Characteristics

Unless otherwise noted, $V_{IN}=V_{OUT(Nominal)}+0.5V$ or $1.8V$ (whichever is greater), $V_{OUT}=1.2V$, $C_{IN}=1\mu F$, $C_{OUT}=4.7\mu F$, and $T_A=25^\circ C$.

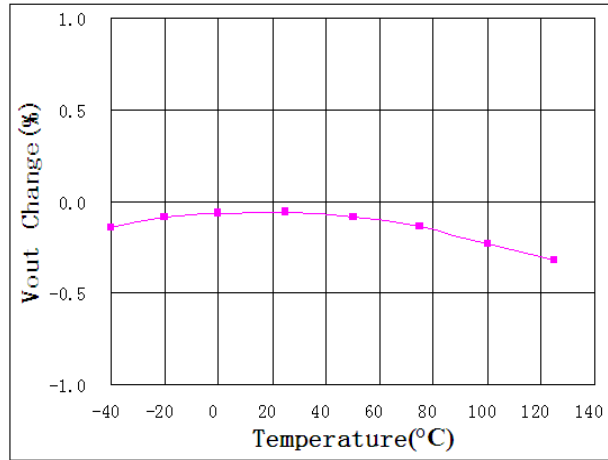


Figure 6. Output Voltage Change vs. Temperature

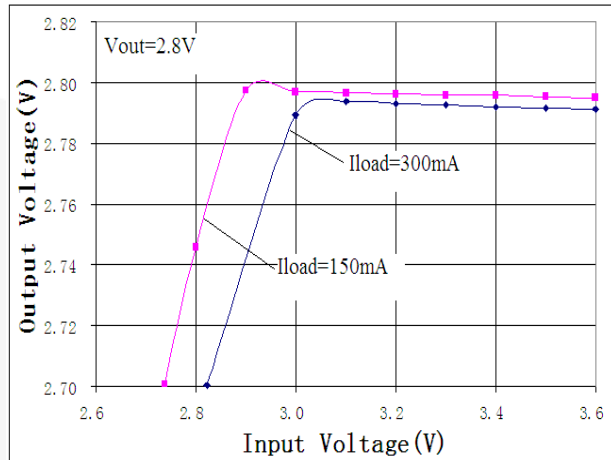


Figure 7. Output Voltage vs. Minimum Input Voltage

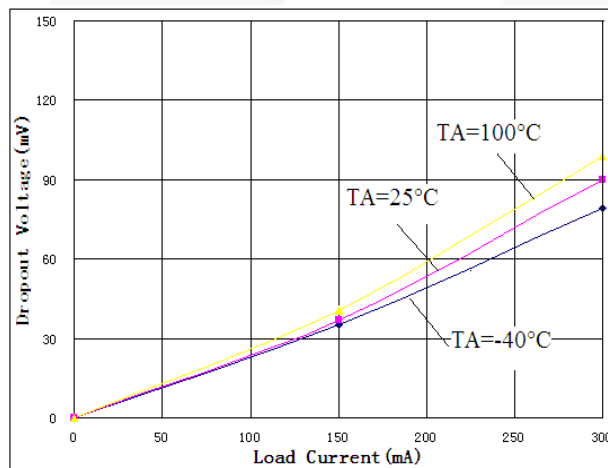


Figure 8. Dropout Voltage

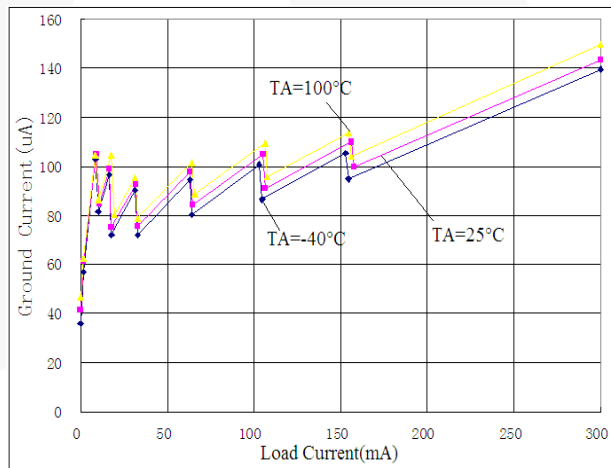


Figure 9. Ground Current vs. Load Current

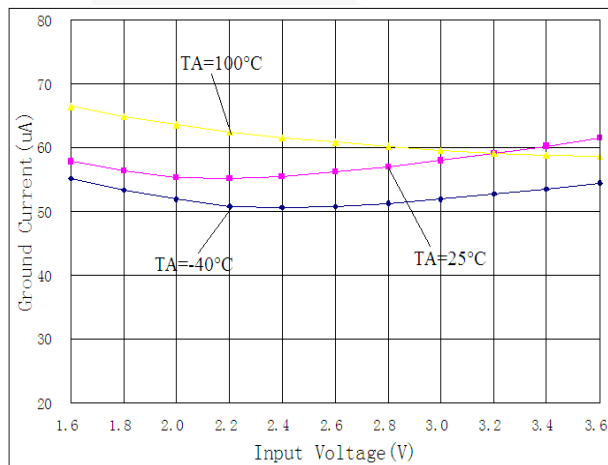


Figure 10. Ground Current vs. V_{IN} , $I_{LOAD}=1mA$

Typical Performance Characteristics

Unless otherwise noted, $V_{IN}=V_{OUT(Nominal)}+0.5V$ or $1.8V$ (whichever is greater), $V_{OUT}=1.2V$, $C_{IN}=1\mu F$, $C_{OUT}=4.7\mu F$, and $T_A=25^\circ C$.

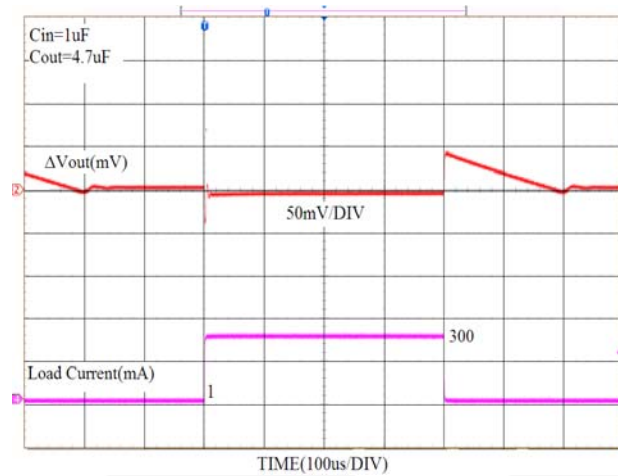


Figure 11. Load Transient, $V_{OUT}=1.2V$

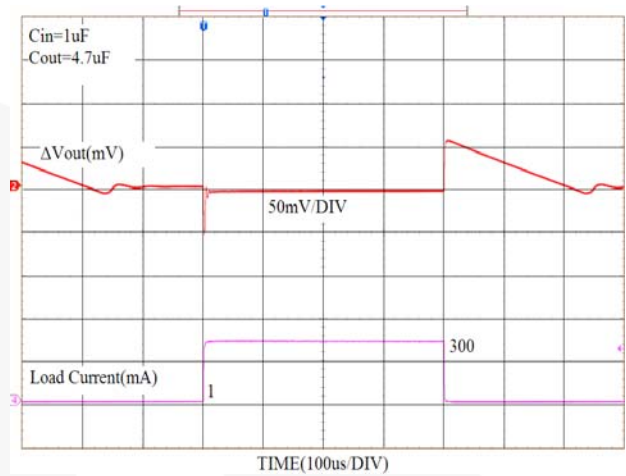


Figure 12. Load Transient, $V_{OUT}=2.8V$

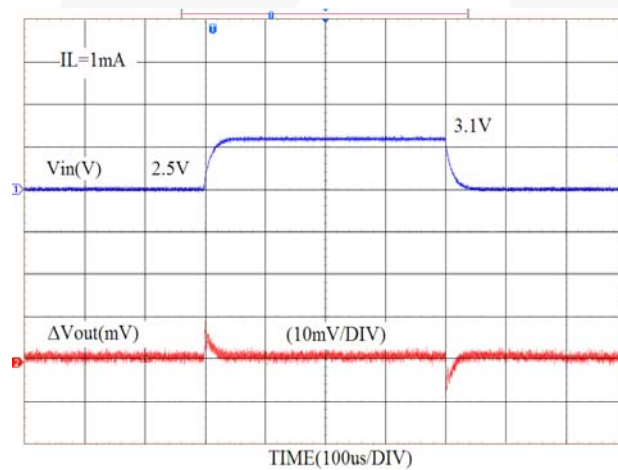


Figure 13. Line Transient, $I_{LOAD}=1mA$

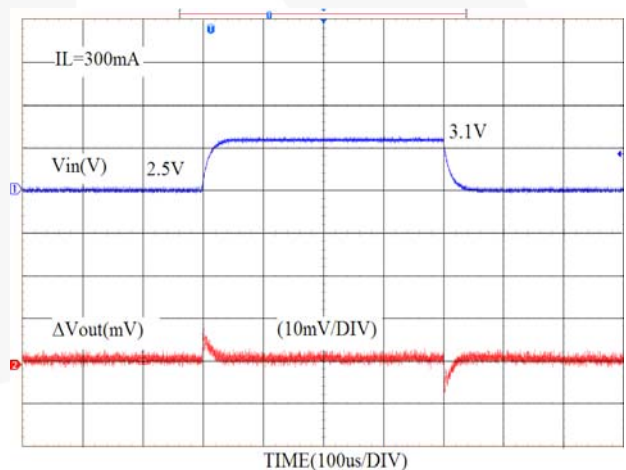


Figure 14. Line Transient, $I_{LOAD}=300mA$

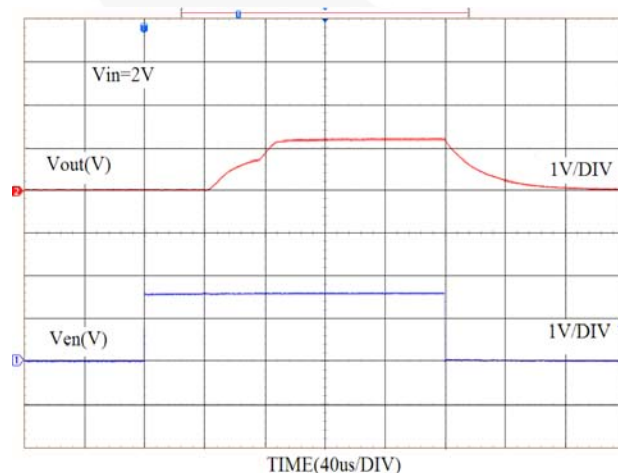


Figure 15. Enable Characteristics

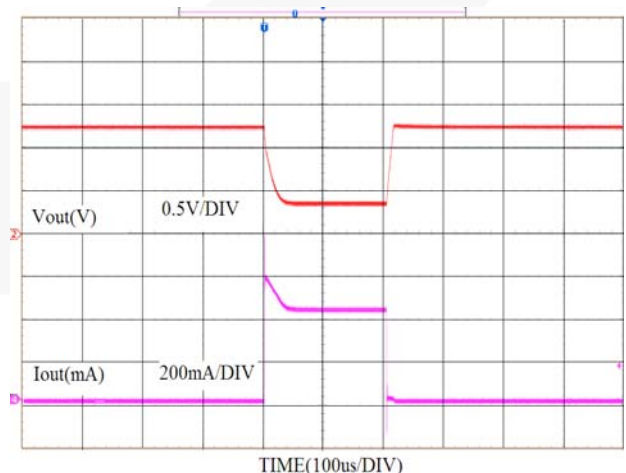


Figure 16. Short Circuit Current

Typical Performance Characteristics

Unless otherwise noted, $V_{IN}=V_{OUT(Nominal)}+0.5V$ or $1.8V$ (whichever is greater), $V_{OUT}=1.2V$, $C_{IN}=1\mu F$, $C_{OUT}=4.7\mu F$, and $T_A=25^\circ C$.

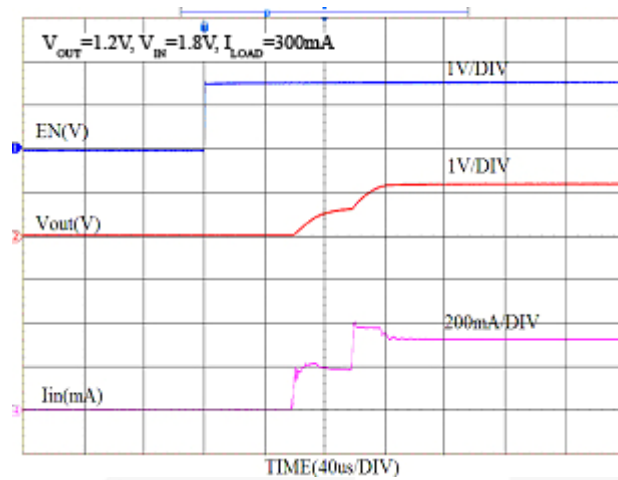


Figure 17. Inrush Current

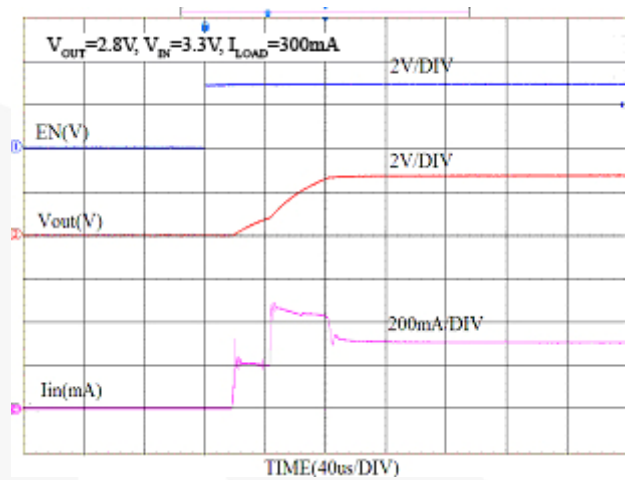


Figure 18. Inrush Current

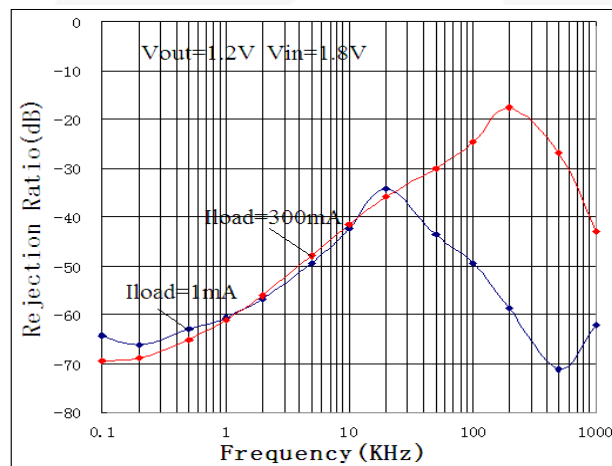


Figure 19. Power Supply Rejection Ratio

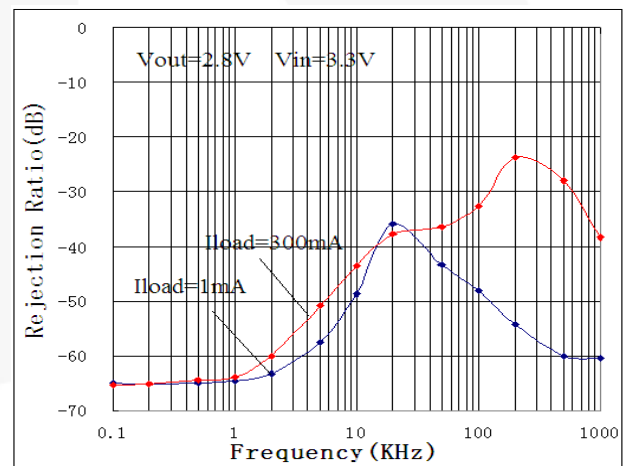


Figure 20. Power Supply Rejection Ratio

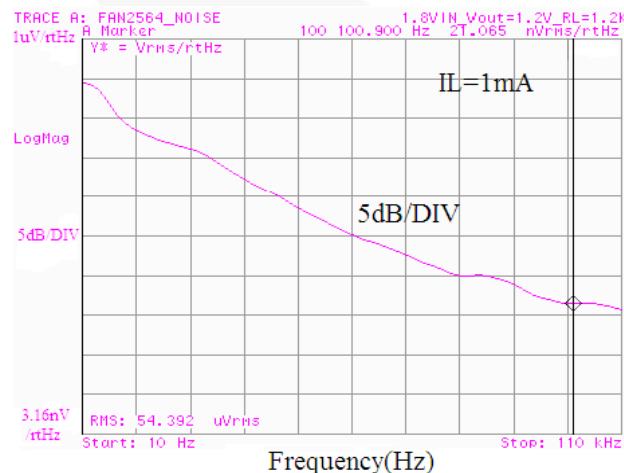


Figure 21. Noise Density

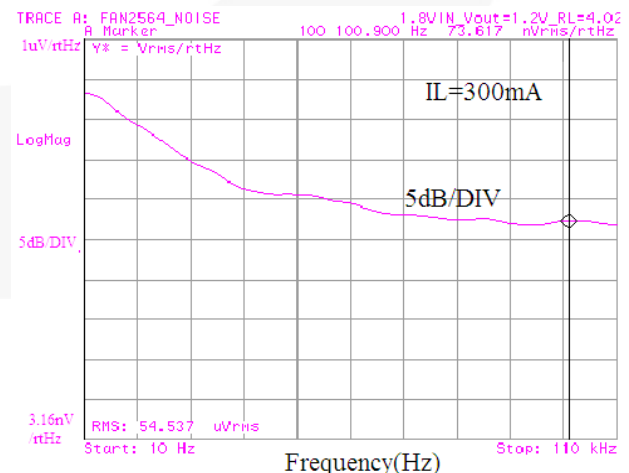


Figure 22. Noise Density

Application Information

Enable and Soft Start

A 1.4 M Ω pull-down resistor ensures the EN pin to be in LOW state when it is floating. The chip is in shut-down mode when EN pin is LOW.

To enable the chip, the EN pin needs to be raised higher than 0.95V. The output pin starts to charge up to the final voltage. On-chip soft-start circuitry limits the peak inrush current through VIN pin to less than the specified typical value of 500mA, regardless of C_{OUT} value and load conditions.

The startup time increases as V_{OUT}, C_{OUT}, and load increases, but meets the specified 100 μ s under the worst load and V_{OUT} conditions.

Short-Circuit and Thermal Protection

The output current is short-circuit protected. When a short-circuit fault occurs, the output current is automatically limited and V_{OUT} drops, depending on the actual short-circuit resistance.

Short-circuit fault or output overload may cause the die temperature to increase and exceed maximum ratings due to power dissipation. In such cases, depending upon the ambient temperature; V_{IN}, load current, and the junction-to-air thermal resistance (θ_{JA}) of the die; the device may enter thermal shutdown.

When the die temperature exceeds the shutdown limit temperature, the onboard thermal protection disables the output until the temperature drops below its hysteresis value, at which point the output is re-enabled and a new soft-start sequence occurs as described above.

Thermal Considerations

For best performance, the die temperature and the power dissipated should be kept at moderate values. The maximum power dissipated can be evaluated based on the following relationship:

$$P_{D(max)} = \left\{ \frac{T_{J(max)} - T_A}{\theta_{JA}} \right\} \quad (1)$$

where T_{J(max)} is the maximum allowable junction temperature of the die and T_A is the ambient operating temperature. θ_{JA} is dependent on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground.

The addition of backside copper with through-holes, stiffeners, and other enhancements can also aid in reducing θ_{JA} . The heat contributed by the dissipation of other devices located nearby must be included in design considerations.

Capacitors Selection

The FAN2564 is stable with a wide range of capacitor values and sizes.

For loop stability, a 1 μ F input capacitor or bigger is recommended. Tolerance, temperature, and voltage coefficients of the capacitor must be considered to ensure effective capacitance stays around 1 μ F or above. There is no special requirement on its ESR value.

An output capacitor with an effective capacitance between 1 μ F and 10 μ F is required for loop stability. The ESR value should be within 5 to 100m Ω . 2.2 μ F or 4.7 μ F ceramic capacitors are recommended to ensure stability over the full temperature, input, and output voltage range of operation, such as those listed in Table 1.

Table 1. Recommended Capacitors

Capacitance	Size	Vendor	Part Number
1 μ F	0603	MURATA	GRM188R71C105KA120
2.2 μ F	0603	MURATA	GRM188R61A225KF340
2.2 μ F	0402	MURATA	GRM155R60J225ME15
4.7 μ F	0603	MURATA	GRM188C80G475KE19
4.7 μ F	0402	MURATA	GRM155R60G475M

Layout Considerations

C_{IN} and C_{OUT} should be placed close to the device for optimal transient response and device behavior. A dedicated ground plane is recommended for proper GND connection.

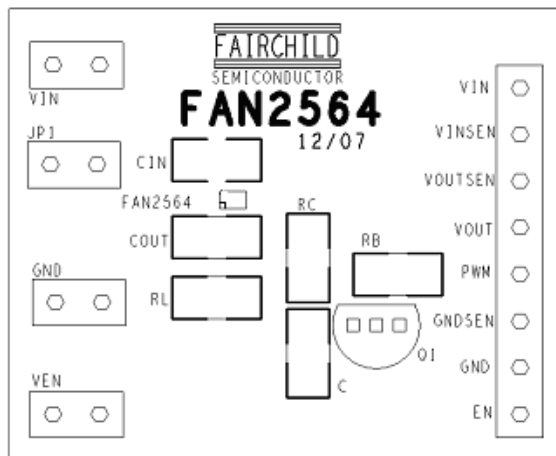


Figure 23. Assembly Diagram

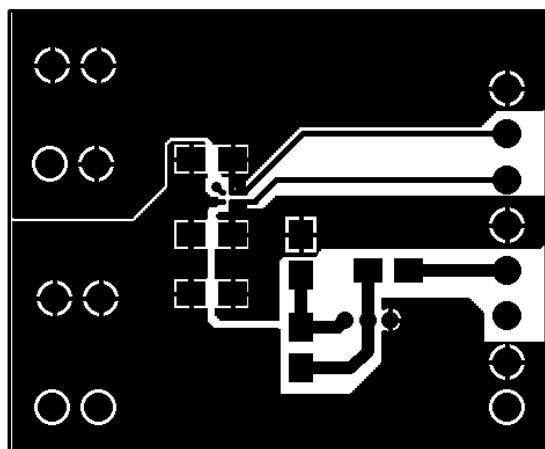


Figure 24. Top Layer

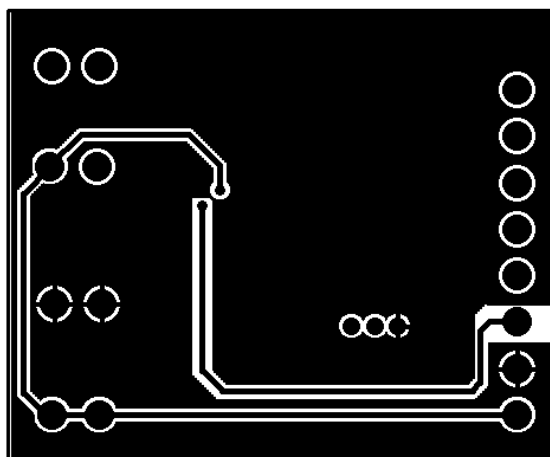


Figure 25. Bottom Layer

Physical Dimensions

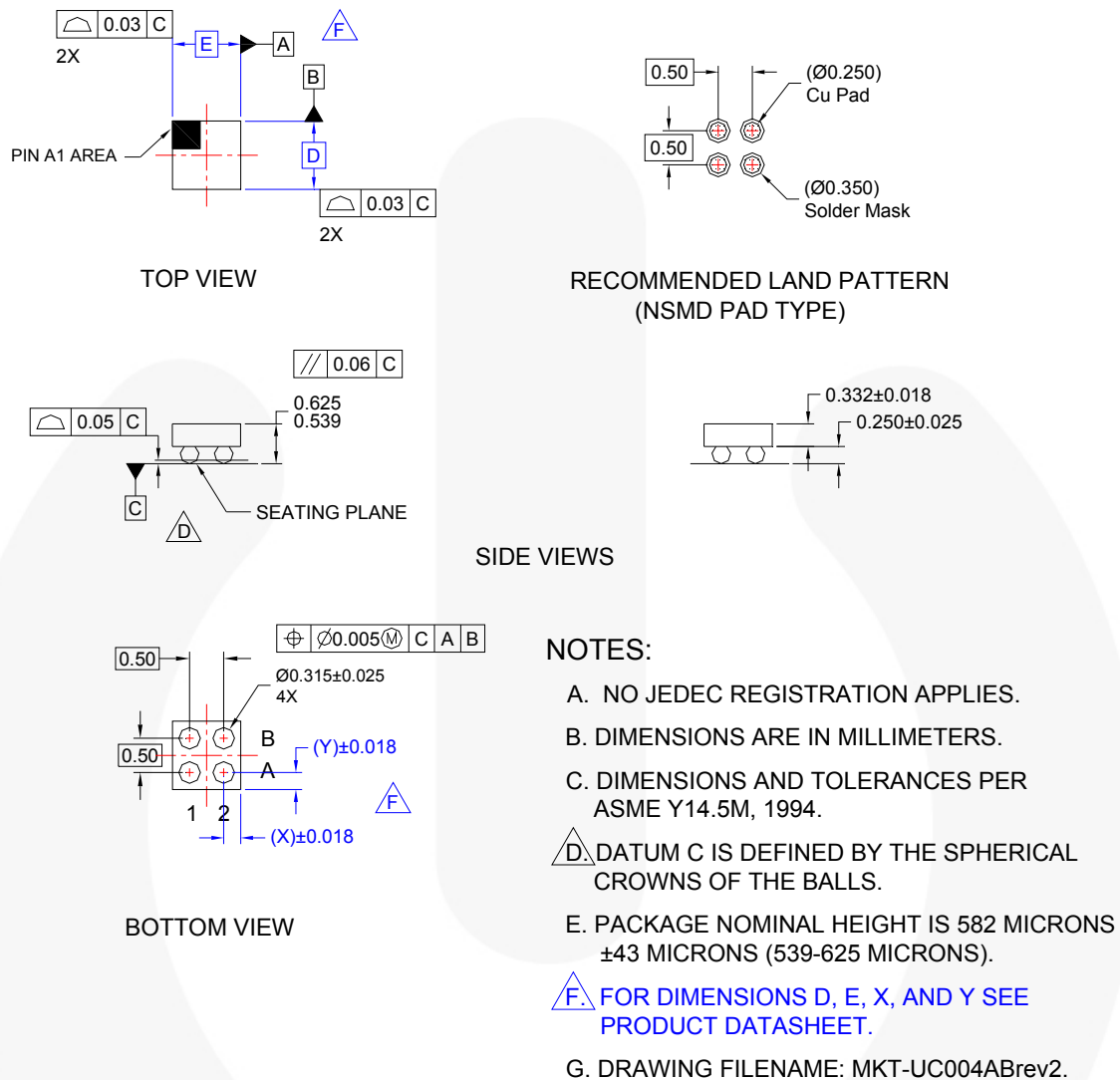


Figure 26. 4-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.5mm Pitch

Product Specific Dimensions

Product	D	E	X	Y
FAN2564UCX	1.41 ± 0.030	0.93 ± 0.030	0.215	0.455

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Physical Dimensions

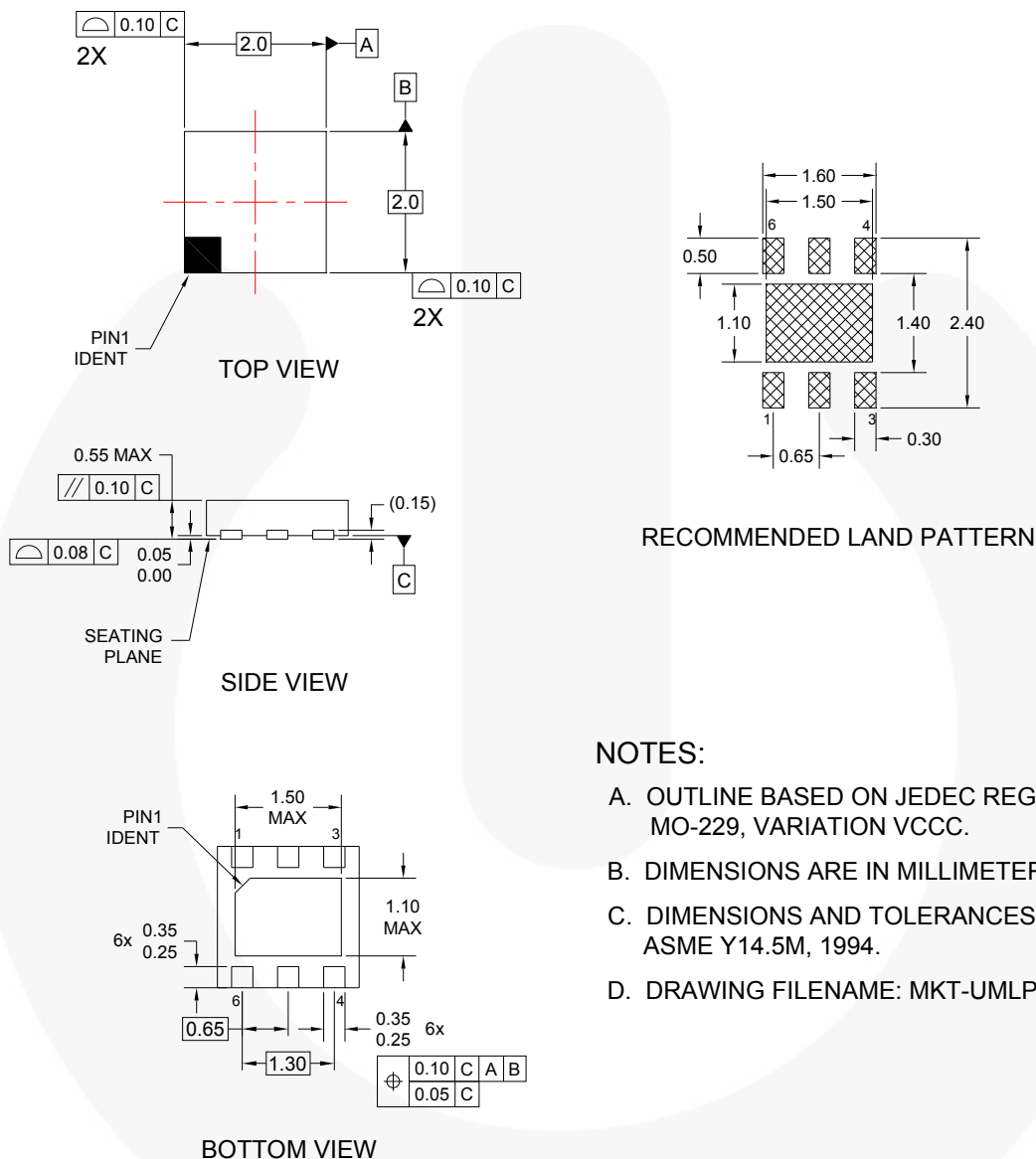


Figure 27. 6-Pin, Ultrathin Molded Leadless Package (UMLP)

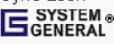
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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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