

NVD5C684NL

Product Preview

Power MOSFET

60 V, 17.5 mΩ, 38 A, Single N-Channel

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage			V_{GS}	± 16	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	Steady State	$T_C = 25^{\circ}\text{C}$	I_D	38	A
		$T_C = 100^{\circ}\text{C}$		27	
Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 25^{\circ}\text{C}$	P_D	27	W
		$T_C = 100^{\circ}\text{C}$		13	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	13	A
		$T_A = 100^{\circ}\text{C}$		9.0	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		$T_A = 25^{\circ}\text{C}$	P_D	3.0	W
		$T_A = 100^{\circ}\text{C}$		1.5	
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$	I_{DM}	130	A	
Operating Junction and Storage Temperature			T_J , T_{stg}	-55 to 175	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	TBD	A
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^{\circ}\text{C}$, $V_{GS} = 10\text{ V}$, $I_{L(pk)} = \text{TBD A}$, $L = 0.1\text{ mH}$)			E_{AS}	TBD	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	5.6	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	50	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

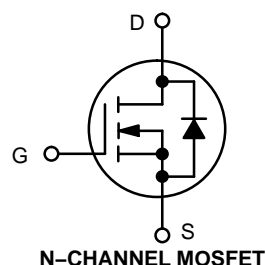
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



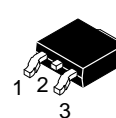
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
60 V	17.5 mΩ @ 10 V	38 A
	24.5 mΩ @ 4.5 V	

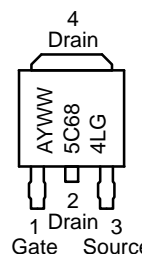


N-CHANNEL MOSFET



DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location
Y = Year
WW = Work Week
5C684L = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NVD5C684NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			TBD		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 60 V	T _J = 25°C		1.0	μA
			T _J = 125°C		250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 16 V			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.2		2.1	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			TBD		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A		14	17.5	mΩ
		V _{GS} = 4.5 V, I _D = 10 A		19.6	24.5	
Forward Transconductance	g _{FS}	V _{DS} = TBD V, I _D = 10 A		TBD		S

CHARGES, CAPACITANCES AND GATE RESISTANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		700		pF
Output Capacitance	C _{oss}			300		
Reverse Transfer Capacitance	C _{rss}			3.0		
Total Gate Charge	Q _{G(TOT)}	V _{DS} = 48 V, I _D = 10 A	V _{GS} = 4.5 V	4.0		nC
			V _{GS} = 10 V	9.0		
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 10 A		TBD		nC
Gate-to-Source Charge	Q _{GS}			2.0		
Gate-to-Drain Charge	Q _{GD}			1.0		
Plateau Voltage	V _{GP}			TBD		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 10 A, R _G = 2.5 Ω		TBD		ns
Rise Time	t _r			TBD		
Turn-Off Delay Time	t _{d(off)}			TBD		
Fall Time	t _f			TBD		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 10 A	T _J = 25°C		TBD	TBD	V
			T _J = 125°C		TBD		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 10 A			TBD		ns
Charge Time	t _a				TBD		
Discharge Time	t _b				TBD		
Reverse Recovery Charge	Q _{RR}				TBD		nC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Order Number	Package	Shipping [†]
NVD5C684NLT4G	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

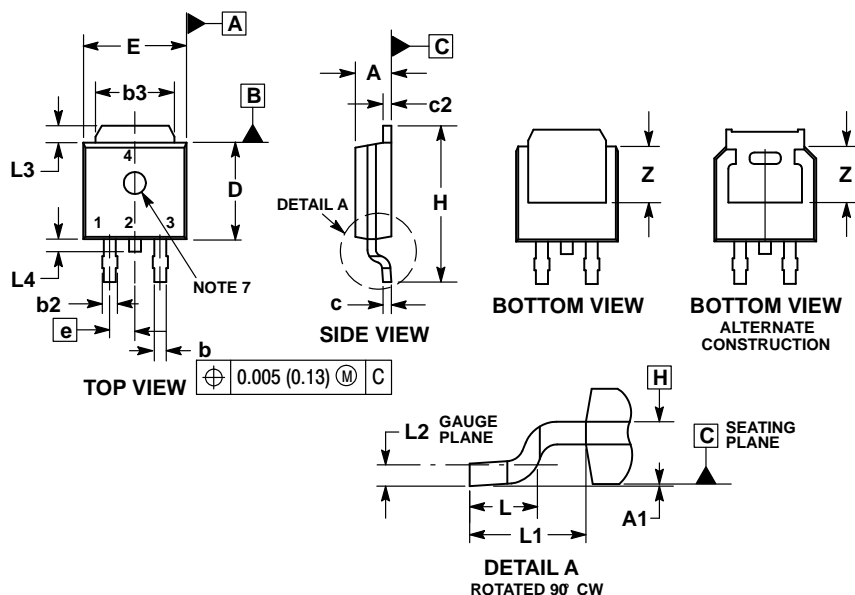
NVD5C684NL

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)

CASE 369C

ISSUE E

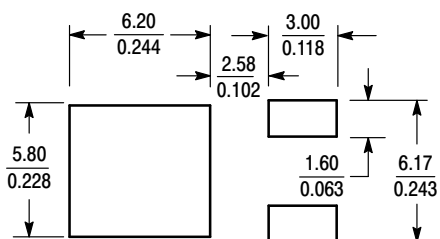


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*




SCALE 3:1 (mm/inches)

STYLE 2:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

NVD5C684NL/D