

# MC10EP35, MC100EP35

## 3.3 V / 5 V ECL JK Flip-Flop

### Description

The MC10/100EP35 is a higher speed/low voltage version of the EL35 JK flip-flop. The J/K data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

The 100 Series contains temperature compensation.

### Features

- 410 ps Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:
  - ♦  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:
  - ♦  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



**ON Semiconductor®**

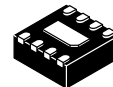
[www.onsemi.com](http://www.onsemi.com)



**SOIC-8 NB  
D SUFFIX  
CASE  
751-07**

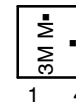
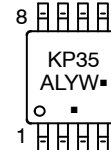
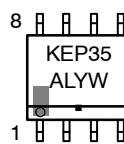
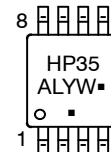
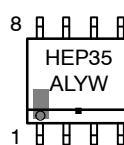


**TSSOP-8  
DT SUFFIX  
CASE  
948R-02**



**DFN-8  
MN SUFFIX  
CASE 506AA**

### MARKING DIAGRAMS\*



H = MC10	A = Assembly Location
K = MC100	L = Wafer Lot
5R = MC10	Y = Year
3M = MC100	W = Work Week
	M = Date Code
	▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

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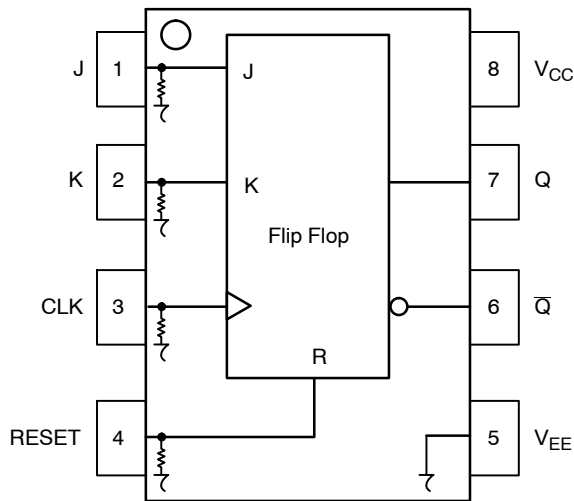


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK*	ECL Clock Inputs
J*, K*	ECL Signal Inputs
RESET*	ECL Asynchronous Reset
Q, $\bar{Q}$	ECL Data Outputs
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply
EP	(DFN-8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

\* Pins will default LOW when left open.

Table 2. TRUTH TABLE

J	K	RESET	CLK	Q <sub>n+1</sub>
L-	L-	L	Z	Q <sub>n</sub>
L-	H	L	Z	L
H-	L	L	Z	H
H-	H	L	Z	$\bar{Q}_n$
X	X	H	X	L

Z = LOW to HIGH Transition

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC-8 NB TSSOP-8 DFN-8	Level 1 Level 3 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL-94 V-0 @ 0.125 in
Transistor Count	77 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

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**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-6	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V
$I_{out}$	Output Current	Continuous Surge		50 100	mA
$T_A$	Operating Temperature Range			-40 to +85	°C
$T_{stg}$	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 NB	190 130	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8 NB	41 to 44	°C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8	185 140	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	°C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN-8	129 84	°C/W
$T_{sol}$	Wave Solder (Pb-Free)	<2 to 3 sec @ 260°C		265	°C
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	(Note 1)	DFN-8	35 to 40	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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**Table 5. 10EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	30	40	50	30	40	50	30	40	50	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
$V_{OL}$	Output LOW Voltage (Note 2)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1365		1690	1460		1755	1490		1815	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
2. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 6. 10EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	30	40	50	30	40	50	30	40	50	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
$V_{OL}$	Output LOW Voltage (Note 2)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.
2. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 7. 10EP DC CHARACTERISTICS, NECL** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	30	40	50	30	40	50	30	40	50	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

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**Table 8. 100EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	30	40	50	30	40	50	30	40	50	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 2)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
2. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 9. 100EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	30	40	50	30	40	50	30	40	50	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
$V_{OL}$	Output LOW Voltage (Note 2)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.
2. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 10. 100EP DC CHARACTERISTICS, NECL** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	30	40	50	30	40	50	30	40	50	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

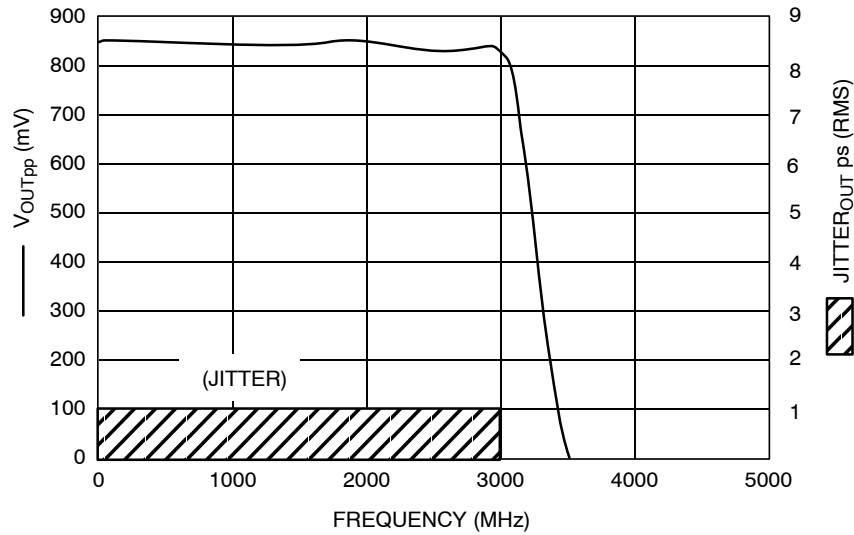
# MC10EP35, MC100EP35

**Table 11. AC CHARACTERISTICS** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Frequency (See Figure 2. $F_{\max}/\text{JITTER}$ )		> 3			> 3			> 3		GHz
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Propagation Delay to Output Differential R, CLK to Q, $\bar{Q}$	200	400	480	200	410	490	200	420	575	ps
$t_{\text{RR}}$	Reset Recovery	150	80		150	90		150	100		ps
$t_{\text{S}}$ $t_{\text{H}}$	Setup Time Hold Time	150	50		150	50		150	80		ps
$t_{\text{PW}}$	Minimum Pulse width RESET	550	400		550	400		550	400		ps
$t_{\text{JITTER}}$	Cycle-to-Cycle Jitter (See Figure 2. $F_{\max}/\text{JITTER}$ )		0.2	< 1		0.2	< 1		0.2	< 1	ps
$t_{\text{r}}$ $t_{\text{f}}$	Output Rise/Fall Times Q, $\bar{Q}$ (20% – 80%)	70	120	170	80	130	180	100	150	200	ps

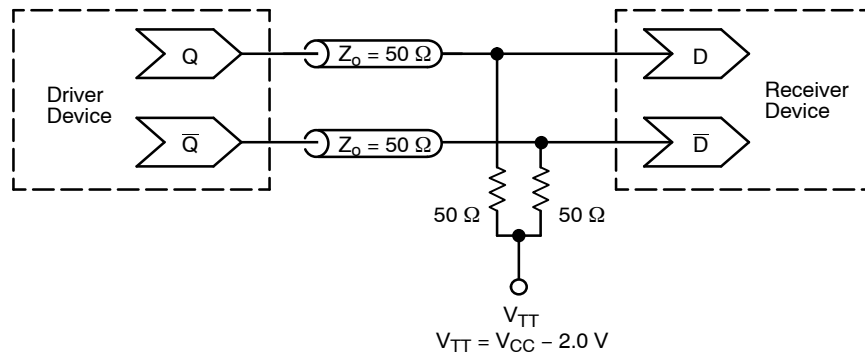
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .



**Figure 2.  $F_{\max}/\text{Jitter}$**

## MC10EP35, MC100EP35



**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC10EP35DG	SOIC-8 NB (Pb-Free)	98 Units / Rail
MC10EP35DR2G	SOIC-8 NB (Pb-Free)	2500 / Tape & Reel
MC10EP35DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10EP35DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100EP35DG	SOIC-8 NB (Pb-Free)	98 Units / Rail
MC100EP35DR2G	SOIC-8 NB (Pb-Free)	2500 / Tape & Reel
MC100EP35DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100EP35DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100EP35MNR4G	DFN-8 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

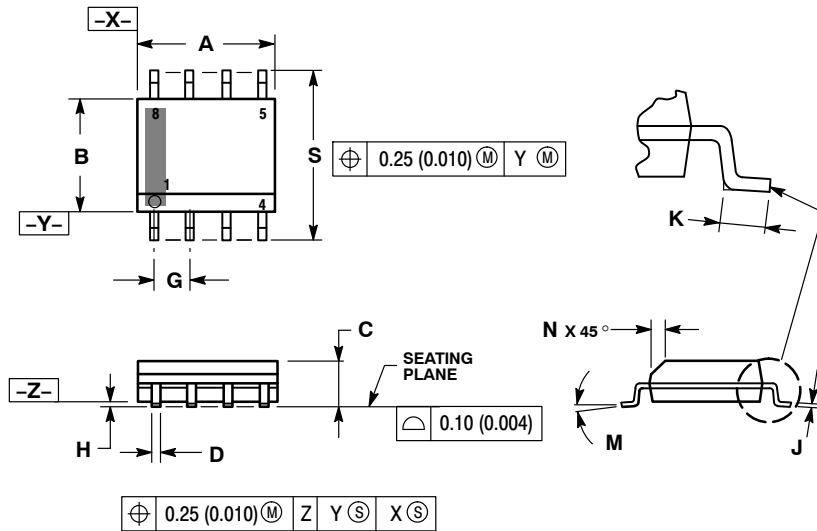
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10EP35, MC100EP35

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AK

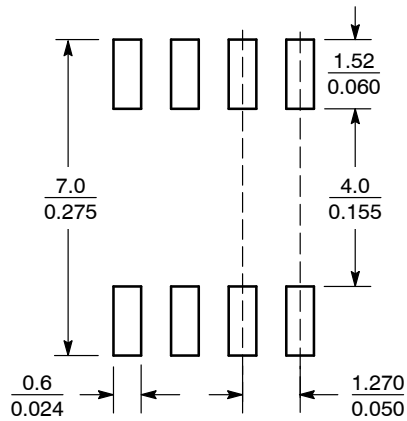


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



SCALE 6:1 (mm/inches)

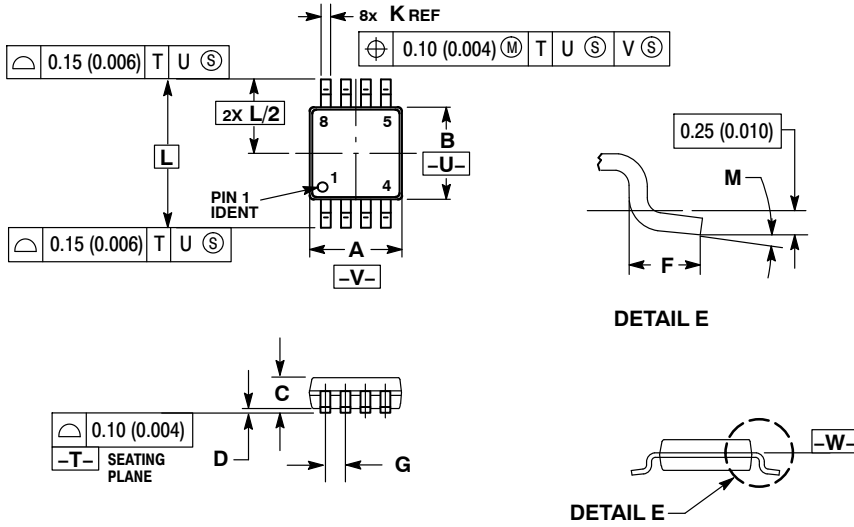
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](#).



# MC10EP35, MC100EP35

## PACKAGE DIMENSIONS

TSSOP-8  
CASE 948R-02  
ISSUE A



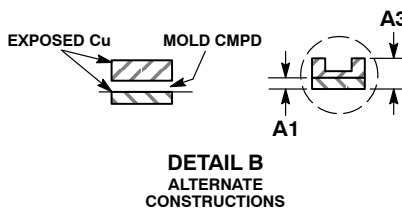
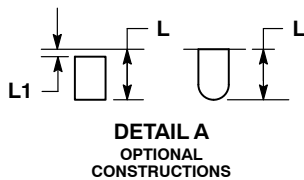
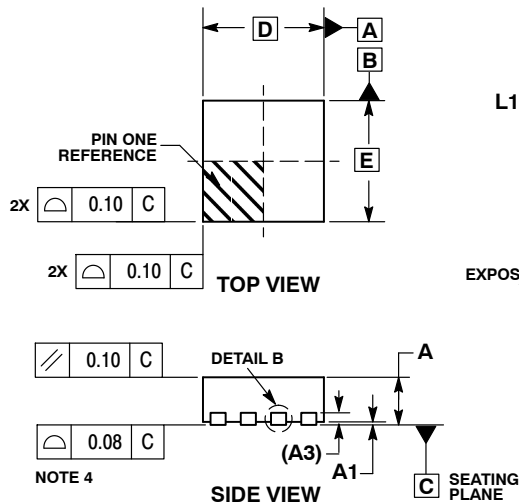
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

# MC10EP35, MC100EP35

## PACKAGE DIMENSIONS

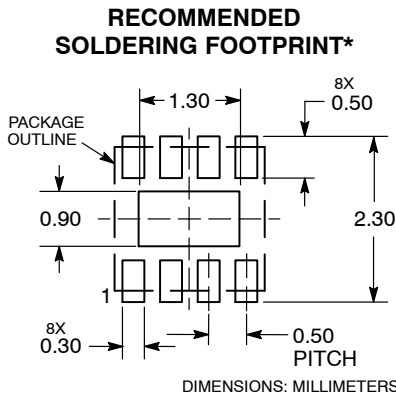
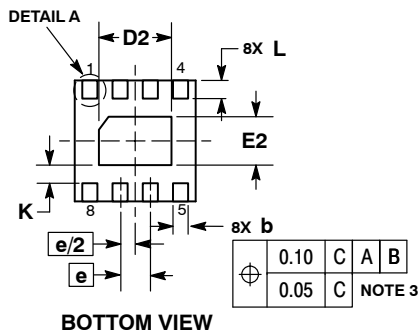
DFN-8 2x2, 0.5P  
CASE 506AA  
ISSUE F



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.10	1.30
E	2.00	BSC
E2	0.70	0.90
e	0.50	BSC
K	0.30	REF
L	0.25	0.35
L1	---	0.10



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDDRRM/D](#).

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