

NCP1200

Product Preview

PWM Current-Mode Controller for Low-Power Universal Off-Line Supplies

Housed in SO-8 or DIP8 package, the NCP1200 represents a major leap toward ultra-compact Switch-Mode Power Supplies. Thanks to a novel concept, the circuit allows the implementation of a complete offline battery charger or a standby SMPS with few external components. Furthermore, an integrated output short-circuit protection lets the designer build an extremely low-cost AC/DC wall adapter associated with a simplified feedback scheme.

With an internal structure operating at a fixed 40 kHz, 60 kHz or 100 kHz, the controller drives low gate-charge switching devices like an IGBT or a MOSFET thus requiring a very small operating power. Thanks to current-mode control, the NCP1200 drastically simplifies the design of reliable and cheap offline converters with excellent audio-susceptibility and inherent pulse-by-pulse control.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so-called skip cycle mode and provides excellent efficiency at light loads. Because this occurs at low peak current, no acoustic noise takes place.

Finally, the IC is self-supplied from the DC rail, eliminating the need of an auxiliary winding. This feature ensures operation in presence of low output voltage or shorts.

Features

- No Auxiliary Winding Operation
- Internal Output Short-Circuit Protection
- Extremely Low No-Load Standby Power
- Current-Mode with Skip-Cycle Capability
- Internal Leading Edge Blanking
- 110 mA Peak Current Source/Sink Capability
- Internally Fixed Frequency at 40 kHz, 60 kHz and 100 kHz
- Direct Optocoupler Connection
- Built-in Frequency Jittering for Lower EMI
- SPICE Models Available for TRANSient and AC Analysis
- Internal Temperature Shutdown

Typical Applications

- AC/DC Adapters
- Offline Battery Chargers
- Auxiliary/Ancillary Power Supplies (USB, Appliances, TVs, etc.)

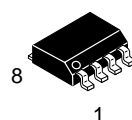
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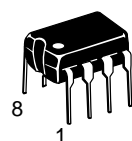
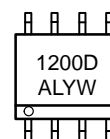
ON Semiconductor™

<http://onsemi.com>

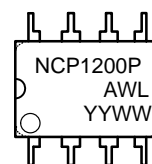
MARKING DIAGRAMS



SO-8
D SUFFIX
CASE 751

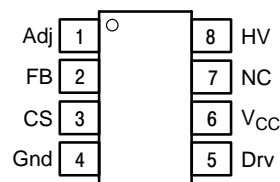


DIP-8
P SUFFIX
CASE 626



A = Assembly Location
L = Wafer Lot
Y, YY = Year
W, WW = Work Week

PIN CONNECTIONS

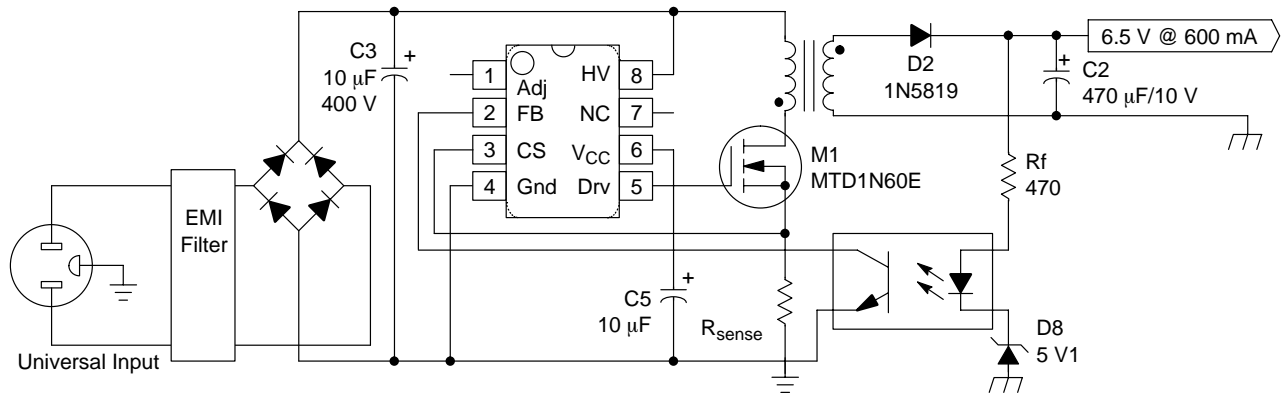


(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

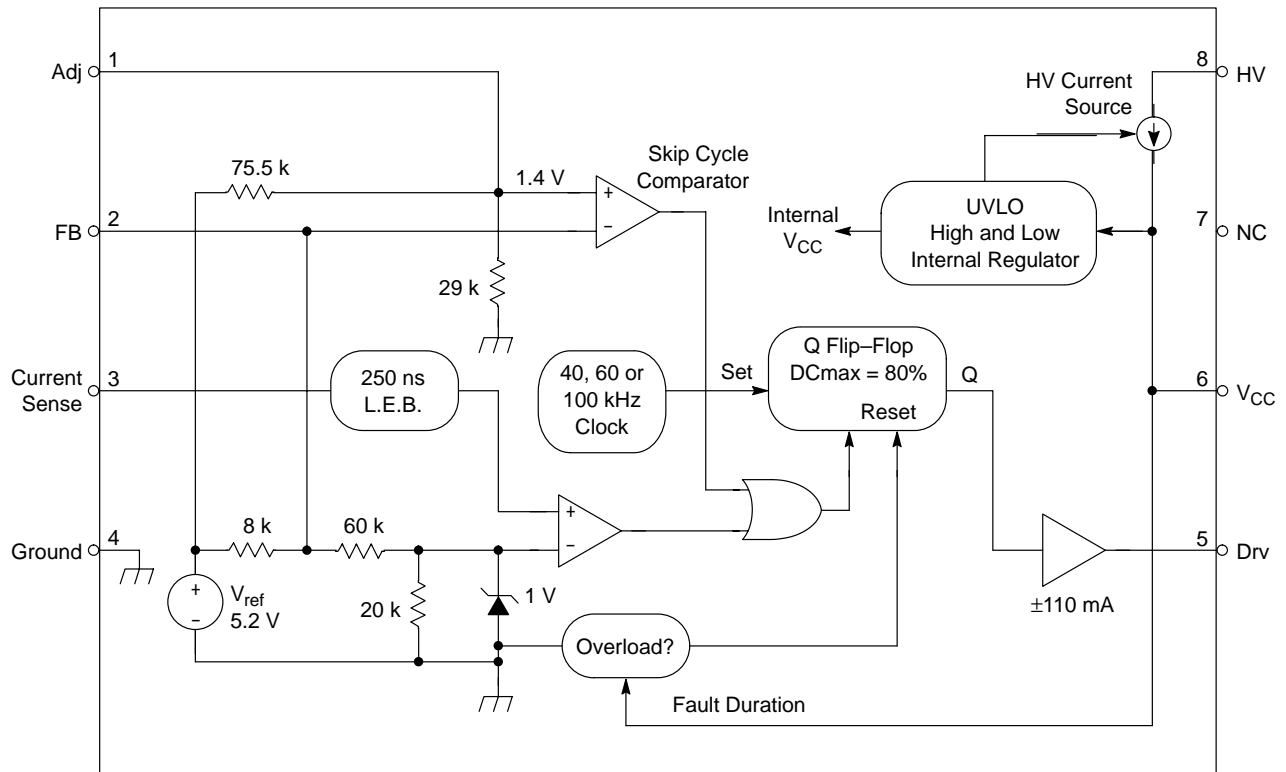
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PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	Adj	Adjust the skipping peak current	This pin lets you adjust the level at which the cycle skipping process takes place
2	FB	Sets the peak current setpoint	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand
3	CS	Current sense input	This pin senses the primary current and routes it to the internal comparator via an L.E.B
4	Gnd	The IC ground	
5	Drv	Driving pulses	The driver's output to an external MOSFET
6	V _{CC}	Supplies the IC	This pin is connected to an external bulk capacitor of typically 10 µF
7	NC	No Connection	This un-connected pin ensures adequate creepage distance
8	HV	Generates the V _{CC} from the line	Connected to the high-voltage rail, this pin injects a constant current into the V _{CC} bulk capacitor

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Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC}	16	V
Thermal Resistance Junction-to-Air, PDIP8 version	$R_{\theta JA}$	100	$^{\circ}C/W$
Thermal Resistance Junction-to-Air, SOIC version	$R_{\theta JA}$	178	$^{\circ}C/W$
Maximum Junction Temperature	T_{Jmax}	150	$^{\circ}C$
Typical Temperature Shutdown	-	140	$^{\circ}C$
Storage Temperature Range	T_{stg}	-60 to +150	$^{\circ}C$
ESD Capability, HBM model (All pins except V_{CC} and HV)	-	2.0	kV
ESD Capability, Machine model	-	200	V
Maximum Voltage on pin 8 (HV), pin 6 (V_{CC}) grounded	-	450	V
Maximum Voltage on pin 8 (HV), pin 6 (V_{CC}) decoupled to ground with 10 μF	-	500	V

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ELECTRICAL CHARACTERISTICS (For typical values $T_J = +25^\circ\text{C}$, for min/max values $T_J = -25^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, $V_{CC} = 11\text{ V}$ unless otherwise noted)

Rating	Pin	Symbol	Min	Typ	Max	Unit
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DYNAMIC SELF-SUPPLY (All frequency versions, otherwise noted)

V_{CC} increasing level at which the current source turns-off	6	V_{CCOFF}	10.8	11.4	12	V
V_{CC} decreasing level at which the current source turns-on	6	V_{CCON}	9.2	9.8	10.5	V
V_{CC} decreasing level at which the latch-off phase ends	6	$V_{CClatch}$	–	6.3	–	V
Internal IC Consumption, no output load on pin 6	6	I_{CC1}	–	710	880 Note 1.	μA
Internal IC Consumption, 1 nF output load on pin 6, $F_{SW} = 40\text{ kHz}$	6	I_{CC2}	–	1.2	1.4 Note 2.	mA
Internal IC Consumption, 1 nF output load on pin 6, $F_{SW} = 60\text{ kHz}$	6	I_{CC2}	–	1.4	1.6 Note 2.	mA
Internal IC Consumption, 1 nF output load on pin 6, $F_{SW} = 100\text{ kHz}$	6	I_{CC2}	–	1.9	2.2 Note 2.	mA
Internal IC Consumption, latch-off phase	6	I_{CC3}	–	350	–	μA

INTERNAL CURRENT SOURCE

High-voltage current source, $V_{CC} = 10\text{ V}$	8	I_{C1}	2.8	4.0	–	mA
High-voltage current source, $V_{CC} = 0$	8	I_{C2}	–	4.9	–	mA

DRIVE OUTPUT

Output voltage rise-time @ $CL = 1\text{ nF}$, 10–90% of output signal	5	T_r	–	67	–	ns
Output voltage fall-time @ $CL = 1\text{ nF}$, 10–90% of output signal	5	T_f	–	28	–	ns
Source resistance (drive = 0, $V_{gate} = V_{CCHMAX} - 1\text{ V}$)	5	R_{OH}	27	40	61	Ω
Sink resistance (drive = 11 V, $V_{gate} = 1\text{ V}$)	5	R_{OL}	5	12	20	Ω

CURRENT COMPARATOR (Pin 5 un-loaded)

Input Bias Current @ 1 V input level on pin 3	3	I_{IB}	–	0.02	–	μA
Maximum internal current setpoint	3	I_{Limit}	0.8	0.9	1.0	V
Default internal current setpoint for skip cycle operation	3	I_{Lskip}	–	350	–	mV
Propagation delay from current detection to gate OFF state	3	T_{DEL}	–	100	160	ns
Leading Edge Blanking Duration	3	T_{LEB}	–	230	–	ns

INTERNAL OSCILLATOR ($V_{CC} = 11\text{ V}$, pin 5 loaded by 1 k Ω)

Oscillation frequency, 40 kHz version	–	f_{OSC}	36	42	48	kHz
Oscillation frequency, 60 kHz version	–	f_{OSC}	52	61	70	kHz
Oscillation frequency, 100 kHz version	–	f_{OSC}	91	103	119	kHz
Built-in frequency jittering, $F_{SW} = 40\text{ kHz}$	–	f_{jitter}	–	300	–	Hz/V
Built-in frequency jittering, $F_{SW} = 60\text{ kHz}$	–	f_{jitter}	–	450	–	Hz/V
Built-in frequency jittering, $F_{SW} = 100\text{ kHz}$	–	f_{jitter}	–	100	–	Hz/V
Maximum duty-cycle	–	D_{max}	74	80	87	%

FEEDBACK SECTION ($V_{CC} = 11\text{ V}$, pin 5 loaded by 1 k Ω)

Internal pull-up resistor	2	R_{up}	–	8.0	–	k Ω
Pin 3 to current setpoint division ratio	–	I_{ratio}	–	4.0	–	–

SKIP CYCLE GENERATION

Default skip mode level	1	V_{skip}	1.1	1.4	1.6	V
Pin 1 internal output impedance	1	Z_{out}	–	25	–	k Ω

1. Max value at $T_J = -25^\circ\text{C}$.

2. Max value @ $T_J = 25^\circ\text{C}$, please see characterization curves.

APPLICATIONS INFORMATION

INTRODUCTION

The NCP1200 implements a standard current mode architecture where the switch-off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part-count is the key parameter, particularly in low-cost AC/DC adapters, auxiliary supplies etc. Thanks to its high-performance High-Voltage technology, the NCP1200 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low-pass filter and self-supply. This later point emphasizes the fact that ON Semiconductor's NCP1200 does NOT need an auxiliary winding to operate: the product is naturally supplied from the high-voltage rail and delivers a V_{CC} to the IC. This system is called the Dynamic Self-Supply (DSS).

Dynamic Self-Supply

The DSS principle is based on the charge/discharge of the V_{CC} bulk capacitor from a low level up to a higher level. We can easily describe the current source operation with a bunch of simple logical equations:

POWER-ON: IF $V_{CC} < V_{CCOFF}$ THEN Current Source is ON, no output pulses

IF V_{CC} decreasing $> V_{CCON}$ THEN Current Source is OFF, output is pulsing

IF V_{CC} increasing $< V_{CCOFF}$ THEN Current Source is ON, output is pulsing

Typical values are: $V_{CCOFF} = 11.4$ V, $V_{CCON} = 9.8$ V

To better understand the operational principle, Figure 1's sketch offers the necessary light:

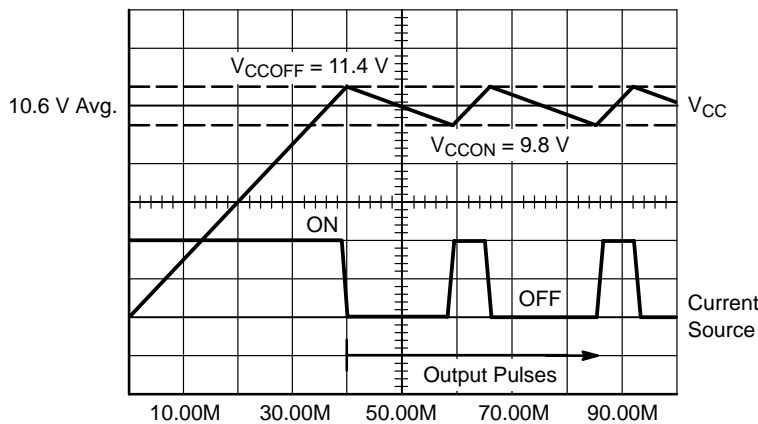


Figure 1. The Charge/Discharge Cycle Over a 10 µF V_{CC} Capacitor

The DSS behavior actually depends on the internal IC consumption and the MOSFET's gate charge, Q_g . If we select a MOSFET like the MTD1N60E, Q_g equals 11 nC (max). With a maximum switching frequency of 48 kHz (for the P40 version), the average power necessary to drive the MOSFET (excluding the driver efficiency and neglecting various voltage drops) is:

$$\frac{1}{2} \cdot F_{sw} \cdot Q_g \cdot V_{CC} \quad \text{with}$$

- F_{sw} = maximum switching frequency
- Q_g = MOSFET's gate charge
- $V_{CC} = V_{GS}$ level applied to the gate

To obtain the final IC current, simply divide this result by V_{CC} : $I_{driver} = \frac{1}{2} \cdot F_{sw} \cdot Q_g = 220 \mu A$. The total standby power consumption at no-load will therefore heavily rely on the internal IC consumption plus the above driving current (altered by the driver's efficiency). Suppose that the IC is supplied from a 400 V DC line. To fully supply the integrated circuit, let's imagine the 4 mA source is ON during 8 ms and OFF during 50 ms. The IC power contribution is therefore: $400 \text{ V} \cdot 4 \text{ mA} \cdot 0.16 = 256 \text{ mW}$. If

for design reasons this contribution is still too high, several solutions exist to diminish it:

1. Use a MOSFET with lower gate charge Q_g
2. Connect pin through a diode (1N4007 typically) to one of the mains input. The average value on pin 8 becomes $\frac{2 \cdot V_{mains} \text{ PEAK}}{\pi}$. Our power contribution example drops to: 160 mW.

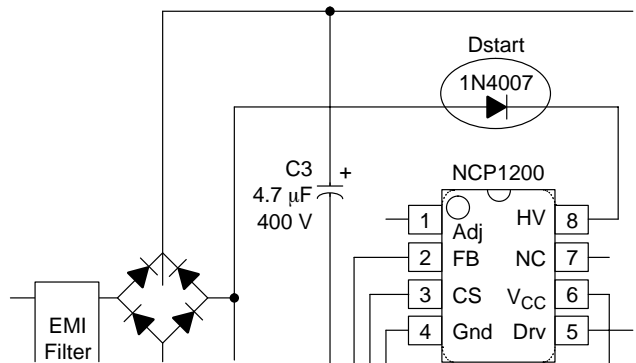


Figure 2. A simple diode naturally reduces the average voltage on pin 8

3. Permanently force the V_{CC} level above V_{CCH} with an auxiliary winding. It will automatically disconnect the internal start-up source and the IC will be fully self-supplied from this winding. Again, the total power drawn from the mains will significantly decrease. Make sure the auxiliary voltage never exceeds the 16 V limit.

Skipping Cycle Mode

The NCP1200 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so-called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 3a). Suppose we have the following component values:

L_p , primary inductance = 1 mH

F_{sw} , switching frequency = 48 kHz

$I_{p\ skip}$ = 300 mA (or 350 mV / R_{sense})

The theoretical power transfer is therefore:

$$\frac{1}{2} \cdot L_p \cdot I_p^2 \cdot F_{sw} = 2.2\ W$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: $2.2 \cdot 0.1 = 220\ mW$.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:

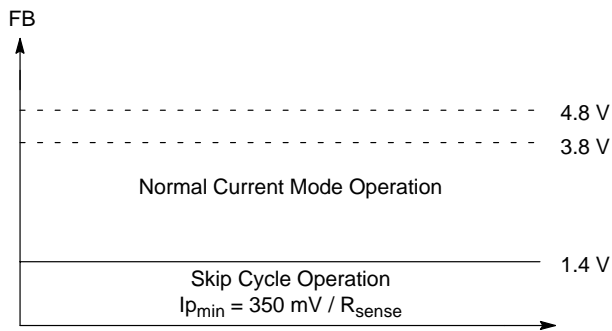


Figure 3. Feedback Voltage Variations

When FB is above the skip cycle threshold (1.4 V by default), the peak current cannot exceed $1\ V/R_{sense}$. When the IC enters the skip cycle mode, the peak current cannot go below $V_{pin1} / 4$ (Figure 3b). The user still has the flexibility to alter this 1.4 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level.

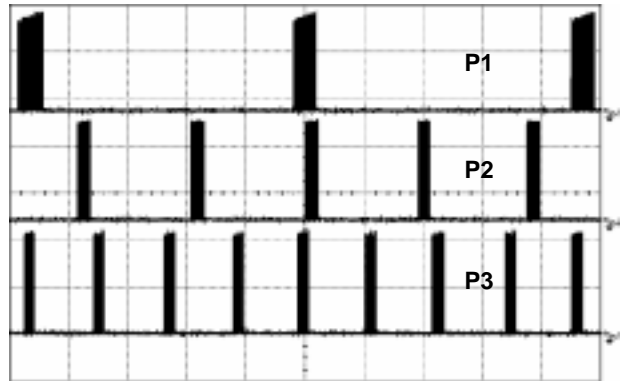


Figure 3a. Output pulses at various power levels (X = 5 $\mu s/div$) $P1 < P2 < P3$

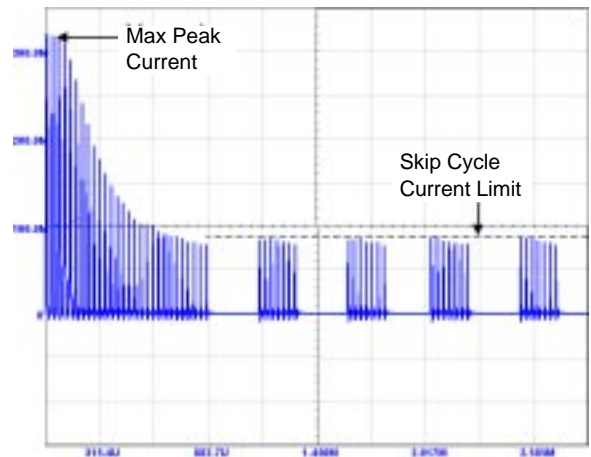


Figure 3b. The skip cycle takes place at low peak currents which guarantees noise free operation

Power Dissipation

The NCP1200 is directly supplied from the DC rail through the internal DSS circuitry. The current flowing through the DSS is therefore the direct image of the NCP1200 current consumption. The total power dissipation can be evaluated using: $(V_{HVDC} - 11\text{ V}) \cdot ICC2$. If we operate the device on a 250 VAC rail, the maximum rectified voltage can go up to 350 VDC. As a result, the worst case dissipation occurs on the 100 kHz version which will dissipate $340 \cdot 1.8\text{ mA} @ T_j = -25^\circ\text{C} = 612\text{ mW}$ (however this 1.8 mA number will drop at higher operating temperatures). A DIP8 package offers a junction-to-ambient thermal resistance of $R_{\theta J-A} 100^\circ\text{C/W}$. The maximum power dissipation can thus be computed knowing the maximum operating ambient temperature (e.g. 70°C) together with the maximum allowable junction temperature (125°C): $P_{max} = \frac{T_{Jmax} - T_{Amax}}{R_{\theta J-A}} = 550\text{ mW}$.

As we can see, we do not reach the worst consumption budget imposed by the 100 kHz version. Two solutions exist to cure this trouble. The first one consists in adding some copper area around the NCP1200 DIP8 footprint. By adding a min-pad area of 80 mm^2 of $35\text{ }\mu\text{ copper}$ (1 oz.) $R_{\theta J-A}$ drops to about 75°C/W which allows the use of the 100 kHz version. The other solutions are:

1. Add a series diode with pin 8 (as suggested in the above lines) to drop the maximum input voltage down to 111 V (350/pi) and thus dissipate less than 200 mW
2. Implement a self-supply through an auxiliary winding to permanently disconnect the self-supply.

SO-8 package offers a worse $R_{\theta J-A}$ compared to that of the DIP8 package: 178°C/W . Again, adding some copper area around the PCB footprint will help decrease this number: $12\text{ mm} \times 12\text{ mm}$ to drop $R_{\theta J-A}$ down to 100°C/W with $35\text{ }\mu\text{ copper}$ thickness (1 oz.) or $6.5\text{ mm} \times 6.5\text{ mm}$ with $70\text{ }\mu\text{ copper}$ thickness (2 oz.). As one can see, we do not recommend using the SO-8 package for the 100 kHz version with DSS active as the IC may not be able to sustain the power (except if you have the adequate place on your PCB). However, using the solution of the series diode or the self-supply through the auxiliary winding does not cause any problem with this frequency version. These options are thoroughly described in the AND8023/D.

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short-circuit protection. A short-circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the FB pin level is pulled up to 4.1 V, as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of feedback loss, e.g. a broken optocoupler. To account for this situation, the NCP1200 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty-cycle. The system recovers when the fault condition disappears.

During the start-up phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. This period of time depends on normal output load conditions and the maximum peak current allowed by the system. The time-out used by this IC works with the V_{CC} decoupling capacitor: as soon as the V_{CC} decreases from the V_{CCOFF} level (typically 11.4 V) the device internally watches for an overload current situation. If this condition is still present when V_{CCON} is reached, the controller stops the driving pulses, prevents the self-supply current source to restart and puts all the circuitry in standby, consuming as little as $350\text{ }\mu\text{A}$ typical ($ICC3$ parameter). As a result, the V_{CC} level slowly discharges toward 0. When this level crosses 6.3 V typical, the controller enters a new startup phase by turning the current source on: V_{CC} rises toward 11.4 V and again delivers output pulses at the $UVLO_H$ crossing point. If the fault condition has been removed before $UVLO_L$ approaches, then the IC continues its normal operation. Otherwise, a new fault cycle takes place. Figure 4 shows the evolution of the signals in presence of a fault.

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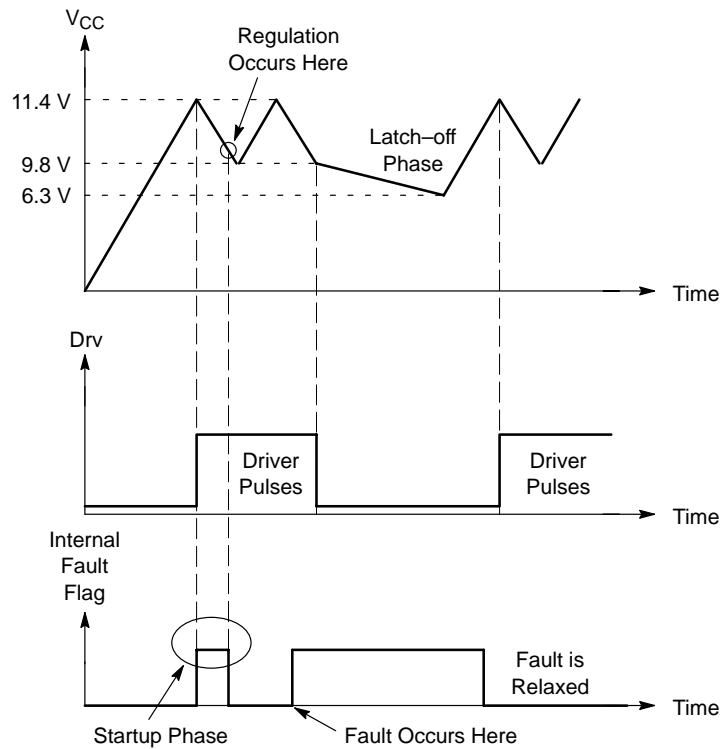


Figure 4. If the fault is relaxed during the V_{CC} natural fall down sequence, the IC automatically resumes. If the fault persists when V_{CC} reached UVLO_L, then the controller cuts everything off until recovery.

Calculating the V_{CC} Capacitor

As the above section describes, the fall down sequence depends upon the V_{CC} level: how long does it take for the V_{CC} line to go from 11.4 V to 9.8 V? The required time depends on the start-up sequence of your system, i.e. when you first apply the power to the IC. The corresponding transient fault duration due to the output capacitor charging must be less than the time needed to discharge from 11.4 V to 9.8 V, otherwise the supply will not properly start. The test consists in either simulating or measuring in the lab how much time the system takes to reach the regulation at full load. Let's suppose that this time corresponds to 6ms. Therefore a V_{CC} fall time of 10 ms could be well appropriated in order to not trigger the overload detection circuitry. If the corresponding IC consumption, including the MOSFET drive, establishes at 1.5 mA, we can calculate the required capacitor using the following formula:

$$\Delta t = \frac{\Delta V \cdot C}{i}, \text{ with } \Delta V = 2V. \text{ Then for a wanted } \Delta t \text{ of } 10 \text{ ms,}$$

C equals 8 μ F or 10 μ F for a standard value. When an overload condition occurs, the IC blocks its internal circuitry and its consumption drops to 350 μ A typical. This happens at V_{CC} = 9.8 V and it remains stuck until V_{CC} reaches 6.5 V: we are in latch-off phase. Again, using the calculated 10 μ F and 350 μ A current consumption, this latch-off phase lasts: 109 ms.

A Typical Application

The below schematic depicts a low-cost 3.5 W AC/DC 6.5 V wall adapter. This is a typical application where the wall-pack must deliver a raw DC level to a given internally regulated apparatus: toys, calculators, CD-players etc. Thanks to the inherent short-circuit protection of the NCP1200, you only need a bunch of components around the IC, keeping the final cost at an extremely low level. The transformer is available from different suppliers as detailed below.

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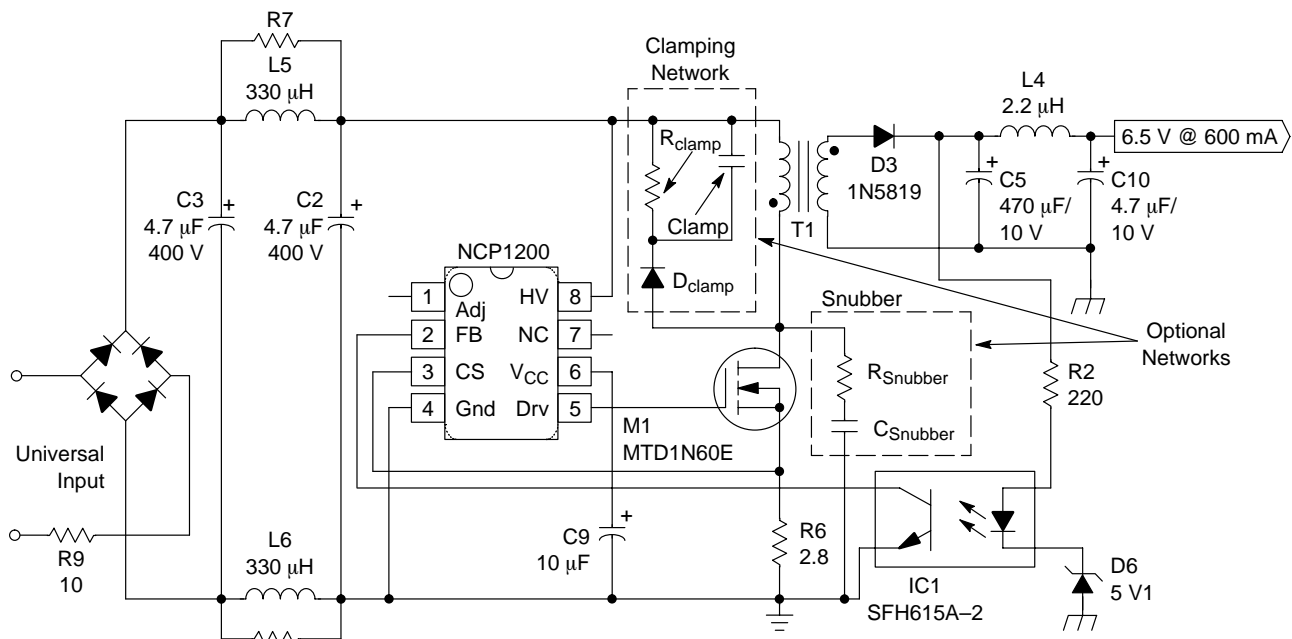


Figure 5. A typical AC/DC wall adapter showing the reduced part count thanks to the NCP1200

T1: $L_p = 2.9$ mH, $N_p:N_s = 1:0.08$, leakage = 80 μ H, E16 core, NCP1200P40

To help designers during the design stage, several manufacturers propose ready-to-use transformers for the above application, but can also develop devices based on your particular specification:

Eldor Corporation Headquarter

Via Plinio 10,
22030 Orsenigo
(Como) Italia
Tel.: +39-031-636 111
Fax : +39-031-636 280
Email: eldor@eldor.it
www.eldor.it

ref. 1: 2262.0058C: 3.5 W version
($L_p = 2.9$ mH, $L_{leak} = 80$ μ H, E16)
ref. 2: 2262.0059A: 5 W version
($L_p = 1.6$ mH, $L_{leak} = 45$ μ H, E16)

EGSTON GesmbH

Grafenbergerstraße 37
3730 Eggenburg
Austria
Tel.: +43 (2984) 2226-0
Fax : +43 (2984) 2226-61
Email: info@egston.com
http://www.egston.com/english/index.htm

ref. 1: F0095001: 3.5 W version
($L_p = 2.7$ mH, $L_{leak} = 30$ μ H, sandwich configuration, E16)

Atelier Special de Bobinage

125 cours Jean Jaures
38130 ECHIROLLES FRANCE
Tel.: 33 (0)4 76 23 02 24
Fax: 33 (0)4 76 22 64 89
Email: asb@wanadoo.fr

ref. 1: NCP1200-10 W-UM: 10 W for USB
($L_p = 1.8$ mH, 60 kHz, 1:0.1, RM8 pot core)

Coilcraft

1102 Silver Lake Road
Cary, Illinois 60013 USA
Tel: (847) 639-6400
Fax: (847) 639-1469
Email: info@coilcraft.com
http://www.coilcraft.com

ref. 1: Y8844-A: 3.5 W version
($L_p = 2.9$ mH, $L_{leak} = 65$ μ H, E16)
ref. 2: Y8848-A: 10 W version
($L_p = 1.8$ mH, $L_{leak} = 45$ μ H, 1:01, E core)

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If the leakage inductance is kept low, the MTD1N60E can withstand *accidental* avalanche energy, e.g. during a high-voltage spike superimposed over the mains, without the help of a clamping network. If this leakage path permanently forces a drain-source voltage above the MOSFET BV_{dss} (600 V), a clamping network is mandatory and must be built around R_{clamp} and C_{clamp}. D_{clamp} shall react extremely fast and can be a MUR160 type. To calculate the component values, the following formulas will help you:

R_{clamp} =

$$\frac{2 \cdot V_{\text{clamp}} \cdot (V_{\text{clamp}} - (V_{\text{out}} + V_f \text{ sec}) \cdot N)}{L_{\text{leak}} \cdot I_p^2 \cdot F_{\text{sw}}}$$

$$C_{\text{clamp}} = \frac{V_{\text{clamp}}}{V_{\text{ripple}} \cdot F_{\text{sw}} \cdot R_{\text{clamp}}}$$

with:

V_{clamp}: the desired clamping level, must be selected to be between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

V_{out} + V_f: the regulated output voltage level + the secondary diode voltage drop

L_{leak}: the primary leakage inductance

N: the N_s:N_p conversion ratio

F_{sw}: the switching frequency

V_{ripple}: the clamping ripple, could be around 20 V

Another option lies in implementing a snubber network which will damp the leakage oscillations but also provide more capacitance at the MOSFET's turn-off. The peak voltage at which the leakage forces the drain is calculated

by: $V_{\text{max}} = I_p \cdot \sqrt{\frac{L_{\text{leak}}}{C_{\text{lump}}}}$ where C_{lump} represents the

total parasitic capacitance seen at the MOSFET opening. Typical values for R_{snubber} and C_{snubber} in this 4W application could respectively be 1.5 kΩ and 47 pF. Further tweaking is nevertheless necessary to tune the dissipated power versus standby power.

Available Documents

“Implementing the NCP1200 in Low-cost AC/DC Converters”, AND8023/D

“Conducted EMI Filter Design for the NCP1200”, AND8032/D

“Ramp Compensation for the NCP1200”, AND8029/D

TRANSient and AC models available to download at: <http://onsemi.com/pub/NCP1200>

NCP1200 design spreadsheet available to download at: <http://onsemi.com/pub/NCP1200>

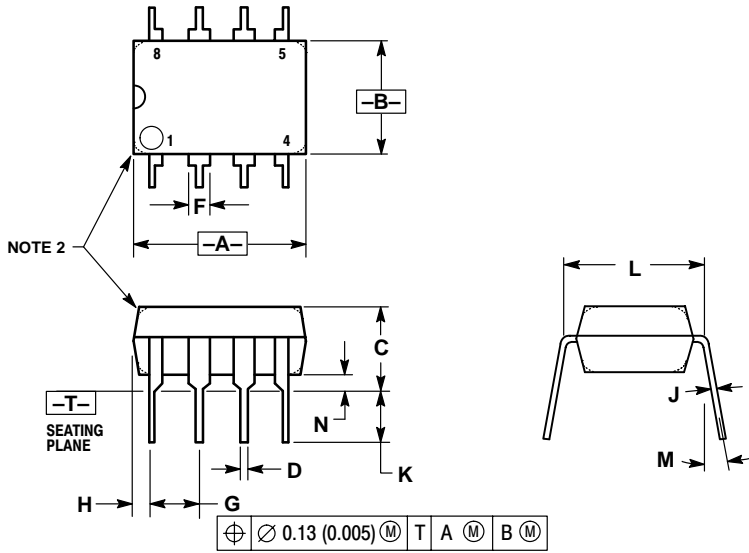
ORDERING INFORMATION

Device	Type	Package	Shipping
NCP1200P40	F _{SW} = 40 kHz	PDIP8	50 Units / Rail
NCP1200D40	F _{SW} = 40 kHz	SO-8	2500 Units / Reel
NCP1200P60	F _{SW} = 60 kHz	PDIP8	50 Units / Rail
NCP1200D60	F _{SW} = 60 kHz	SO-8	2500 Units / Reel
NCP1200D100	F _{SW} = 100 kHz	PDIP8	50 Units / Rail
NCP1200P100	F _{SW} = 100 kHz	SO-8	2500 Units / Reel

NCP1200

PACKAGE DIMENSIONS

DIP8
P SUFFIX
CASE 626-05
ISSUE L

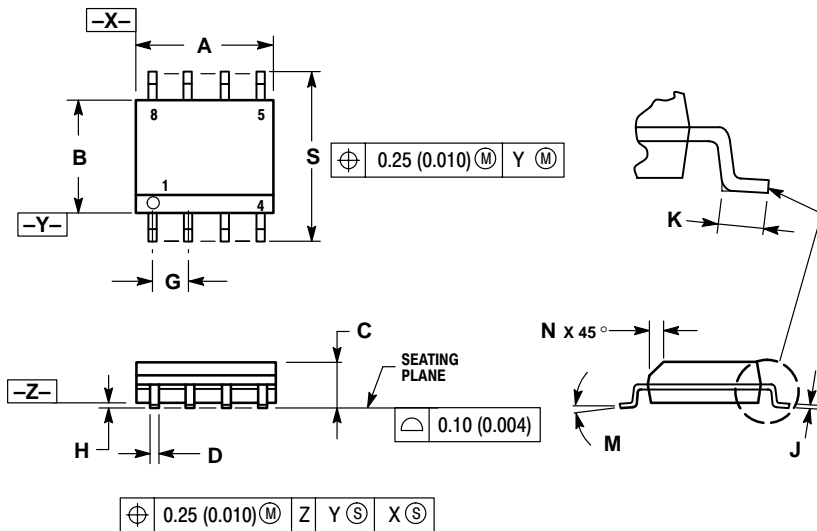


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040


(SO-8)
D SUFFIX
CASE 751-07
ISSUE V



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0° 8°		0° 8°	
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

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